TM-1081

OPERATION AND MAINTENANCE MANUAL

TACAN BEACON TEST SET

PART NO. 7124–0160

6625-22-302-4656

SIERRA
RESEARCH CORPORATION

POST OFFICE BOX 222, BUFFALO, N.Y. 14225

OCTOBER 1973

The information in this operation and maintenance manual does not profess to include all the details of design, production, or variations of the equipment, or to cover all the possible contingencies which may arise during operation, installation or maintenance. Should special problems arise or further information be desired, please contact Sierra Research Corporation.

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SERVICE BULLETIN RECORD

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The above chart is provided for your use in listing SIERRA Service Bulletins covering the equipment in this manual. We suggest that you file these Service Bulletins in your Master Service Bulletin Notebook for future reference.

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DESCRIPTION AND OPERATION

1. GENERAL

A. Purpose of Equipment

The portable TACAN Beacon Test Set model TTS-7124 (see figure 1), hereinafter identified as test set, provides a TACAN capability and a ground beacon signal analysis capability. The test set operator selects the TACAN station to be monitored. Range and bearing information to the selected TACAN station is provided to the operator. In addition, the test set operator can determine the selected ground beacon signal characteristics by indications appearing on the test set. Certain output signals of the test set that are indicative of ground beacon signal characteristics are provided to a recorder (not supplied as part of the test set) so that a permanent record may be obtained. The test set operates in conjunction with either a TACAN ground beacon having full bearing information (15-Hz and 135-Hz modulation) or a TACAN ground beacon having coarse bearing information (15-Hz only modulation) on any one of the 252 channels available (126X-mode and 126Y-mode). The complete frequency assignment for each channel is given in Maintenance/Overhaul Manual for the KDM-7000 Digital DME. The test set contains a built in self-test circuit. Fault indicators are provided to assist in isolating possible problems to a test set component or component subassembly. The test set may be bench or rack mounted and has the capability of operating from any of the following power sources:

(1) 115 VAC, 60 Hz, 1.5 Amp

(2) 28 VDC, 5 Amp

(3) 115 VAC, 400 Hz, 1.0 Amp

Once the type of power source available is determined, the test set is prepared for operation by connecting the appropriate power cable to the input power connector on the rear of the test set. When the test set is rack mounted, the test set can only be operated from a 115V, 400-Hz power source. Four input power cables are provided with the test set.

B. Equipment Supplied

The test set consists of the following components:

(1) Distance Measuring Equipment (DME), Model SRU-7000D

(2) Digital Bearing Unit, Model SBU-7000D

(3) Signal Analyzer Unit, Model SAU-7000

(4) Console Display and Control Panel Unit, Model SPU-7000

(5) DME Mounting Rack

(6) Digital Bearing Unit Mounting Rack

(7) Signal Analyzer Unit Mounting Rack

(8) Cable Assembly, 7124-2529-1

(9) Cable Assembly, 7124-2529-2

(10) Cable Assembly, 7124-2529-3

(11) Cable Assembly, 7124-2529-4

C. Purpose of DME

Refer to Maintenance/Overhaul Manual for KDM-7000 DME, for DME SRU-7000D.

D. Purpose of Digital Bearing Unit

The Digital Bearing Unit uses signals and control functions generated by the DME to compute the bearing from the selected TACAN ground beacon. Additional control signals are received from and provided to the Console Display and Control Panel Unit. Certain output signals of the Digital Bearing Unit are provided for strip-chart recording and to meter monitoring circuits.

E. Purpose of Signal Analyzer Unit

The Signal Analyzer Unit receives signals from the Digital Bearing Unit and the DME. Some of the received signals are converted to analog voltages and provided for strip-chart recording and to meter monitoring circuits. In addition, certain signals are monitored by voltage comparators whose outputs are connected to LED (light emitting diodes) drivers that control OVER and UNDER function indicators on the Console Display and Control Panel Unit.

F. Purpose of Console Display and Control Panel Unit

The Console Display and Control Panel Unit, hereinafter referred to as Panel Unit, provides a means to control the ground beacon

Figure 1. TACAN Beacon Test Set

signal analysis circuit, and monitor outputs from these circuits. The slant range to ground beacon range and bearing information is displayed on the Panel Unit.

G. Equipment Specifications

The specifications of the test set are as follows:

CHARACTERISTIC	SPECIFICATION	
TEST SET PHYSICAL (with subassemblies installed)		
	Case Configuration	Rack Mounted Configuration
Height	13.00 in.	12.50 in.
Width	19.75 in.	19.00 in.
Depth	21.70 in.	18.50 in.
Weight	90 lb	47 lb
TEST SET OPERATIONAL		
Power Requirements (Cooling fan operates with 115 VAC, 60-Hz input power only)	115 VAC, 60 Hz, at 1.5 amp or 115 VAC, 400 Hz, at 1.0 amp or 28 VDC at 5 amp (Power connector is type MS3112E12-10P.)	
R-F Power Output	Refer to Maintenance/Overhaul Manual for KDM 7000, for DME SRU-7000D. (Power output can be attenuated by insertion of 30 db (± 1 db) attenuator on test set front panel.)	
Recorder Interface (Analog output signals identified below are provided on a single connector suitable for connecting to an external analog recorder with an impedance of not less than 2000 ohms.)	MS3112E14-15S connector	

CHARACTERISTIC	SPECIFICATION	
Recorder Interface (cont)		
Bearing Deviation	-13° to +13° range with an accuracy of ± 0.2° and a scale factor of 1°/V	-13 - +1
15/135 Hz Phase Coherency	-20° to +20° range with an accuracy of ± 1.0° and a scale factor of 2°/V	-10 - +10
15 Hz Modulation Level	0 to 40% with an accuracy of ± 2.0% and a scale factor of 4%/V	0 - 10v
135 Hz Modulation Level	0 to 40% with an accuracy of ± 2.0% and a scale factor of 4%/V	0 - 10v
Range Replies	0 to 100% with an accuracy of ± 2.0% and a scale factor of 10%/V	0 - 10v
Receiver AGC	-20 to -90 dbm range with an accuracy of ± 5.0 db and a scale factor of 10 db/V (nominal)	0 - 10v
Bearing Flag	0 or 5V dc, 5V dc = valid bearing	0 - 10v
Squitter Random Pairs	0 to 100% of selected nominal with an accuracy of ± 2.0% and a scale factor of 10%/V	0 - 10v
Antenna Speed Error	-10 to +10 rpm of 900 rpm with an accuracy of ± 0.2 rpm and a scale factor of 1 rpm/V	-10 - +10
Oscilloscope Outputs (Following outputs are provided for oscilloscope display and synchronization)		
Composite Video	BNC Type Connector	
Transmit Pulse Waveform	BNC Type Connector	
Synchronization pulses for either range interrogation pulses, range reply pulses, main reference groups (MRG's) or auxiliary reference groups (ARG's)	BNC Type Connector	
Suppressor	BNC Type Connector	

CHARACTERISTIC	SPECIFICATION
Antenna Impedance	52-ohm coaxial line
Audio Output (Identification Tone)	75 mw (min), 1350 Hz audio output for internal speaker or headset (standard headset jack provided). Insertion of headset plug disables internal speaker.
Digital Display	
Bearing	000.0° to 359.8° TO or FROM beacon (factory selectable - set to FROM)
Range	000.0 to 399.9 nautical miles
To/From Indicators	Resolves course deviation ambiguity
Range Failure Indicator	Indicates a DME failure
Bearing Failure Indicator	Indicates a Digital Bearing Unit failure
Under/Over Tolerance Indicators (under or over indicator illuminates if any of following signals fall outside tolerances	
Antenna Speed	900 ± 1.8 rpm
Squitter Rate	
TACAN	2700 pps ± 5%
DME	700 to 2850 pps
Phase Coherency	± 5 degrees
MRG	ICAO specification
ARG	ICAO specification
ARG Under Indicator	Illuminates if number of ARG's per antenna revolution is less than 8.
Analog Displays (Panel Meters)	
AGC Voltage Indicator	AGC voltage to DME receiver is displayed on a 0-to-10 volts full scale meter.

CHARACTERISTIC	SPECIFICATION
Analog Displays (Panel Meters) (cont)	
Antenna Speed Indicator	Antenna speed of beacon under test is displayed on a normal zero-center meter calibrated to indicate rpm over range of 895 to 905 rpm.
Beacon Signal Characteristics Indicator (Following signals selectable by switch)	
15 Hz Modulation Level	Zero to 50% range
135 Hz Modulation Level	Zero to 50% range
Squitter Rate	Zero to 100% range
Percent Range Replies	Zero to 100% range
Course Deviation Indicator	Course deviation is displayed on a normal zero-center type meter calibrated to indicate 0 ± 10 degrees.
Phase Coherency Indicator	Measured phase coherency is displayed on a normal zero-center type meter calibrated to indicate 0 ± 20 degrees.
Operating and Control Functions (Refer to paragraph 2 of Operating Procedures Section.)	
TEST SET ENVIRONMENTAL	
Temperature	-40°C to +55°C
Humidity	95%
Altitude	30,000 feet operating
Vibration	0.02-inch double amplitude with 3G max acceleration 10 to 55 Hz, 1.5G 55 to 500 Hz
Shock	Rigid mounting 6G operational, 15G crash safety

CHARACTERISTIC	SPECIFICATION
TEST SET ENVIRONMENTAL (Cont)	
DME	Refer to Maintenance/Overhaul Manual for KDM 7000, for DME SRU-7000D.
DIGITAL BEARING UNIT PHYSICAL	
Height	7.625 in.
Width	2.38 in.
Depth	15.08 in.
Weight	6-3/4 lb
Size	1/4 ATR SHORT
DIGITAL BEARING UNIT OPERATIONAL	
Power Requirements	115 VAC, 400 Hz at 0.26 amperes
Bearing Readout	Digital bearing output for display on digital indicator of Panel Unit
Accuracy (with both 15-Hz and 135-Hz bearing information present)	± 0.2 degree with respect to internal calibration signal ± 1 degree for signal level of -80 dbm to -90 dbm ± 0.4 degree for signal level of -20 dbm to -80 dbm Error will not increase under dynamic tracking conditions up to 4 degrees per second
Accuracy (with 15-Hz bearing information present)	± 1.0 degree with respect to internal calibration signal ± 2.0 degrees for a signal level of -20 dbm to -80 dbm ± 5.0 degrees for a signa level of -80 dbm to -90 dbm Error will not increase under dynamic tracking conditions up to 0.5 degree per second.

CHARACTERISTIC	SPECIFICATION
DIGITAL BEARING UNIT OPERATIONAL (Cont)	
Acquisition Time	3 seconds maximum to search, track, and display a valid bearing signal
Tracking Rate	4 degrees per second (max) with 15 and 135-Hz modulation. 0.5 degrees per second (min) with 15-Hz information only. This applies at all bearings within modulation limits of 15 to 55 percent and modulation indexes of no more than 0.30 or less than 0.07.
Memory Time	3 to 10 seconds (selectable) before searching for a lost signal. Factory set at 6 seconds.
Self Test	Automatic continuous monitoring for failures. Operator initiated self test with zero-degree bearing readout in fine bearing and 10-degree bearing readout in coarse bearing.
DIGITAL BEARING UNIT ENVIRONMENTAL	
Temperature	-40°C to +55°C continuous operation
Humidity	95%
Altitude	30,000 feet operating
Vibration	Same as listed under test set
Shock	Same as listed under test set
SIGNAL ANALYZER UNIT PHYSICAL	
Height	7.625 in.
Width	2.38 in.
Depth	15.08 in.
Weight	5-3/4 lb
Size	1/4 ATR Short

CHARACTERISTIC	SPECIFICATION
SIGNAL ANALYZER UNIT OPERATIONAL	
Power Requirements	115 VAC, 400 Hz at 0.16 amp
Bearing Deviation	D-c voltage comparing station bearing with output of course selected on Panel Unit. Accurate within ± 0.2 degree from zero to ±10 degrees of selected course.
Antenna Speed	Provides outputs that operate indicators on Panel Unit if ground beacon antenna speed exceeds ± 1.8 rpm of nominal speed of 900 rpm.
Squitter Rate	Provides outputs that operate indicators on Panel Unit if squitter rate of ground beacon exceeds ±5 percent of nominal squitter rate for TACAN beacon, or if squitter rate falls outside the 700 to 2850 pulse pairs per second for a DME only station.
Phase Coherency	Provides outputs that operate indicators on Panel Unit if phase difference between 15 Hz a-m signal and 135 Hz a-m signal exceeds ± 5 degrees.
Main Reference Group (MRG) Size	Provides outputs that operate indicators on Panel Unit if MRG exceeds ± 1 pulse pair per group
Auxiliary Reference Group (ARG) Size	Provides outputs that operate indicators on Panel Unit if ARG exceeds ± 1 pulse pair per group.
ARG Counter	Provides an output that operates an indicator on Panel Unit if ARG's per antenna revolution is less than eight.

CHARACTERISTIC	SPECIFICATION
SIGNAL ANALYZER UNIT OPERATIONAL (Cont)	
Percent of Modulation, 15 Hz	Analog output voltage proportional to 15-Hz modulation on received signal over a range of zero to 40 percent ± 1 percent modulation. Output in 0 to 10V range at 0.25V per 1 percent.
Percent of Modulation, 135 Hz	Analog output voltage proportional to 135-Hz modulation on received signal over a range of zero to 40 percent ± 1 percent modulation. Output in 0 to 10V range at 0.25V per 1 percent.
Percent of Range Replies	Provides output voltage to indicate percent of range reply pulses for DME unit interrogations. Cover a range reply rate of at least 30 to 80 percent with output of 10 percent per volt in 0 to 10V range.
Oscilloscope Sync Outputs	Provides signal to trigger oscilloscope to facilitate observation of MRG, first ARG, reply pulse pair, and transmitter pulse pair.
AGC Output	Provides AGC signal to recording equipment.
SIGNAL ANALYZER UNIT ENVIRONMENTAL (Same as Digital Bearing Unit)	
PANEL UNIT PHYSICAL	
Height	7.25 in.
Width	5.21 in.
Depth	3.6 in.
Weight	3 lb

CHARACTERISTIC	SPECIFICATION
PANEL UNIT OPERATIONAL	
Power Requirements	115 VAC, 400 Hz at 0.18 amp
Digital Range Indicator	Displays range to beacon from 0 to 399.9 nautical miles in hundreds, tens, units, and tenths nautical mile.
Digital Bearing Indicator	Displays bearing FROM beacon from 000.0 to 359.8 degrees in 0.2-degree increments.
NOTE: Additional controls and indicators are described in paragraph 2 of Operating Procedures section.	
PANEL UNIT ENVIRONMENTAL	
Temperature	-20°C to +55°C
Humidity	95%
Altitude	30,000 feet operating
Vibration	Same as listed under test set
Shock	Same as listed under test set

2. THEORY OF OPERATION

A. Test Set General Theory

(1) The test set consists of a DME, Digital Bearing Unit, Signal Analyzer Unit, Console Display and Control Panel Unit (Panel Unit), and a front panel consisting essentially of a CHANNEL/MODE selector, control switches, meters, and connectors (see figure 2). The antenna and recorder are not provided as part of the test set. The CHANNEL/MODE selector permits the test set operator to select the desired frequency channel and either the X or Y operating mode. The TRANSMIT pushbutton/indicator switch S7503 controls the logic level of the 1 = STANDBY signal to the CHANNEL/MODE selector. When S7503 is depressed, released, and illuminated, the 1 = STANDBY signal is at ground level (logical 0) and the MANUAL STANDBY signal to the DME and Panel Unit becomes a logical 1 (in the CHANNEL/MODE selector) thus the test set operates in the TRANSMIT mode (DME transmits range interrogate pulse groups). If the TRANSMIT pushbutton/indicator switch is depressed, released, and is extinguished, the 1 = STANDBY signal is at a logical 1 level. The resulting logical 0 MANUAL STANDBY signal holds the test set in the receive mode. All the functions of the test set except displaying range-to-beacon information are performed with the test set operating in the receive mode. To display range to beacon, the test set must be operated in the transmit mode.

(2) The r-f signal from the antenna is applied to the DME. A 30-db attenuator can be inserted between the antenna and r-f signal input to the DME. The DME computes the slant range to the selected ground beacon by measuring the time from transmission of an interrogation pulse-pair from the DME to receipt of a reply pulse-pair from the ground beacon. This distance data, supplied in binary coded decimal (BCD) serial format, is then processed and displayed on the RANGE NAUTICAL MILES indicator of the Panel Unit. Three output signals from the DME are necessary for displaying the range data on the Panel Unit. These signals are identified as SERIAL BCD DIST DATA, SERIAL BCD CLOCK, and SERIAL BCD WORD SYNC. Complete theory of operation of the DME is given in Maintenance/Overhaul Manual for KDM 7000 DME, for DME SRU-7000D.

(3) The identity tone of the selected beacon (audio output of the DME) is provided to either speaker LS7501 or to a headset connected to HEADSET jack P/J7501. When a headset is used, audio to the speaker is inhibited. VOLUME control R7501 permits varying the volume of the identity tone at either the speaker or headset.

(4) The 27.5V DC FLAG ALARM signal output of the DME is provided to the Panel Unit. This signal causes the RANGE FAILURE indicator on the Panel Unit to illuminate and the RANGE NAUTICAL MILES indicator to be blank if there is a DME failure. The RANGE NAUTICAL MILES indicator decimal point is always illuminated when power is applied to the test set (Panel Unit POWER switch in ON position). The 200 MILE RANGE OVRD input signal to the DME is at ground level thus allowing the DME to operate to a range of 399 miles.

(5) Six output signals of the DME are applied to the Digital Bearing Unit and are identified as WIDEBAND SIGNAL, FERRIS DISCRIMINATOR, 0 = MONITOR RESET, 1 = Y MODE, 0 = SUPPRESS, and 0 = TEST. The WIDEBAND SIGNAL is the detected output of the i-f amplifier. When the FERRIS DISCRIMINATOR signal is at a high level, it signifies that the received r-f signal is on frequency. The 0 = SUPPRESS signal prevents decoding operation performed by the Digital Bearing Unit when the DME is transmitting, or during the receipt of any other suppression pulses from other equipments. The 1 = Y MODE signal controls the decoding operation in the Digital Bearing Unit such that Y-Mode pulses are decoded when this signal is high and X-Mode pulses are decoded when the signal is low. The 1 = Y MODE signal is also provided to the Signal Analyzer Unit for controlling the reference group size circuit operation. The 0 = MONITOR RESET signal momentarily changes to a low level when a channel change is made. This low level signal overrides the memory feature of the Digital Bearing Unit thus allowing for the immediate processing of a new signal. The 0 = TEST output of the DME changes to a low state when the test set is in self test. This signal programs the Digital Bearing Unit to the test condition (also programmed to test condition by 0 = CALIBRATE signal). The DME is in the test condition when the SELF TEST push-button/indicator is illuminated.

(6) In addition to the 1 = Y MODE signal, three more outputs of the DME are provided to the Signal Analyzer Unit. These

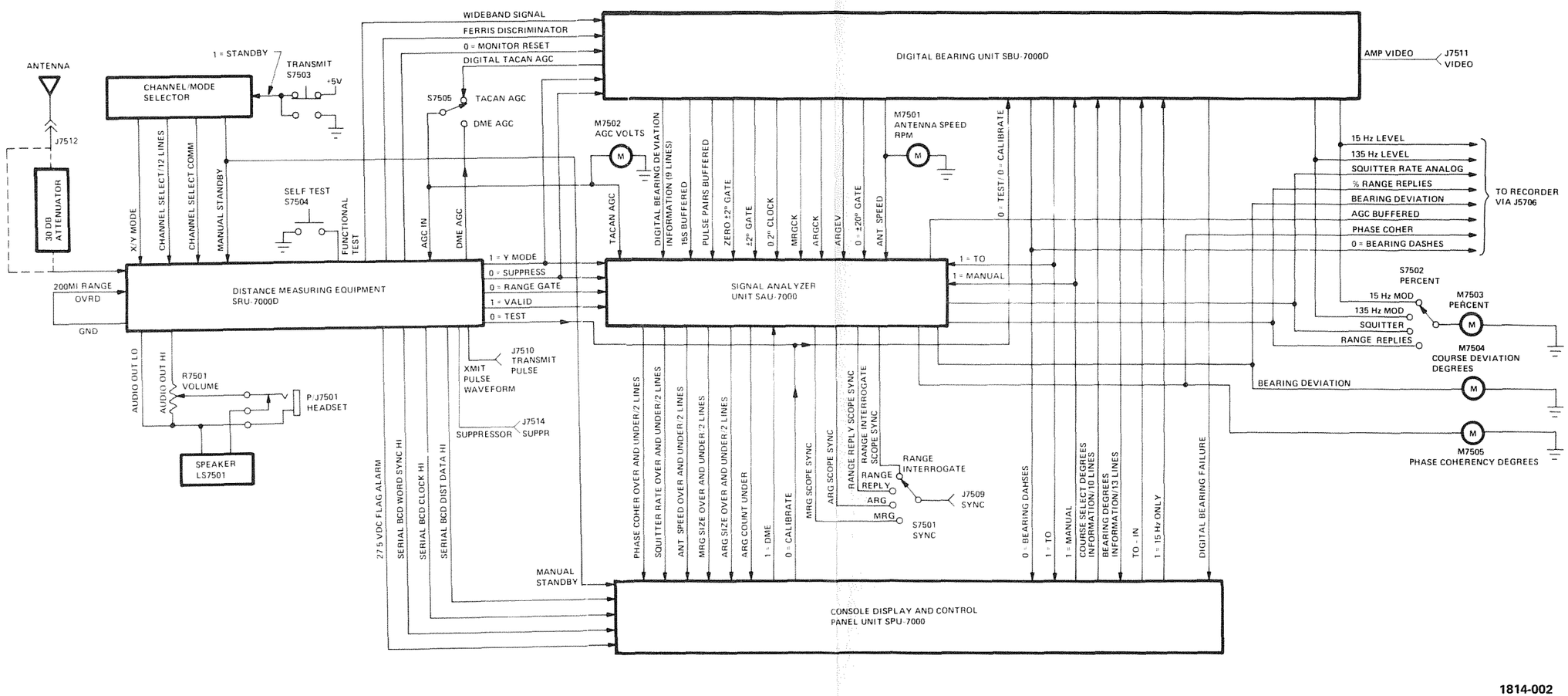


Figure 2. TACAN Beacon Test Set Block Diagram

signals are identified as 0 = SUPPRESS, 0 = RANGE GATE and 1 = VALID. The 0 = RANGE GATE and 1 = VALID signals are processed in the Signal Analyzer Unit to produce the RANGE REPLY SCOPE SYNC signal and % RANGE REPLIES signal respectively. The RANGE REPLY SCOPE SYNC signal is applied to SYNC connector J7509 when the SYNC switch S7501 is in RANGE REPLY position. The % RANGE REPLIES signal is continuously provided to RECORDER connector J5706 and to the PERCENT meter M7503 when the PERCENT switch S7502 is in RANGE REPLIES position. The 0 = SUPPRESS signal is processed in the Signal Analyzer Unit to produce the RANGE INTERROGATE SCOPE SYNC signal. This signal is provided to the SYNC connector J7509 when the SYNC switch S7501 is in the RANGE INTERROGATE position.

(7) The WIDEBAND SIGNAL output of the DME is applied to the Digital Bearing Unit. The Digital Bearing Unit computes the bearing FROM the ground beacon and provides parallel BCD bearing degrees information on 13 lines to the Panel Unit. The COURSE SELECT DEGREES thumbwheel switches on the Panel Unit permit selection of a desired course from 000 to 359 degrees, provided the OBS CONTROL on the Panel Unit is set to the MAN position. This course select information is provided on ten lines to the Digital Bearing Unit where it is compared against the actual bearing. Course deviation information (digital bearing) is provided as parallel offset-BCD on nine lines from the Digital Bearing Unit to the Signal Analyzer Unit. A digital-to-analog converter in the Signal Analyzer Unit converts these nine digital inputs to an analog voltage (BEARING DEVIATION) that is provided to the COURSE DEVIATION DEGREES meter M7504 and a strip-chart recorder. When the OBS CONTROL is in the AUTO position, the COURSE SELECT DEGREES control is disabled and the course select information to the Digital Bearing Unit is equivalent to 000 degrees. In this automatic mode, the 1 = MANUAL output signal of the Panel Unit is at a low level. This, in turn, causes the 1 = TO output signal of the Digital Bearing Unit to be at a low level, thus causing the FROM indicator on the Panel Unit to illuminate. In the automatic mode, the low level 1 = MANUAL signal causes the bearing deviation to be computed from the nearest cardinal (multiples of 10°) radial.

(8) The Digital Bearing Unit provides a d-c level proportional to the percent of modulation of the 15-Hz component (15 HZ LEVEL) of the received signal, and a d-c level proportional to the percent of modulation of the 135-Hz component (135 HZ LEVEL) of the received signal. These d-c levels are provided for recording purposes and to the PERCENT meter M7503 via PERCENT switch S7502. If the Digital Bearing Unit is not locked to a received signal, the 0 = BEARING DASHES signal is at a low level. This signal causes the BEARING DEGREES indicator on the Panel Unit to display dashes. The 0 = BEARING DASHES signal is also provided for recording purposes.

(9) The WIDEBAND SIGNAL is processed by the Digital Bearing Unit and produces the 15S BUFFERED, PULSE PAIRS BUFFERED, ANT. SPEED, MRGCK (main reference group clock), ARGCK (auxiliary reference group clock), and ARGEV (auxiliary reference group event) signals. These signals are provided to the Signal Analyzer Unit. The ANT. SPEED signal is also applied to the ANTENNA SPEED RPM meter M7501. This meter indicates antenna speed from 895 to 905 revolutions per minute. The Digital Bearing Unit also generates a 0.2° CLOCK BUFFERED signal and three GATE signals (ZERO ± 2° GATE, ±2° GATE, 0 = ±20° GATE) all of which are applied to the Signal Analyzer Unit. If the operation of the Digital Bearing Unit fails, the DIGITAL BEARING FAILURE output signal causes the BEARING FAILURE indicator on the Panel Unit to illuminate. The DIGITAL BEARING FAILURE signal also causes the BEARING DEGREES indicator to be blank if there is a Digital Bearing Unit failure. The BEARING DEGREES decimal point is always illuminated when the Panel Unit POWER switch is in the ON position.

(10) The Signal Analyzer Unit processes the ANT. SPEED signal to determine if it is within 1.8 rpm of 900 rpm. The ANT. SPEED OVER and UNDER outputs of the Signal Analyzer Unit will cause the ANT. SPEED ± 1.8 RPM OVER or UNDER indicators (respectively) on the Panel Unit to illuminate if an out-of-tolerance condition is detected.

(11) The PULSE PAIRS BUFFERED output signal of the Digital Bearing Unit is analyzed by the Signal Analyzer Unit to determine if the ground beacon squitter rate is within tolerance. An out-of-tolerance condition is displayed by the SQUITTER RATE ±5% OVER and UNDER indicators on the Panel Unit.

The SQUITTER RATE OVER and UNDER output signals of the Signal Analyzer Unit control these indicators. The SQUITTER switch on the Panel Unit permits the Signal Analyzer Unit to analyze the squitter rate of a TACAN ground beacon or DME-only ground beacon. The Panel Unit output that controls Signal Analyzer Unit circuits that permit this function is the 1 = DME signal. The SQUITTER RATE ANALOG signal from the Signal Analyzer Unit is provided (via RECORDER connector J5706) for strip-chart recording, and to the PERCENT meter M7503 via PERCENT switch S7502.

(12) The 15S BUFFERED output of the Digital Bearing Unit, in conjunction with the 0.2° CLOCK BUFFERED signal and 0 = ±20° GATE signal, is processed in the Signal Analyzer Unit to determine the phase coherency of the ground beacon. Phase coherency in this instance is defined as the phase difference between the 15 Hz amplitude-modulated signal and the 135 Hz amplitude-modulated signal. The PHASE COHER OVER and UNDER output signals of the Signal Analyzer Unit cause the PHASE COHER ±5° OVER and UNDER indicators on the Panel Unit to indicate if this phase coherency is greater than plus five degrees, or less than minus five degrees respectively. The PHASE COHER analog signal output of the Signal Analyzer Unit is provided (via RECORDER connector J5706) for strip-chart recording, and to the PHASE COHERENCY DEGREES meter M7505.

(13) The MRGCK output signal of the Digital Bearing Unit is provided to the Signal Analyzer Unit to determine if the MRG size is correct. The 1 = Y MODE input to the Signal Analyzer Unit permits this to be accomplished for either X or Y modes of operation. If the MRG does not have the correct number of pulses, the MRG SIZE OVER or UNDER output signals of the Signal Analyzer Unit causes the MRG SIZE OVER or UNDER indicator on the Panel Unit to display the appropriate fault condition.

(14) In a similar manner, the ARGCK output of the Digital Bearing Unit is checked in the Signal Analyzer Unit for a over or under size condition. The ARG SIZE OVER and UNDER output signals of the Signal Analyzer Unit control the ARG SIZE OVER and UNDER indicators on the Panel Unit thus allowing an incorrect condition to be indicated. An ARG count circuit in the Signal Analyzer Unit analyzes the ARGEV signal to determine if there are eight ARG events for every antenna revolution.

If there are less than eight ARG events, the ARG COUNT UNDER output of the Signal Analyzer Unit causes the ARG COUNT UNDER indicator on the Panel Unit to illuminate. The Signal Analyzer Unit also provides MRG SCOPE SYNC and ARG SCOPE SYNC signals to SYNC connector J7509 (via SYNC switch S7501) for oscilloscopic analysis of the video signal.

(15) The OPERATE/CALIBRATE switch on the Panel Unit permits the Digital Bearing Unit to be operated in the calibrate or operate mode. The 0 = CALIBRATE output signal of the Panel Unit, an output of the OPERATE/CALIBRATE switch, performs this mode selection. When in the calibrate mode, a precisely-known bearing is simulated. This bearing, which is 000.0 degrees in NORMAL mode, or 010.0 degrees in the 15 HZ ONLY mode, may be used to align the bandpass filters in the Digital Bearing Unit, or to provide a reference datum for digital bearing outputs.

(16) The TO-IN input signal to the Digital Bearing Unit is jumpered to ground in the Panel Unit. This signal causes the digital BEARING DEGREES readout on the Panel Unit to indicate bearing FROM the ground beacon. If this signal is jumpered to a logical 1 (+5V), the digital BEARING DEGREES readout will indicate bearing TO the ground beacon. If the OBS CONTROL is in the MAN position, and the test set bearing TO the beacon is within ±90 degrees of the course selected by the COURSE SELECT DEGREES thumbwheel switches, the TO indicator on the Panel Unit is illuminated. If the test set bearing FROM the beacon is within ±90 degrees of the selected course, the FROM indicator is illuminated.

(17) The DIGITAL TACAN AGC output of the Digital Bearing Unit is applied to the TACAN AGC/DME AGC switch S7505. This switch is normally left in the TACAN AGC position. The agc voltage developed in the Digital Bearing Unit is applied to the DME (AGC IN) and to the AGC VOLTS meter M7502. This signal is also applied to the Signal Analyzer Unit where it is buffered and provided via RECORDER connector J5706 for strip-chart recording. When the TACAN AGC/DME AGC switch S7505 is in the DME AGC position, the DME AGC signal is reapplied to the DME.

(18) Three additional test set signals are provided to connectors. These signals are identified as XMIT PULSE WAVEFORM, SUPPRESSOR, and AMP VIDEO. The XMIT PULSE WAVEFORM and SUPPRESSOR signals are outputs of the DME and are provided the TRANSMIT PULSE connector J7510 and the SUPPR connector J7514 respectively. The AMP.VIDEO signal is an output of the Digital Bearing Unit and is provided to VIDEO connector J7511. The XMIT PULSE WAVEFORM and AMP. VIDEO signals are available for analysis on oscilloscope. The SUPPRESSOR signal is provided for application to external equipment for blanking purposes during test set transmissions.

B. Test Set Power Input Circuits

(1) The test set is capable of operating from three different power sources. The DME, Digital Bearing Unit, Signal Analyzer Unit, and Panel Unit all require 115 VAC, 400 Hz for operation. Application of this power to these major assemblies of the test set is controlled by the POWER switch S7401 on the Panel Unit. The external power sources from which the test set can be operated are:

1. 115 VAC, 60 Hz
2. 28 VDC
3. 115 VAC, 400 Hz

(2) The 115V ac, 60-Hz input power circuit is illustrated on figure 3. When the POWER switch S7401 is placed in the ON position, fan B7501 operates and +28V dc is generated by a rectifying circuit consisting of T7501, CR7501, and C7501. The 28V dc is applied to the static inverter that generates the 115V, 400 Hz for test set operation. The 115V ac, 60-Hz input line is protected by a 2.5 amp circuit breaker CR7501. The 28V d-c line is protected by 7.5 amp circuit breaker CB7503, and the 115 VAC, 400-Hz line is protected by 1 amp circuit breaker CB7502. The power input circuit configuration is determined by the selection of power cable 7124-2529-1 used when the power source available for test set operation is 115 VAC, 60 Hz.

(3) The 28V d-c input power circuit is illustrated on figure 4. POWER switch S7401 controls the application of 28V dc to the static inverter. The output circuit from the static inverter

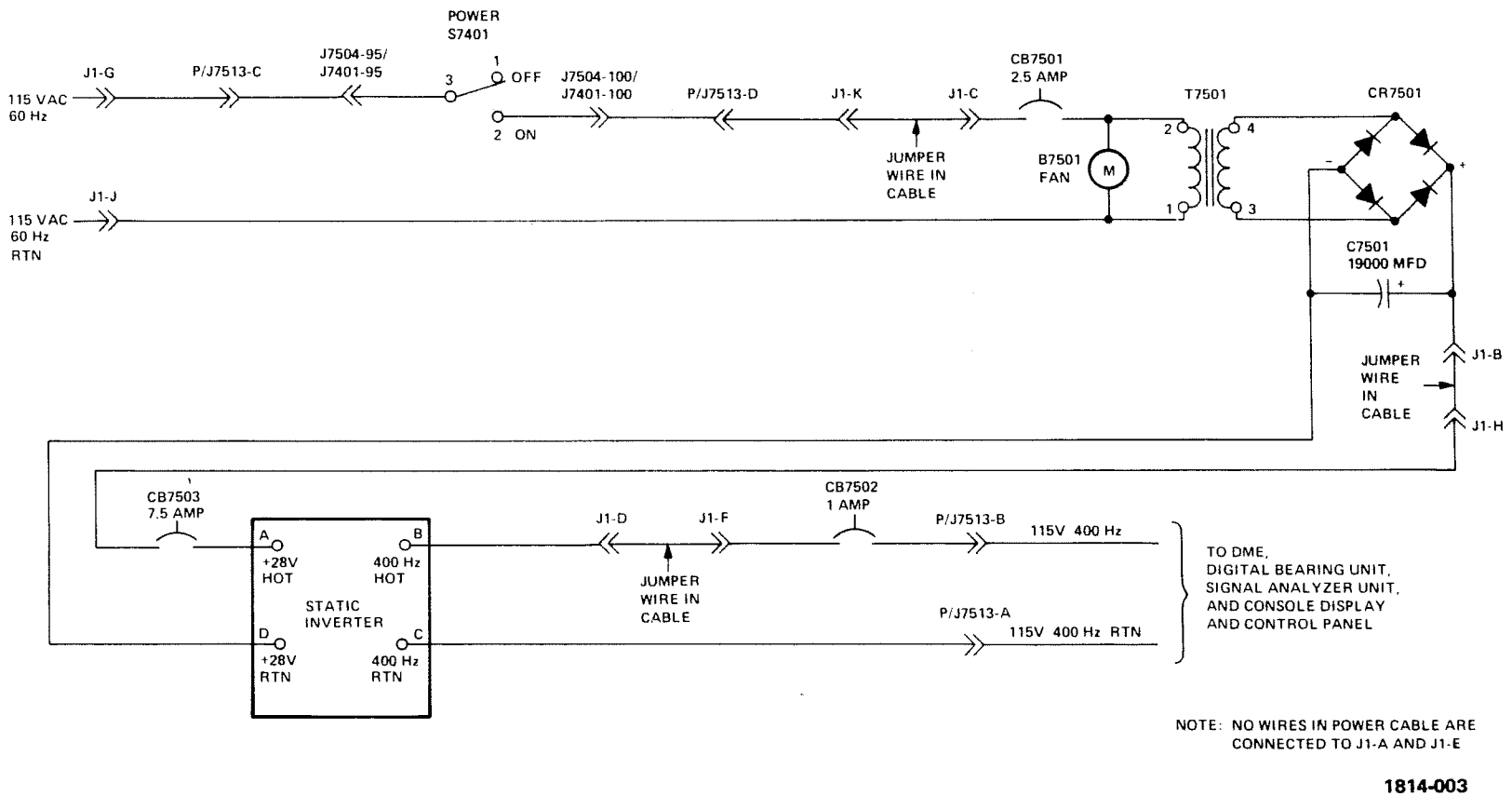


Figure 3. 115 VAC 60 Hz Power Input Circuit

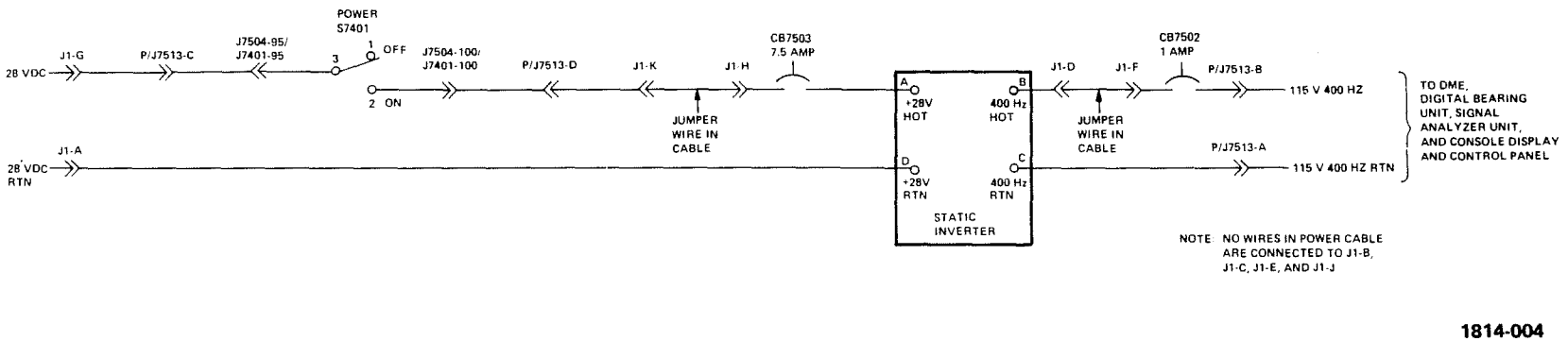


Figure 4. 28 VDC Power Input Circuit

to the test set major components is identical to that illustrated on figure 3. In this input power circuit configuration, the fan B7501 and rectifier circuit are not used. This power input circuit configuration is determined by the selection of power cable 7124-2529-3 used when the power source available for test set operation is 28V dc.

(4) The 115V ac, 400-Hz input power circuit is illustrated on figure 5. This input power is applied directly to the test set major components via circuit breaker CB7502 and POWER switch S7401. In this input power circuit configuration, the fan B7501, rectifier circuit, and static inverter are not used. This power input circuit configuration is determined by the selection of power cable 7124-2529-2 used when the power source available for test set operation is 115V ac, 400 Hz.

(5) If the test set is rack mounted, power cable 7124-2529-4 is connected directly to connector J7513 located on the Digital Bearing Unit mounting rack at the rear of the panel and chassis assembly. POWER switch S7401 controls the application of 115V ac, 400 Hz to the test set major components.

C. Digital Bearing Unit General Theory

(1) The Digital Bearing Unit uses signals and control functions generated by the DME to compute the bearing from the selected TACAN ground beacon (see figure 6). Additional control signals are provided to the Digital Bearing Unit from the Console Display and Control Panel (Panel Unit). The signals and control functions from the DME used by the Digital Bearing Unit are:

1. WIDEBAND SIGNAL
2. FERRIS DISCRIMINATOR
3. X or Y Mode (1 = Y Mode)
4. Suppressor Pulse (0 = SUPPRESS)
5. Channel Change (0 = MONITOR RESET)

(2) The signals and control functions from the Panel Unit used by the Digital Bearing Unit are:

1. Normal or 15-Hz only Bearing (1 = 15HZ ONLY)
2. Operate or Calibrate/Test (0 = CALIBRATE/0 = TEST)

3. Course Select Degrees (10 input lines providing the selected course information, for manual mode only)
4. OBS Control Manual or Automatic (1 = MANUAL)
5. TO-IN Signal

(3) The Digital Bearing Unit provides outputs to the Panel Unit, to the Signal Analyzer Unit, and to a recording device (not part of the test set). In addition, a DIGITAL TACAN AGC signal is provided to the DME, Signal Analyzer Unit, and AGC VOLTS meter when the TACAN AGC/DME AGC switch is in the TACAN AGC position. The signal outputs to the Panel Unit are:

1. Bearing Degrees Information (provided on 13 parallel lines)
2. To/From (1 = TO)
3. 0 = BEARING DASHES
4. Digital Bearing Unit Status (DIGITAL BEARING FAILURE)

(4) The signal outputs provided to the recording device are:

1. 15 HZ LEVEL
2. 135 HZ LEVEL
3. 0 = BEARING DASHES

(5) The signal outputs to the Signal Analyzer Unit are:

1. ANT. SPEED
2. Main Reference Group Clock (MRGCK)
3. Auxiliary Reference Group Clock (ARGCK)
4. ZERO ± 2° GATE
5. ±2° GATE
6. To/From (1 = TO)
7. 0.2° CLOCK BUFFERED
8. Digital Bearing Deviation Information (provided on 9 parallel lines)
9. Auxiliary Reference Group Events (ARGEV)

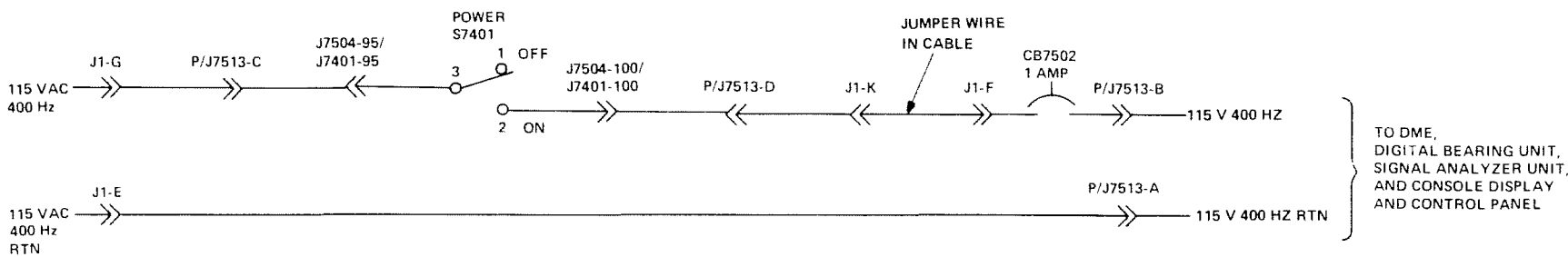


Figure 5. 115 VAC 400 Hz Power Input Circuit

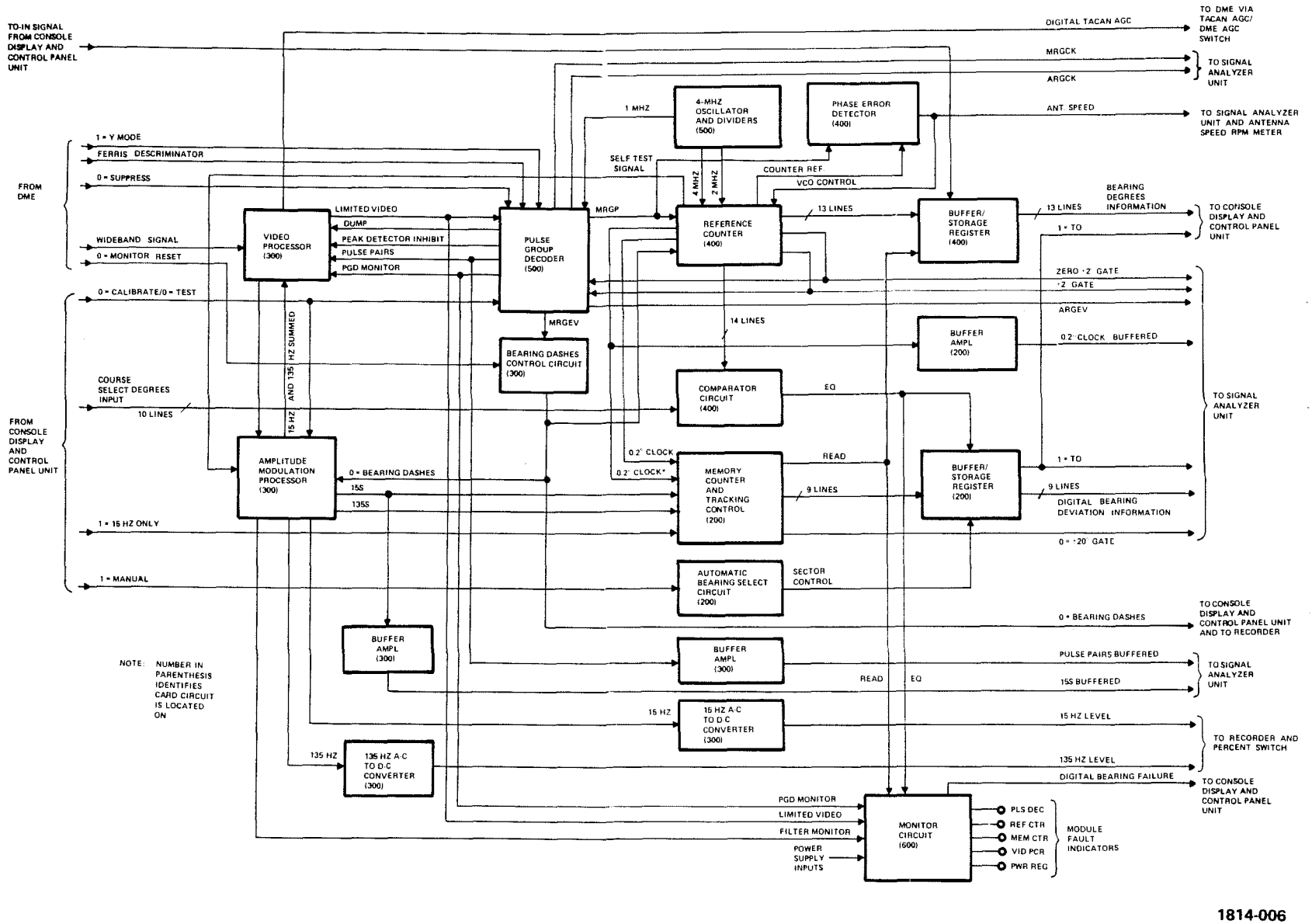


Figure 6. Digital Bearing Unit Block Diagram

10. 0 = ±20° GATE

11. PULSE PAIRS BUFFERED

12. 15S BUFFERED

(6) In general, the bearing of the test set from the selected TACAN ground beacon is derived from the phase relationship between the received main reference pulse groups (MRG's) and the amplitude-modulation components of the ground beacon signal. The amplitude-modulation components are generated by the rotating directional antenna of the ground beacon, and therefore have different phase relationships, with respect to the reference pulse transmissions, for different azimuth radials. In order to provide improved angular resolution and reduce errors due to multipath, a coarse-fine system approach is used (except in 15 Hz-only beacons). In this scheme, the fundamental (coarse) signal component (15-Hz amplitude-modulation component) is used to determine the bearing within a 40-degree sector, and the fine signal (135-Hz amplitude-modulation component) determines the precise bearing within the 40-degree sector. For 15-Hz only beacons, the BEARING switch on the Panel Unit is set to the 15 Hz ONLY position thus the 1 = 15 HZ ONLY input to the Digital Bearing Unit is at a logical 1 level and the memory counter, part of the bearing computer, operates in the 15-Hz only mode of operation.

(7) The Video Processor (see figure 6) accepts the WIDEBAND SIGNAL from the DME and amplifies it by a gain factor of 5. The base line is translated to a -5V level, and the nominal pulse height is 5 volts above the baseline, or zero volts. This signal is then sliced at the 50-percent amplitude point of each pulse in a voltage comparator. The resulting constant-width, constant-height pulses (LIMITED VIDEO signal) are supplied to the pulse group decoder for recognition of properly spaced pairs and triplets.

(8) The output of the linear video amplifier circuit in the video processor circuit drives a peak-riding detector circuit, that reconstructs the combined 15-Hz and 135-Hz amplitude-modulation envelope of the received signal. This circuit stores the peak-voltage of the first pulse in an intermediate storage. Upon verification of a valid pulse pair by the Pulse Group Decoder, the intermediate stored value is transferred to the final storage amplifier and the intermediate stored value is dumped. This sequence is a result of the PULSE

PAIRS, PEAK DETECTOR INHIBIT, and DUMP signal outputs of the Pulse Group Decoder. The resulting envelope signal is separated into its 15-Hz and 135-Hz components by two highly-stable, active bandpass filters in the amplitude-modulation processor circuit. The output of each filter is sliced at its zero-crossing points by a voltage comparator in order to supply logic-level signals (15S and 135S) to the memory counter. The comparator also provides enough return hysteresis to discriminate against component modulation percentages of less than 5 percent. The outputs of the filters (15 Hz and 135 Hz) are summed together, attenuated, and level translated to provide a 50 percent-of-peak amplitude reference to the LIMITED VIDEO comparator in the video processor circuit. A second summing network provides a FILTER MONITOR output signal to the monitor circuit for control of the VID PCR fault indicator.

(9) The 15-Hz and 135-Hz sine wave outputs of the respective filters are provided to a-c to d-c converters. The 15 HZ LEVEL and 135 HZ LEVEL output signals to the recorder are at a 10-volt level when the sine wave input is 4V peak-to-peak. The PULSE PAIRS output of the Pulse Group Decoder is applied via a buffer amplifier circuit (PULSE PAIRS BUFFERED) to the Signal Analyzer Unit.

(10) The envelope signal is supplied as the main error input of the AGC amplifier, which generates the necessary bias voltage to the i-f amplifier to force the average level of the envelope signal to zero volts. The frequency response characteristics of the AGC loop have been carefully designed to introduce no phase-shift into the 15- and 135-Hz amplitude-modulation components, and yet provide maximum agility to follow r-f signal strength variations. The PGD MONITOR signal provides a secondary error input to the AGC amplifier, which becomes significant only in the absence of a received beacon signal. This control loop limits the maximum receiver gain at an acceptable low video noise level. A third AGC error input is provided by summing in a very slight amount of LIMITED VIDEO to prevent AGC hangup in the event of a constantly saturated WIDEBAND SIGNAL. The AGC output is identified as DIGITAL TACAN AGC.

(11) The bearing dashes control circuit on the Video Signal Processor card includes circuitry to sense the percent of successful reference group decoding in order to make test set

lock-on decisions. When the test set is in the search condition, the 0 = BEARING DASHES signal inhibits the 15S signal to the memory counter and causes the BEARING DEGREES indicator on the Panel Unit to display dashes. The decoding of at least 67 percent of transmitted Main Reference Groups (MRG's) within a one-second averaging period causes the 0 = BEARING DASHES signal to change to a high level thus allowing the 15S signal to be applied to the memory counter. The aircraft-to-beacon bearing degrees will be displayed on the BEARING DEGREES indicator on the Panel Unit. After lock-on is achieved, the reduction of decoded MRG's below 33 percent within a one-second averaging period initiates the bearing memory period. If lock-on is not regained within the memory period (6 seconds), the test set will return to the search condition. The 0 = MONITOR RESET interface signal from the DME terminates the bearing memory period and resets the percent-of-MRG decoding circuit when a channel change is made. The 15S output is buffered and applied to the Signal Analyzer Unit.

(12) The Pulse Group Decoder accepts the LIMITED VIDEO signal from the video processor, combines it with the FERRIS DISCRIMINATOR information to suppress off-channel signals, and processes the pulse train to recognize validly spaced pulsed combinations. The selection of specific pulse spacings which are to be accepted is controlled by the X or Y mode signal (1 = Y MODE). The 0 = SUPPRESS signal is used to inhibit the decoder during the range-interrogate transmissions, or the receipt of suppression signals from any other equipment.

(13) Basically, the desired inter-pulse periods are recognized by correlation of the states of various stages of a shift register, which shifts the LIMITED VIDEO signal at 1-MHz clock rate. Validation of an X-mode pulse-pair, for example, occurs when the leading edge of the first pulse at the end of the shift register coincides with the presence of a second pulse 12 ± 1 μsec later, or in the 13th and 14th previous stages in the shift register. In addition, it is required that three successive stages in the register be simultaneous logical 1's to impose a minimum pulse width requirement on the incoming video. This requirement discriminates against narrow noise spikes. Successfully decoded pulse-pair events (PULSE PAIRS) are supplied to the video processor to enable updating of the envelope signal by the peak-riding circuit.

(14) To decode reference groups, pulse triplets are required having the appropriate characteristic spacings. For example, an X-mode MRG triplet would consist of a second pulse spaced 12±1 μsec from the first pulse, and simultaneously, a third pulse 30±1 μsec from the first pulse. In addition, the number of successfully decoded triplets is accumulated in a counter. When this counter reaches a count equal to half of the total possible pulse triplets in a main reference group, a narrow pulse (MRGP) is generated to indicate a successful decode. The counter is reset to zero count after each trial period to prevent false decodes due to noise. A pair of flip-flops are used to generate reference-group event occurrence information to be used by the video processor to make search/lock-on and ground beacon type decisions.

(15) Another counter on the Pulse Group Decoder card generates control signals for the peak-riding circuit on the video processor card. This counter starts at the occurrence of the first pulse and generates a gate (PEAK DETECTOR INHIBIT) beginning after the peak of the first pulse to prevent further charging of the peak detector by a possibly higher second-pulse peak. This counter also generates a gate which will coincide with the valid-pair decode pulse to enable the peak-level transfer (PULSE PAIRS) to the final envelope storage. This is followed by a dump gate (DUMP) to discharge the peak-detector intermediate storage in preparation for the next pulse-pair.

(16) The main reference group pulse (MRGP) output of the Pulse Group Decoder, signifying a successful decode of a MRG, is provided to the reference counter to phase the counter output with respect to the ground beacon MRG transmissions. A 4-MHz oscillator and a divide-by-two stage provides the 4-MHz and 2-MHz inputs required for reference counter operation. The reference counter provides 13 parallel output lines to the buffer/storage register. These 13 lines contain reference bearing information from 000.0 to 359.8 degrees, in 0.2-degree increments. The TO-IN signal from the Panel Unit, a ground level signal, is also provided to this buffer/storage register. This ground level signal allows the contents of the buffer/storage register to be sampled on the leading edge of the READ pulse occurring when the memory counter contains a count representing 180 degrees. The 0.2° CLOCK and 0.2° CLOCK* output signals of the reference counter are provided as trigger pulses to the memory counter. The 0.2° CLOCK*

signal is buffered and then applied to the Signal Analyzer Unit. The 15S and 135S outputs are provided to the memory counter. The memory counter contains the bearing degrees to the ground beacon; for example, if the test set is directly south of the beacon, the 15S and 135S signals phase-lock the memory counter operation so that the READ pulse samples the buffer/storage register contents when the reference counter outputs (13 lines) contain a count representing 180 degrees. (The MRGP, 15S, and 135S signals occur simultaneously when the test set is directly south of the beacon therefore the reference counter and the memory counter are set to the state representing 0 degrees simultaneously.) Since the READ pulse occurs 180 degrees later, the bearing degrees information provided to the Panel Unit causes the BEARING DEGREES indicator to indicate 180.0 degrees.

(17) The memory counter provides outputs containing bearing information to a second buffer/storage register. This register is sampled by a equal pulse (EQ) output from a comparator network. Fourteen outputs are provided from the reference counter to the comparator network. When the OBS CONTROL on the Panel Unit is set to the MAN position (normal operation), the 10 inputs from the COURSE SELECT DEGREES thumbwheel switches on the Panel Unit (containing bearing information for the course selected) are also applied to the comparator network. When the bearing angle in the reference counter equals the bearing angle of the course selected, the EQ pulses occurs. For example, if the course selected is 45 degrees, then the EQ pulse occurs when the reference counter provides a count equivalent to 45 degrees. If the test set is in an aircraft that is flying on the selected course, then the memory counter will contain a count representative of 0 degrees (on course) when the EQ pulse occurs. The digital bearing deviation output signals (9 outputs from the buffer/storage register) to the Signal Analyzer Unit will contain information indicative of 0.0 degrees deviation from the selected course. Deviation information to the Signal Analyzer Unit indicates course deviation from 0 to ±10 degrees in 0.2-degree increments during manual operation. When the system is operating in the manual mode, the automatic bearing select circuit controls the buffer/storage register circuit in such a manner that any course digital bearing deviation information within ±14 degrees of the selected heading to or from the ground beacon is provided in 0.2-degree increments.

(18) The 1 = TO output signal of the buffer/storage register is provided to the Signal Analyzer Unit and to the Panel Unit. In the automatic mode of operation, the 1 = MANUAL signal is at a logical 0 level. This signal level is obtained from the Panel Unit when the OBS CONTROL switch is in the AUTO position. The output of the automatic bearing select circuit causes the 1 = TO signal to be at a logical 0 level. A logical 0 level 1 = TO signal causes the FROM indicator on the Panel Unit to illuminate. In the manual mode of operation, the level of the 1 = TO signal depends upon the bearing angle information contained in the memory counter when the EQ pulse occurs. If the test set is in an aircraft and the aircraft bearing to the beacon is within ±90 degrees of the course selected by the COURSE SELECT DEGREES thumbwheel switches (OBS CONTROL in MAN position), the 1 = TO signal is a logical 1 and the TO indicator on the Panel Unit is illuminated. If the aircraft bearing from the beacon is within ±90 degrees of the selected course, the 1 = TO signal is a logical 0 and the FROM indicator on the Panel Unit is illuminated.

(19) The Pulse Group Decoder provides the MRGCK and ARGCK signals to the Signal Analyzer Unit whenever a main reference group and auxiliary reference group is decoded. When the FERRIS DISCRIMINATOR input to the Pulse Group Decoder is a logical 1, decoding operation is normal; however, if the FERRIS DISCRIMINATOR input changes to a logical 0 indicating an off-channel input pulse, the DUMP signal becomes a logical 1 thus discharging the peak-detector in the Video Processor. If the 0 = SUPPRESS input changes to a logical 0, the Pulse Group Decoder is prevented from operating.

(20) The ZERO ±2° GATE and ±2° GATE output signals of the reference counter are provided to the Signal Analyzer Unit and to the Pulse Group Decoder. These signals control the main reference group event (MRGEV) and auxiliary reference group event (ARGEV) outputs of the Pulse Group Decoder. The ARGEV signal occurs whenever an ARG event is decoded. The MRGEV signal is provided to the bearing dashes control circuit also referred to as beacon lock-on circuit.

(21) The memory counter provides the 0 = ±20° GATE signal to the Signal Analyzer Unit. This signal is a logical 0 approximately 40 degrees in duration centered around the 0-degree output of the memory counter.

(22) The antenna speed circuit receives two inputs from the reference counter. One of these signals is four degrees wide and the leading edge of the signal is coincident with the occurrence of the MRGP signal. The second signal is also four degrees wide and the leading edge occurs when the reference counter count represents 358 degrees. Both inputs occur at a 15-Hz rate. The antenna speed circuit checks for coincident of the two input signals and provides the ANT. SPEED output signal, a d-c level indicative of the antenna speed, to the Signal Analyzer Unit and to the ANTENNA SPEED RPM meter M7501. In addition, the ANT. SPEED signal is provided to the reference counter to control a voltage-controlled oscillator that, in turn, controls the clock rate to the reference counter.

(23) When the OPERATE/CALIBRATE switch on the Panel Unit is set to the CALIBRATE position, or the SELF TEST push-button/indicator is illuminated, the 0 = CALIBRATE/0 = TEST signal input to the Pulse Group Decoder and amplitude-modulation processor is a logical 0. The MRGEV and ARGEV outputs of the Pulse Group Decoder become logical 1's. Since the computed bearing is a function of the phase relationship between the memory counter and the reference counter, a given test bearing can be simulated by causing one loop to lock-up to the other when the calibrate or test function is activated. This scheme is effected by summing together the 15-Hz and 135-Hz square-wave outputs from the reference counter (SELF TEST SIGNAL), and introducing the simulated amplitude-modulated envelope into the input of the bandpass filters in the amplitude modulated processor. In order to simulate the sample-and-hold lag introduced by the peak-riding circuit, the summed square waves are processed by a low-pass RC network which introduces a two-degree lag at 15 Hz. The resulting waveform precisely simulates a bearing at 000 degrees when the BEARING switch in the Panel Unit is in the NORMAL position, and provides a precision signal to align the bandpass filters during system minimum performance tests. When the BEARING switch is in the 15 Hz ONLY position, the simulated bearing is 10 degrees.

(24) The Digital Bearing Unit also monitors (monitor circuit) various repetitive signals and supply voltages in the Digital Bearing Unit to ensure that circuits are operating. The precision analog reference voltages (±12Vdc) and 5 V d-c logic supply are monitored so that any voltages outside acceptable tolerances cause the PWR REG (power regulator) indicator to

illuminate. The summed outputs (15 Hz and 135 Hz) of the amplitude modulation processor filters (FILTER MONITOR) are monitored, and if the FILTER MONITOR d-c level deviates from zero, or the LIMITED VIDEO output of the video processor fails to exhibit at least 100 pulses per second, then the VID PCR (video processor) fault indicator illuminates. If the PGD MONITOR output of the Pulse Group Decoder fails to provide at least 100 pulses per second when the LIMITED VIDEO output of the video processor is nominal, then the PLS DEC (pulse group decoder) fault indicator illuminates. The monitor circuit also receives the EQ and READ output of the memory counter and comparator circuit respectively. If either signal fails to appear, then the REF CTR (reference counter) or MEM CTR (memory counter) indicator, respectively, illuminates. When any of the module failure indicators illuminate, the DIGITAL BEARING FAILURE signal becomes a logical 0 and the BEARING FAILURE indicator on the Panel Unit illuminates.

D. Digital Bearing Unit Detailed Theory

To accomplish the Digital Bearing Unit functions described in paragraphs C (1) through C (24), six printed-circuit cards are required. These cards are identified as the Digital Video Signal Processor, Pulse Group Decoder, Reference Counter, Memory Counter, Digital Bearing Unit Monitor, and Power Supply Regulator. Additional electrical parts are mounted on the main frame.

(1) Digital Video Signal Processor Card (300)

The functions performed by the Digital Video Signal Processor card are as follows:

1. Amplify and buffer the WIDEBAND SIGNAL (2nd detector output) from the DME receiver,

2. Generate a logic level signal (0 or +5 V) identified as LIMITED VIDEO. This signal is at a logical 1 level whenever the WIDEBAND SIGNAL exceeds 50% of the peak voltage for a given pulse,

3. Reconstruct the WIDEBAND SIGNAL amplitude-modulated envelope by successively storing the peak level of the first pulse of each valid pulse pair,

4. Separate and filter the 15-Hz and 135-Hz components of the amplitude-modulated signal,

5. Produce d-c level signals (15 HZ LEVEL and 135 HZ LEVEL) indicative of the a-c peak-to-peak amplitude output of the 15-Hz filter and 135-Hz filter,

6. Produce logic level signals (15S and 135S) that transition to a logical 1 level at the positive-going zero crossings of the 15-Hz and 135-Hz amplitude-modulated components,

7. Determine the percentage of decoded Main Reference Groups (MRG's) for operation of the memory counter circuits and the dash displays on the BEARING DEGREES indicator on the Panel Unit,

8. Generate a delay period after loss of signal to provide a bearing memory before displaying dashes on the BEARING DEGREES indicator of the Panel Unit, and allowing the memory counter to be re-phased with the zero-degree crossing of the 15-Hz amplitude-modulated components,

9. Provide a buffer output of the PULSE PAIRS signal,

10. Provide an automatic gain control (AGC) signal to the DME i-f amplifier for normalizing the WIDEBAND SIGNAL to a constant level over a large dynamic range (70 db) of input r-f signal strength.

(a) The WIDEBAND SIGNAL is applied to wideband video amplifier U314 (see figure 917). This amplifier multiplies the signal level by a factor of five and shifts the baseline to a level of -5 Vdc by the divider action of resistors R347 through R349. Resistors R350 and R351 and capacitors C324 and C325 provide power supply decoupling. Capacitor C323 provides amplifier stabilization and resistor U312D supplies an output quiescent current to eliminate amplifier cross-over distortion.

(b) High-speed voltage comparator U315 produces the LIMITED VIDEO signal. Resistors R355 and R343, in the output circuit of operational amplifiers U301A and U301B respectively, sum the 15-Hz and 135-Hz filter outputs to reconstruct the amplitude-modulated envelope.

Since these filter circuits introduce a phase reversal, their summed outputs are mixed with the video amplifier U314 output through resistor R352 such that the 50-percent points of the video pulses at the non-inverting input of comparator U315 are stabilized at a constant level. Resistors R353 and R354 derive this voltage level from the -12 V d-c supply to provide the reference input to comparator U315. Resistor U312F provides a pull-up load for the output of the comparator to establish the logical 1 level voltage.

(c) Hot carrier diodes CR303 and CR304, resistor U312C, and capacitor C320 form a peak-detector circuit that allows C320 to charge to the peak voltage of a pulse from the output of video amplifier U314. As the pulse decreases from its peak value, diode CR303 becomes reversed-biased thus allowing C320 to remain charged to the peak voltage. Since the second pulse of the pulse pair may have its amplitude corrupted by delay multipath reflections of the first pulses, the PEAK DETECTOR INHIBIT signal closes FET analog switch U309A just after receipt of the first pulse of the pulse pair. The negative voltage applied to the anodes of CR303 and CR304 via resistor R341 and U309A reverse biases CR303 and CR304 thus preventing any additional charging of capacitor C320 by the second pulse of the pulse group. The stored voltage across C320 is buffered by operational amplifier U310A, connected as a unity-gain voltage follower. If the stored pulse subsequently proves to be the first pulse of a validly-spaced pulse-pair, the PULSE PAIRS signal momentarily closes FET analog switch U309C to update the voltage across capacitors C315 and C316 to the new peak voltage appearing at the output of U310A. After the pulse validation trial period (34 microseconds), the DUMP signal momentarily closes analog FET switch U309B which discharges capacitor C320 through resistor U312B to the baseline voltage (-5 V dc), whether or not the stored pulse was validated. Thus, the peak-detector circuit is ready to process the next received pulse. As long as the test set is receiving ground beacon signals, the PULSE PAIRS signal will occur sufficiently often enough to maintain retriggerable monostable multivibrator U308B in its unstable state. This keeps FET switch U309D open. If no PULSE PAIRS signal occurs for three

milliseconds, the monostable multivibrator returns to its stable state, and its 0 output becomes high. In this condition, closed FET switch U309D clamps envelope-storage capacitor (C315 and C316) voltage to approximately -0.5 volts, as determined by U312A and R342.

(d) The amplitude-modulated envelope, or peak-riding voltage, across capacitor C315 and C316 is buffered by operational amplifier U310B, connected as a unit-gain voltage follower. When the test set is in the operate mode (0 = CALIBRATE/0 = TEST signal at a logical 1 level), one section of dual analog FET switch U307 connects the buffered envelope voltage output of U310B to the inputs of a pair of 2-pole active bandpass filters tuned to 15 Hz and 135 Hz. The 15-Hz filter, having a Q of 5, consists of operational amplifier U301A and frequency-determining components C301, C303, R304 through R306, and R318. The 135-Hz filter, having a Q of 10, consists of operational amplifier U301B and frequency-determining components C302, C306, R309 through R311, and R321. Variable resistors R304 and R310 provide fine tuning controls for the center frequencies of the 15-Hz and 135-Hz filters respectively. All frequency-determining components possess excellent thermal stability to preserve system accuracy over a wide range of ambient temperatures. Resistors R319 and R320 provide input current offset balancing for the two operational amplifiers, and C304 and C305 prevent extraneous signals from appearing at their reference (non-inverting) inputs. The 15-Hz filter attenuates the 135-Hz component by 97 percent. Therefore, a residual 3 percent 135-Hz component having a phase lag of 90 degrees is present at the output of the 15-Hz filter. Approximately 3 percent of the 135-Hz filter output having a phase lag of 90 degrees is coupled by C326 into the input of U303 effectively canceling the residual 135-Hz component from the 15-Hz filter. When the test set is in the calibrate or test mode (0 = CALIBRATE /0 = TEST signal is at a logical 0 level), analog FET switch U307 connects the inputs of the bandpass filters to the SELF TEST SIGNAL after it has been buffered by operational amplifier U305B connected as a unity-gain voltage follower. (The other pole of dual FET switch U307 is switched to ground in the calibrate/test mode to provide the signal called GROUND = TEST.)

This SELF TEST SIGNAL precisely simulates a 000-degree bearing (from the ground beacon) in the normal mode, or a 010-degree bearing in the 15-Hz only mode. In addition, the SELF TEST SIGNAL provides a calibration signal against which the bandpass filters can be precisely tuned. Resistors R307 and R308 sum the filter outputs to form the FILTER MONITOR signal which is processed by the Digital Bearing Unit Monitor card to detect filter circuit malfunctions.

(e) High-speed voltage comparator U303, in conjunction with resistors U302A, U302B, U302C, and R312, form a zero-crossing detector for the 15-Hz bandpass filter output. Resistor U302A supplies a pull-up load to establish the logical 1 level when the comparator output is high. Resistor R312 and resistor U302B provide positive feedback to introduce a return hysteresis. This hysteresis serves to effect a clean switching action when the comparator output changes state, and also prevents zero-crossing detection for 15-Hz component modulation of less than 5 percent. Since the bandpass filter inverts the phase of the input signal component, the zero-crossing detector is configured to produce a 0-to-1 transition when the input passes through zero volts in the negative-going direction. The reference (non-inverting) input of the comparator is at the required ground potential prior to this transition, since both the comparator output and the return of resistor U302B are at ground potential. Resistor U302C provides input-current offset balancing to the inverting input of the comparator. The 15-Hz sine wave output of the filter is applied to an a-c to d-c level converter circuit consisting basically of amplifiers U313A and U313B, and diode CR305. The output of U313A is rectified by diode CR305 and applied to U313B. Variable resistor R314 permits calibrating the d-c output voltage. The gain of this circuit is adjusted for a 5 V d-c output for a 2 V P-P a-c input corresponding to 15-Hz component modulation of 20 percent. Comparator U304, resistors U302D, U302E, U302F, and R313 form the zero-crossing detector for the 135-Hz bandpass filter output which operates in exactly the same manner as the 15-Hz zero-crossing detector. The 135-Hz sine wave output of the filter is applied to an a-c to d-c level converter circuit consisting basically of amplifiers U306A and U306B,

and rectifying diode CR301. Variable resistor R316 permits calibrating the d-c output voltage. The gain of this circuit is adjusted for a 5V d-c output for a 2V P-P a-c input corresponding to 135-Hz component modulation of 20 percent.

(f) Operational amplifier U305A, resistors U302G, R303, R302, R317, R326 and capacitor C311 comprise the bearing dashes control circuit (beacon lock-on decision circuit). The MRGEV signal is set to the logical 1 state through pull-up resistor U302G for nearly 1/15 second each time a MRG is successfully decoded. This signal is averaged by a low-pass filter consisting of R317 and C311 having a time constant of one second. Resistors R303, R302, and R326 form a positive feedback network which results in a hysteresis characteristic. The effect of this hysteresis is that an average of at least 67 percent decode success of transmitted MRG's is required to cause a lock-on decision; however, once in the lock-on condition, the test set will not unlock until the average percentage of decoded MRG's falls below 33 percent. This characteristic prevents the test set from exhibiting erratic behavior in very weak r-f signal regions.

(g) When a beacon lock-on decision is made, the output of U305A falls, which turns off transistor Q303 through R327 and R331 thus allowing the 0 = BEARING DASHES signal to change to a logical 1 level. The pull-up resistor for the logical 1 level is located in the Panel Unit. When the system reverts to the unlock condition, the output of U305A rises which triggers monostable one-shot U308A through C312. This causes the emitter of Q303 to be pulled up to a logical 1 level, thus preventing Q303 from being turned on for the 5-second duration of the one-shot. Capacitor C312 ensures that the input signal to U308A, pin 2 has returned to a logical 0 level before the 0 = MONITOR RESET returns to a logical 1 level. This prevents U308A from being prematurely triggered and removing the 0 = BEARING DASHES signal before a new bearing angle has been computed after a TACAN channel change has been accomplished. The bearing-memory period, determined by R334 and C314, may be altered by selecting a proportionately different value for R334. Transistor Q302 provides

current gain for the timing input of the monostable multivibrator, and R330 limits the timing input current for the stable condition. Should unlock occur due to a channel change or manual test, the 0 = MONITOR RESET signal will momentarily fall to a logical 0 and clear the memory period monostable U308A to allow for immediate acquisition of the new signal.

(h) Dual operational amplifier U311, resistors R335 through R340 and R346; capacitors C321, C319, and C322; and diode CR306 make up the AGC voltage amplifier. The open-loop gain-and phase-versus-frequency characteristics of this circuit are carefully controlled to provide virtually no quadrature phase component at 15 Hz or 135 Hz. These characteristics also cause the closed-loop AGC response to have a maximum agility in order to follow rapid r-f signal fading without signal breakup. The main input for the AGC amplifier is the peak-riding envelope signal at the output of U310B. This output is first processed by a low-pass section consisting of R335 and C321, having a breakpoint frequency of precisely 7.5 Hz. The output of this filter is buffered by U311B, connected as a non-inverting follower having a gain of approximately 8 as determined by R339 and R340. The output of U311B is then connected to the summing input of U311A through an input network consisting of R337, R336, and C319, which provides a second breakpoint at precisely 30 Hz. The effect of these two breakpoints is to produce an open-loop phase-lag of exactly 90 degrees at 15 Hz. The remaining 90 degrees of phase lag required to eliminate the quadrature component at 15 Hz is provided by feedback capacitor C322, which also establishes the open-loop gain at 15 Hz. This open-loop a-c gain at 15 Hz has been selected to provide a closed-loop damping factor of approximately 0.4.

(i) The PGD MONITOR signal is summed into the summing input of U311A to provide a noise AGC override to limit the receiver gain in the absence of a beacon signal. The envelope signal is switched to a -0.5V d-c level in the absence of valid pulse-pairs. This level is amplified to about -4 V dc in U311B, and provides an increasing-gain slew rate of 60 db per second in the absence of receiver output. However, when the

receiver gain increases to the point where thermal noise just begins to decode as valid pulse-pairs, sufficient average voltage of the PGD MONITOR is developed which, when summed through R346, cancels the current drain through R337 and R336 to the output of U311B. Diode CR306 prevents any input to the summing node when the PGD MONITOR is at a logical 0 level. This stabilizes the receiver sensitivity at a maximum level in the absence of a beacon signal. A small amount of the LIMITED VIDEO is also summed into the summing node of U311A through R359. This causes the AGC voltage to decrease receiver sensitivity in the event that LIMITED VIDEO is continuously in a logical 1 state.

(j) Resistor R338 provides a current drain from the summing node just equal to the average current contributions of R346 and R359 during normal beacon signal reception. DIGITAL TACAN AGC is applied to the DME, Signal Analyzer Unit, and AGC VOLTS meter when the TACAN AGC/DME AGC switch S7505 is in the TACAN AGC position. For normal test set operation, S7505 is set to the TACAN AGC position.

(2) Pulse Group Decoder Card (500)

The Pulse Group Decoder card consists entirely of digital circuitry with the exception of the 4-MHz crystal-controlled oscillator. The functions performed by the Pulse Group Decoder are as follows:

1. Decode validly-spaced pulse-pairs (X- or Y-Mode),

2. Manage the peak-detector circuitry by generating the PEAK DETECTOR INHIBIT and DUMP signals,

3. Decode the occurrence of Main and Auxiliary Reference Groups (MRG's and ARG's) for X- or Y-Mode,

4. Generate logic functions which indicate successful reference-group detection events, called the MRGEV and ARGEV signals,

5. Suppress off-channel signals to prevent false lock-on to them, or degradation of on-channel bearing information.

6. Provide the main reference group clock (MRGCK) signal to the Signal Analyzer Unit,

7. Provide the auxiliary reference group clock (ARGCK) signal to the Signal Analyzer Unit,

8. Provide the 2-MHz and 4-MHz signal to the Reference Counter card 400.

(a) The 4-MHz oscillator output of U522 is divided-by-four by dual flip-flop U523 (see figure 919). The output of U523B provides a 1-MHz clock signal to the shift register and peak-detector management counter.

(b) The LIMITED VIDEO signal, a train of rectangular pulses derived by thresholding each received video pulse at its half-amplitude level, is applied as the data input to U505A. This is the first stage of a 34-bit shift register comprised of U505 through U509. Integrated circuits U506 through U509 are 8-bit serial-in, parallel-out shift registers. The O = SUPPRESS signal from the DME will hold flip-flop U505A in a clear condition during DME transmissions, or transmissions of any other aircraft equipments supplying suppressor pulses to the DME. This will prevent processing any LIMITED VIDEO pulses that are known to have not been transmitted by the ground beacon. The clear input to U505B is supplied from the 0 output of flip-flop U516A, which is toggled to a low state whenever an off-channel pulse is received. This occurs because the output of NAND gate U520D is forced to a high state whenever the FERRIS DISCRIMINATOR signal input to this gate is a logical 0, as is the case for off-channel signals. This will prevent these pulses from propagating down the remainder of the shift register.

(c) NAND gate U513C and NOR gate U512C comprise a pulse-presence detector which will produce a 1-μsec positive pulse at the output of NOR gate U512C when the last stage of the shift register is at a logical 0 and the preceding two stages are logical 1's. Since TACAN beacon pulses are at least 3-μsec wide at their 50-percent amplitude points, this pulse-presence detector will discriminate against narrower noise spikes. NAND gate U501B and inverter U512D also form a pulse-

presence detector at a position 12 stages earlier in the shift register. For X-mode operation, 12- μsec spaced pulse-pairs will be detected by simultaneous output of both of the previously identified pulse-presence detectors. Since the shift register is being clocked asynchronously with respect to the input data (LIMITED VIDEO), the position of the leading edge of the second pulse in the shift register may have a plus-or-minus one-stage uncertainty with respect to the first pulse. Thus, the second pulse-presence detector requires only two logical 1's, 13 and 14 stages earlier than the leading logical 1 stage of the first pulse-presence detector, to produce an output.

(d) NAND gate 501A and NOR gate U502D form a pulse-presence detector located along the shift register so as to detect a second pulse spaced 15 μsec from the first pulse, the spacing used for Y-mode ARG's. This pulse-presence detector, and those for 24- and 30- μsec pulse spacings, are different from the 12- μsec detector in that the NOR gate requires a logical 0 in the third shift register stage downstream from the stage with the leading logical 1 in order to provide a positive output pulse. The two intervening shift register stages are not sensed because of the plus-or-minus one stage leading-edge uncertainty. This configuration is not used for the 12- μsec pulse-presence detector since strong-signal saturation could obscure the leading edge of a second pulse spaced by only 12 μsec. NAND gate U501C and NOR gate U502B detect pulses spaced 24 μsec from the first pulse (X-mode ARG's) and NAND gate U501D and NOR gate U502A detect pulses spaced 30 μsec from the first pulse (X-mode MRG's, and Y-mode pulse-pairs, MRG's, and ARG's). NOR gate U502C is used to detect the absence of a pulse 15 μsec from the first pulse for the purpose of discriminating between Y-mode MRG's and ARG's. (Y-mode ARG's also contain sufficient 30- μsec pulse-pairs to decode as MRG's if this absence-of-pulse condition were not imposed.)

(e) The pulse-pair decoder, AND gate U504D, detects a two-pulse coincidence, with the first-pulse input coming from NOR gate U512C and the second-pulse input coming from one section of data-selector U503. For X-mode,

the data-selector is switched to the 12- μsec pulse-presence detector, and for Y-mode, the data-selector is switched to the 30- μsec pulse-presence detector. The pulse-pair coincidence signal at the output of U504D is further functionally ANDed with decoded outputs from the peak-detector management counter through gates U520A and U512A. This step is necessary to insure that the final PULSE PAIRS output corresponds to a particular input pulse-pair, the first-pulse amplitude of which is being stored in the peak-detector circuit.

(f) The peak-detector management circuit consists of dual flip-flops U516 and U519, decade counter U518, NAND gates U513A, U517, U520D, inverter U514A, and AND gate U504C. Starting from the "ready" condition, the counter, consisting of dual flip-flop U519 wired as a pair of divide-by-two counters, and decade counter U518, is in count-of-36 state (100100). This count produces a logical 0 at the output of NAND gate U517D. This logical 0 clears flip-flop U516B and also prevents the 1-MHz clock signal from advancing the counter by disabling AND gate U504C. When a LIMITED VIDEO pulse appears at the input of the shift register, flip-flop U505A will transition to a logical 1 on the rising edge of the next 1-MHz clock pulse. Immediately after this occurs, all three inputs of NAND gate U513A are high since the 0 output of the second stage of the shift register U505B is still a logical 1, and the 0 output of flip-flop U516B is a logical 1. This causes the output of U513A to be a logical 0 which sets flip-flop U519B and clears flip-flop U519A. At the same time, the logical 1 output of inverter U514A resets the stages of decade counter U518 to the all-zero state. This, in turn, causes the output of NAND gate U517D to rise thus releasing the clear hold to flip-flop U516B and enabling AND gate U504C. It also causes the output of NAND gate U517C to drop, disabling NAND gate U517B thus releasing the clear hold on flip-flop U516A. On the next clock pulse, the second stage of the shift register (U505B) is set. The resulting logical 0 from the 0 output of U505B inhibits NAND gate U513A thus releasing the set, clear, and reset inputs to U519B, U519A, and U518, respectively. With the clock input to the counter (T of U519B) now running, the counter advances at a rate of one count per microsecond. When the

counter transitions to a count of two (000010), the 1 output of flip-flop U519A rises and clocks flip-flip U516A. If, at this time, the FERRIS DISCRIMINATOR input to NAND gate U520D is low, indicating an off-channel input pulse, the output of U520D is a logical 1, and flip-flop U516A is clocked to the set state. This raises the DUMP line to discharge the peak-detector (on the Digital Video Signal Processor card), and enables the reset-to-nine gate of decade-counter U518. At the same time, the 0 output of U516A becomes a logical 0. This logical 0 clears the second stage of the shift register (U505B) and prevents the off-channel pulse from propagating down the remainder of the shift register. When the counter advances to a count of four (000100), output A of U518 rises, producing a logical 1 at the other input of the reset-to-nine gate. Resetting U518 to nine causes both inputs of NAND gate U517D to be logical 1's. The resulting logical 0 output of U517D turns off the counter clock by disabling AND gate U504C. At this time, the logical 0 output of U517D also assures that the outputs of both NAND gates U517A and U517C are logical 1's. Since both inputs of NAND gate U517B are now logical 1's, the resulting logical 0 output of U517B clears flip-flop U516A and the DUMP signal becomes a logical 0.

(g) Conversely, if the FERRIS DISCRIMINATOR signal is high when the counter transitions to a count of two, indicating an on-channel input pulse, both inputs of NAND gate U520D are logical 1's. (A logical 1 output of NAND gate U517A is assured by a logical 0 at the D output of U518.) The resulting logical 0 output of U520D causes flip-flop U516A to remain in the clear state at this time. In this case, when the counter transitions to a count of four, the rising of the A output of U518 toggles flip-flop U516B to the set state (its data input is tied to the +5 Vdc supply), causing the PEAK DETECTOR INHIBIT signal to become a logical 1. At the same time, the 0 output of U516B disables NAND gate U513A to prevent any further counter resets for the remainder of the count-cycle, and also causes the output of NAND gate U517C to rise. Since the D output of U518 is a logical 0 at this time, the output of NAND gate U517A is a logical 1. Thus, both inputs of NAND gate U517B are logical 1's and the resulting logical 0

output holds flip-flop U516A in the clear state. This is done so that a subsequent off-channel input pulse will not abort the decode-attempt of the original on-channel input pulse.

(h) The next significant event which occurs in the count-cycle is the sensing of counts 32 through 35 by NAND gate U517A. On count 32 (100000), the D output of U518 becomes a logical 1 which raises one input of U517A. The other input, connected to the output of NAND gate U517D, is also a logical 1, since the output A of U518 is a logical 0 at this time. The logical 0 output of U517A during these counts enables NOR gate U512A to pass the pulse-pair coincidence pulse which occurs at precisely this time for a valid pulse-pair. The logical 0 output of U517A also raises the outputof U520D and U517B to prepare flip-flop U516A for a dump cycle. When the counter transitions to count 34 (100010), the 1 output of flip-flop U519A will rise and toggle U516A to the set state, causing the DUMP signal to become a logical 1. The logical 0 from the 0 output of U516A disables NAND gate U520A from passing any subsequent pulse-pair coincidence pulses from U504D for this cycle. When the counter finally advances to count 36 (100100), the A and D outputs of U518 both become logical 1's. The resulting logical 0 from U517D inhibits the 1-MHz clock gate U504C and clears both flip-flops U516 thereby resetting the PEAK DETECTOR INHIBIT and DUMP signals to a logical 0 level. The DUMP clearing operation is obtained since the logical 0 output of U517D causes the outputs of NAND gates U517A and U517C to be logical 1's. These two logical 1's cause the output of NAND gate U517B to be a logical 0 thus clearing flip-flop U516A. Finally, the logical 1 from the 0 output of U516B is applied to NAND gate U513A, thereby returning the peak-detector management circuit to the initial condition, and ready to process the next LIMITED VIDEO pulse.

(i) Reference group decoding is accomplished by sensing the occurrence of specifically-spaced groups of three LIMITED VIDEO pulses (or two pulses and the absence of a third pulse, in the case of Y-mode MRG's). If the number of such pulse-triplets detected within a trial period is at least five, a reference-group detection

event has occurred. The trial periods for MRG and ARG decoding are determined by dual retriggerable monostable U521. In both cases, the leading edge of a three-pulse coincidence pulse (outputs of U504A and U504B, respectively) triggers the appropriate monostable, the 0 output of which releases the reset-to-zero input of the respective counter (U511 or U510). The periods of the monostable, determined by R505-C502 and R506-C503, are such that three successive pulse-triplet decode failures will abort a reference group decode attempt. Being retriggerable, the monostable periods are restarted by each successful pulse-triplet decode. Main reference group pulse-triplets are detected by AND gate U504A. For X-mode, this gate detects coincidence of a 12- μsec pulse-pair, as indicated by a logical 1 output from AND gate U504D, and a pulse 30 μsec later than the first pulse, as indicated by a logical 1 output from NOR gate U502A. The latter output is switched to the input of U504A by data-selector U503 when in X-mode operation. For Y-mode MRG detection, the output of AND gate U504D, which indicates 30- μsec pulse-pair detection, is ANDed with the output of U502C, as selected by data-selector U503. A logical 1 output from U502C indicates the absence of a pulse 15 μsec later than the first pulse. (For Y-mode ARG's, a 15- μsec pulse would be present.) The MRG three-pulse coincidence output of AND gate U504A provides the clock input to four-bit binary counter U511. For counts zero through three, the C output of U511 is a logical 0 thus disabling NAND gate U513B. When the counter advances to a count of four (0100), NAND gate U513B is enabled. Since the 1 output of flip-flop U515B is initially high (to be explained below) the next clock (pulse-triplet) pulse produces a 1- μsec logical 0 output of U513B. This becomes a positive pulse output on the MRGP line, after being inverted by U514C. Also, when the counter reaches a count of four (0100), the output of NOR gate U512B drops producing a logical 0 on the data (D) input to flip-flop U515B. Thus, when the counter transitions to a count of five (0101), the rising of the A output of U511 toggles U515B to the clear state (a logical 0 on the 1 output). The clear input of U515B is then a logical 0 which causes this flip-flop to be held in the clear state regardless of subsequent data and toggle input signals. Once in the clear state, this

flip-flop can be set only by applying a logical 0 to its set input. A logical 0 at the 1 output of U515B inhibits NAND gate U513B to prevent more than one MRGP pulse from being generated during a single group. The 0 = CALIBRATE/0=TEST signal allows NAND gate U520C to act as an inverter in the normal test set operating mode. Thus, the logical 0 occurring on the 1 output of U515B, upon successful MRG decoding, results in a logical 1 MRGEV signal. The 1 output of U515B is returned to the logical 1 state (resulting in a logical 0 MRGEV) by the action of the ZERO ±2° GATE input signal. This signal is generated by the reference phase-locked loop counter just prior to the next anticipated MRG reception, and toggles monostable multivibrator U524A. The resulting short logical 0 pulse from the 0 output of U524A unlocks (sets) flip-flop U515B, returning it to the ready state (1 output at a logical 1 level).

(j) Auxiliary reference group pulse-triplets are detected by AND gate U504B. For X-mode, the gate detects coincidence of a 12- μsec pulse-pair, as indicated by a logical 1 output from AND gate U504D and of a pulse 24 μsec later than the first pulse, as indicated by a logical 1 output from NOR gate U502B. This output is switched to the input of U504B by data-selector U503 when in X-mode operation. For Y-mode ARG detection, the output of AND gate U504D indicates 30- μsec pulse-pair detection. This event is then ANDed with the output of NOR gate U502D, as selected by data-selector U503. A logical 1 output from U502D indicates the presence of a pulse 15 microseconds later than the first pulse. The three-pulse coincidence output of AND gate U504B provides the clock input to four-bit binary counter U510. As in the MRG counter circuit, when this counter reaches a count of four, the output of NOR gate U514D drops, enabling flip-flop U515A to be toggled on the fifth count. Flip-flop U515A is returned to its ready state by the action of the ±2° GATE input signal and monostable multivibrator U524B. The ARGEV output signal is supplied by NAND gate U520B, acting as an inverter when the 0 = CALIBRATE/0= TEST signal is a logical 1. When the test set is placed in the self-test mode, 0 = CALIBRATE/0 = TEST is a logical 0, and the outputs of both NAND gates U520B and U520C

are forced to a logical 1 level. This is done to simulate the successful reference group decoding to allow the test set to come out of the search condition.

(k) The 4-MHz output of U522 is inverted by U514B and applied to pin 12 of the card connector. The 2-MHz signal on the 0 output of U523A is applied to pin 11. These card outputs are applied to the Reference Counter card 400. The MRGCK and ARGCK output signals on pins 13 and 14, respectively, are applied to the Signal Analyzer Unit.

(3) Reference Counter Card (400)

The purpose of the Reference Counter is to synthesize a local bearing angle reference which is accurately phase-locked to the main reference groups of the received TACAN signal. The synthesized bearing angle reference is subdivided into very fine angular increments. The Reference Counter card also contains a digital buffer for storing the computed bearing angle, and a digital comparator to sense the point in the count cycle when the reference bearing angle is equal to the manually selectable bearing angle input obtained from the COURSE SELECT DEGREES control on the Panel Unit.

(a) The bearing angle reference circuit consists basically of a main counter and associated trigger controlling circuit, and decoder gates (see figure 918). The trigger for the main counter is controlled by a circuit consisting of a voltage-controlled oscillator (VCO) U401, flip-flops U409A and U409B, and NAND gates U408A and U408D. The 4-MHz input is applied to NAND gate U408A and the 2-MHz input is applied to the trigger input of flip-flop U409B and to NAND gate U408D. The VCO U401 output has a center frequency of 160 kHz and a range of ±24 kHz for a 2.5-volt input variation. Each positive-going edge of the output of U401 triggers flip-flop U409A to the set state. The next positive-going edge of the 2-MHz signal sets flip-flop U409B and the resulting logical 0 from the 0 output clears flip-flop U409A. One 2 MHz-clock period later, flip-flop U409B is cleared. Therefore, for each positive-going output of U401, a 0.5- μsec logical 0 output of flip-flop U409B is applied to NAND gate U408D. This 0.5- μsec logical 0 is "OR"ed in U408D with the 2-MHz squarewave so as

to override one low state between two successive 0.5-μsec positive pulses. This output signal of U408D is then strobed with the 4-MHz squarewave input in U408A to produce a train of pulses having an average rate of 2.16 ±0.024 MHz.

(b) This signal frequency is divided by 16 by 4-stage binary counter U407. The output of U407 is further divided by five by the last three stages of decade divider U412. In this manner, the center frequency has been reduced by a factor of 80 to 27 kHz, which is the rate of occurrence of 0.2-degree increments of the TACAN signal (15 Hz x 360° x 5). The 0.2° CLOCK signal, at pin 11 of U412, drives a second divide-by-five circuit consisting of the last three stages of decade divider U413. The 1-degree output on pin 11 of U413 is divided by two by the first stage of U414 to produce a 2-degree output on pin 12 of U414. The 2-degree output is further divided by five in the last 3 stages of U414. The 10-degree output on pin 11 of U414 is divided by 10 in decade divider U415. The 100-degree output of U415 is divided by two by the first stage of U413 to produce the 200-degree output. A 20-degree output appears on pin 12 of U415. The 200-degree output on pin 12 of U413 is divided by two by the first stage of U412.

(c) The .2B, .4C, and .8D outputs of U413 of the main counter produce a count equivalent to tenths of a degree in 0.2-tenths increment. The 1A, 2B, 4C, and 8D outputs of U414 produce a count equivalent to degree increments from 0 to 9. Outputs 10A, 20B, 40C, and 80D from U415 produce a count equivalent to tens of degrees from 0 to 9, and the 100 and 200 outputs of U413 and U414 produce a count equivalent to 100 degrees from 0 to 3. Thus, U412 through U415 comprise a binary coded decimal (BCD) counter which continuously counts from 000.0 to 359.8 degrees in 0.2-degree increments with 15 complete count cycles per second.

(d) A decoder circuit consisting of exclusive OR gates U410A and U410B, NAND gates U405A and U405B, NOR gates U406A and U406B, and flip-flops U404A and U404B provides the signal required for resetting the counter to zero when a count representative of 360 degrees is decoded. In addition, this decoder circuit recognizes and

produces a ZERO ±2° GATE signal, a ±2° GATE signal, and a SELF TEST SIGNAL. Except for a period between 358 and 2 degrees (ZERO ±2° GATE), flip-flop U404A is in the clear state. The operation consists of digitally synchronizing the reference counter to the received, decoded main reference groups (MRG's). A 1- μsec positive pulse (MRGP), generated by the successful decoding of a MRG, resets the counter to a 359.8-degree count when the 0 = BEARING DASHES signal is a logical 0 (search mode) and the output of inverter U422C is a logical 1. Digital resets of the counter are inhibited when the 0 = BEARING DASHES signal is a logical 1 (track mode) and the output of U422C is a logical 0. The logical 0 output of U422C disables the reset-to-9 inputs of the counter. Thus, further digital resets of the reference counter are prevented to allow the VCO phase-locking action to take over. The next trigger to the counter changes it to the 000.0 degree count (all zeros in the counter).

(e) Exclusive OR gate U410B produces a squarewave with a period equivalent to 4 degrees (approximately 740 μsec) and the positive-going transition occurring at 2, 6, 10, 14, 18, 22, and every 4 degrees thereafter. Exclusive OR gate U410A produces a squarewave with a period equivalent to 40 degrees (approximately 7.4 milliseconds) and the negative-going transition occurring at 40, 80, 120 degrees, etc. The output of U410A is NANDed with the outputs from pin 8 of U414 and 10A output from U415 pin 12 in NAND gate U405B to produce a 4-degree logical 0 output occurring at 38 degrees and every 40-degree increment thereafter. The output of NAND gate U405A becomes a logical 0 at a count equivalent to 340 degrees and remains at a logical 0 level until the counter is reset. The logical 0 outputs of NAND gates U405A and U405B are NORed in gate U406A to produce a logical 1 on the data (D) input of flip-flop U404A from counts equivalent to 354 to 358 degrees. The positive-going transition from exclusive OR gate U410B occurring at 358-degree count sets flip-flop U404A. The logical 0 from the 0 output is applied to NOR gate U406B. The remaining input to NOR gate U406B is a logical 1 from a 350 to 360-degree count; therefore, the output of NOR gate U406B remains at a logical 0 level. At the 360-degree count, the input

on pin 6 of NOR gate U406B becomes a logical 0 and the output of U406B becomes a momentary logical 1. The main counter is reset to the all 0 state (000.0 degrees). Since U414 is already in the all 0 state, resetting of this decade divider is not required and its "reset-to-0" input is grounded. When the counter is reset to the all 0 state by the output of NOR gate U406B, the resulting 0 from pin 12 (100 signal) of U413 is applied to the "reset-to-0" input of U413 thus the reset hold is removed. The 0.2° CLOCK output of U412, pin 11 triggers U413, and the output of pin 11 of U413 triggers U414. In this manner, the 2-degree count is reached even though U415 is still held in the reset state. Flip-flop U404A is triggered to the clear state at the 2-degree count. The logical 1 from the 0 output of U404A causes the output of NOR gate U406B to return to a logical 0 thus the main counter is allowed to continue the complete new cycle. The signal on 1 output of flip-flop U404A is identified as ZERO ±2° GATE.

(f) The output of NAND gate U405B is provided to the data (D) input of flip-flop U404B. The output of U410B is the trigger input to this flip-flop. The 0 output from this flip-flop is identified as the ±2° GATE. This signal is a logical 1 having a period equivalent to 4 degrees with the 0-to-1 transition occurring at 38 degrees and every 40 degrees thereafter.

(g) The output of exclusive OR gate U410A is applied to resistor R408. The output from pin 12 of U412 is applied to resistor R407. The signal at the junction of R407 and R408 is identified as the SELF TEST SIGNAL. This signal is essentially a squarewave with a period equivalent to 40 degrees superimposed on a squarewave with a period equivalent to 360 degrees. Thus, this signal contains 15 Hz and 135 Hz components with precisely known phase relationships to simulate the amplitude modulation components of a test bearing angle of 0 degrees. The combination of R407, R408, and C406 provide exactly the same phase lag that is introduced by the sample-and-hold action of the modulation envelope detector.

(h) The output signals from the reference counter (identified in paragraph 2D(3)(c)) are applied to the inputs of a 13-bit buffer/storage register comprised of U418, U420, and flip-flop U411B. When the READ input signal transitions (from a 0 to 1 when the TO-IN signal is a logical 0, or from a 1 to 0 when the TO-IN signal is a logical 1), the resulting logical 1 from U410D loads data into the buffer/storage register. The outputs of this register are the computed bearing angle in parallel BCD format. The output signals of this counter are also applied to a comparison network comprised of exlusive NOR gates U417, U419, and U421. The ten signal outputs of the COURSE SELECT DEGREES control on the Panel Unit are applied to the comparison network. The T1A, T2B, T4C, and T8D input signals contain information for the unit position for the selected course in BCD form. Signals T10A, T20B, T40C, and T80D contain the information for the tens position in BCD form, and signals T100 and T200 contain the information for the hundreds position. This course select information is from 000 to 359 degrees. NAND gate U408B couples a clock pulse through whenever the .2B output of U413 is a logical 0. This clock pulse is approximately 8 microseconds in duration. When the reference counter bearing angle is equal to the selected angle, and the .4C and .8D outputs are both at a logical 0 level, the 8-microsecond (approximately) EQ (equal) output pulse occurs. The EQ pulse is applied to the Memory Count card.

(i) A counter one-shot circuit is used in conjunction with U403, a TTL-to-high level interface module, and operational amplifier U402. The 1-microsecond MRGP pulse resets decade counter U416 to the all 0 state when the 0 = BEARING DASHES signal is a logical 1 (tracking mode). The 0.2° CLOCK signal triggers the decade counter. The output of the decade counter is applied to the trigger input of flip-flop U411A. At receipt of the MRGP, the output of NAND gate U405C becomes a logical 1 and remains at this level for approximately 740 microseconds (4 degrees). Assuming that flip-flop U411A is initially in the set state, the data (D) input is at a logical 0 level when the count of 9 is reached in the decade counter. The positive-going transition on pin 11 of U416 clears flip-flop U411A. The decade counter must be incremented through its complete cycle

(10 more 0.2-degree clock pulses) until a second count of 9 is reached and flip-flop U411A is set. At this time, the output of NAND gate U405C becomes a logical 0. This logical 0 is coupled through and inverted by U406D, and applied to the "reset-to-9" input when the MRGP input to U406D is a logical 0. Decade counter is held at the count of 9 until the next MRGP pulse occurs at which time the cycle repeats.

(j) The ZERO ±2° GATE signal from flip-flop U404A is NORed with the 200 output (pin 12) of U412 in U406C. The output of U406C is a logical 1 from 2 degrees to 200 degrees and a logical 0 from 200 degrees to 2 degrees. This signal is applied to pin 6 of U403, and its inverse is applied to pin 2 of U403. Integrated circuits U403 and U402 form a time-to-voltage converter. The two signals from U406C and U422A are compared against the occurrence of the 4-degree output pulse of NAND gate U405C to produce the ANT. SPEED output signal of U402. The output of U403 is a bi-polar signal with the ratio of the positive and negative outputs of U403 depending upon an early or late occurrence of the output of NAND gate U405C with respect to the outputs of U406C and U422A. When the ground beacon antenna speed is 900 rpm (15 Hz rate), the ANT. SPEED output signal is 0 volts and the VCO U401 output remains at 160 kHz. When the ground beacon antenna speed exceeds 900 rpm, then the output of NAND gate U405C occurs before the outputs of U406C and U422A, the ANT. SPEED signal increases from 0 to a positive voltage, and the output of the VCO U401 increases in frequency. This feedback VCO loop causes the reference counter to speed up to keep the outputs of U406C and U422A in step with the output of NAND gate U405C. Conversely, if the ground beacon antenna speed is less than 900 rpm, the output of NAND gate U405C occurs after the outputs of U406C and U422A, the ANT. SPEED signal increases from 0 to a negative voltage, the VCO output slows down, and the reference counter outputs slow down. An increase or decrease of ground beacon antenna speed equal to ±1.8 rpm causes a voltage output of U402 of +1.8 V (for a +1.8 rpm increase) or -1.8 V (for a -1.8 rpm decrease). The ANT. SPEED signal is applied to the Signal Analyzer Unit and to the ANTENNA SPEED RPM meter M7501.

(k) The 0.2° CLOCK output signal is obtained from pin 11 of U412. The 0.2° CLOCK* output signal is obtained from inverter U422B. The output of U412 pin 9 is applied to NAND gate U408C. The output of U412 pin 8 is inverted by U422E and applied to NAND gate U408C. Although both of these output signals (0.2° CLOCK and 0.2° CLOCK*) are at a 27-kHz rate (period equivalent to 0.2 degrees of antenna rotation at 15 Hz), the phase is such that the clock pulses of the 0.2 CLOCK signal occur approximately seven microseconds after the clock pulses of the 0.2 CLOCK* signal.

(l) Diode CR401 and capacitor C403 comprise a half-wave rectifier circuit to supply a nominal +28V dc to pin 3 of U401.

(4) Memory Counter Card (200)

The purpose of the Memory Counter card is to store the computed bearing angle as the phase angle difference between the reference and memory counters, and to provide a means for incrementing this phase angle either positively or negatively to track a changing bearing angle. Also included is circuitry for setting the memory counter in the proper 40-degree sector, and monitoring the coarse bearing information to eliminate 40-degree lock-on errors.

(a) The memory counter consists fundamentally of decade counters U216 and U217, and divide-by-12 counters U218 and U219 (see figure 916). The counting sequence begins with a clock pulse having a period equivalent to 0.2 degrees of antenna rotation at a 15-Hz rate. The 0.2° CLOCK* signal from the Reference Counter card is applied to NAND gate U208A. This gate is enabled by a logical 1 from the 0 output of flip-flop U206B. NAND gate U208D is inhibited by a logical 0 from the 1 output of flip-flop U204B. The input on pin 1 of exclusive OR gate U214A is a logical 0. The 0.2° CLOCK* signal is therefore coupled through and inverted by NAND gate U208A, and coupled through and inverted by gate U214A. A 0.2-degree clock is applied to the divide-by-5 input of U216 (pin 1), the D output of which becomes a 1-degree clock. Decade counter U217 is triggered by the 1-degree clock and produces a 2-degree clock output on pin 12 of U217. This 2-degree clock is

applied to the divide-by-5 input of U217 (pin 1), and the D output on pin 11 is a 10-degree clock. The 10-degree clock signal is divide-by-6 in U218 to produce a 60-degree clock signal on pin 9 (C output). Divider U219 is triggered, at the divide-by-3 input, by the 60-degree clock and produces a 180-degree and 360-degree output. The counter automatically recycles to the all zero state.

(b) Additional gates and flip-flops are provided to generate the 0 = ±20° GATE and READ output signals, and provide additional control signals to the memory counter. NOR gate U210D combines the M1A and M2B signals of U217 to produce a string of 1-degree logical 1 pulses with the trailing edges occurring at 1 degree and every 10 degrees thereafter, at 5 degrees and every 10 degrees thereafter, and at 9 degrees and every 10 degrees thereafter; i.e., 1, 5, 9, 11, 15, 19, etc. These time intervals are referenced to the all zero state of the memory counter. The M4C output of U217, M.8D output of U216, and the pulse train output of NOR gate U210D are applied to NAND gate U211B. The output of NAND gate U211B consists of 0.2-degree logical 0 pulses with the trailing edges occurring at 5 degrees and every 10-degree increments (with respect to the all zero state of the memory counter) thereafter. The output of NAND gate U211B is applied to the trigger input circuits of flip-flops U212B and U213A.

NOTE: Unless otherwise specified, all times (described in degree increments) for the memory counter are referenced to the all zero state of the memory counter.

(c) The M10 output of U218 is applied to inverter U207B. The output of U207B is applied as an enabling level to OR gate U223D. The output of NAND gate U211B is applied to OR gate U223D. The resulting output of U223D consists of 0.2-degree logical 0 pulses with positive-going transitions occurring at the 15, 35, 55, 75, and every 20-degree interval thereafter. This pulse train is applied to the trigger input to flip-flops U213A and U213B. The data (D) input to flip-flop U213A is the M180 output of U219. The M180 signal is a logical 0 from 0 to 180 degrees, and a logical 1 from 180 to 360 degrees. Therefore, flip-flop U213A is

cleared at 15 degrees and set at 195 degrees. The READ output signal from the 1 output of flip-flop U213A is a logical 0 from 15 degrees to 195 degrees and a logical 1 from 195 to 15 degrees.

(d) The M10 output of U218 is applied as an enabling level to NOR gate U210A in the trigger input circuit of flip-flop U212B. The pulse train output of NAND gate U211B is also applied to NOR gate U210A. The output of U210A consists of 0.2-degree logical 1 pulses with the trailing edges of the pulses occurring at 5, 25, and 45 degrees, and every 20-degree increment thereafter. This pulse train is applied to NAND gate U211A along with the M40C output of U218 and the M60B output of U219. The resulting output of NAND gate U211A consists of two pulses occurring every memory counter cycle (0-360 degrees). These pulses are 0.2 degree in duration and are logical 0 pulses, the first pulse trailing edge occurring at 105 degrees and the second pulse trailing edge occurring at 285 degrees. The data (D) input to flip-flop U212B is the M180 signal previously described. Flip-flop U212B is set at 285 degrees and cleared at 105 degrees. The 0 output of U212B is applied to OR gate U223C.

(e) The signal level at the data (D) input to flip-flop U213B is controlled by the output of NAND gate U215D. The M40C signal output of U218 and the M120C output signal of U219 (pin 9) are applied to NAND gate U215D. The output of NAND gate U215D consists of two 20-degree logical 0 pulses with the trailing edge of the first pulse occurring at 180 degrees and the second pulse trailing edge occurring at 360 degrees. The trigger input signal to flip-flop U213B is the output of OR gate U223D. The set input to flip-flop U213B is controlled by NAND gate U208C. The gating level to U208C is the M20B output of U218. This signal gates through every fourth output pulse from OR gate U223D after inversion by U207E. The output of NAND gate U208C is therefore 0.2-degree logical 0 pulses with trailing edges occurring at 35, 95, 155, 215, 275, and 335 degrees. The 1 output of flip-flop U213B is connected to the clear input of U213B. Operation of flip-flop U213B is as follows:

1. At 355 degrees, the flip-flop is triggered to the clear state since the data (D) input is a logical 0 at this time. The next trigger occurring at 15 degrees has no affect since the logical 0 at the 1 output holds the flip-flop in the clear state.

2. At 34.8 degrees, the flip-flop is set by the 0.2-degree logical 0 output of NAND gate U208C and the clear hold is removed since the 1 output of the flip-flop is now at a logical 1 level. The flip-flop remains in the set state until 175 degrees since the data (D) input is a logical 1.

3. At 175 degrees, the flip-flop is triggered to the clear state since the data (D) input is now at a logical 0 level. The trigger occurring at 195 degrees has no affect since the flip-flop is held in the clear state.

4. At 214.8 degrees, the flip-flop is set by the 0.2-degree logical 0 output of NAND gate U208C. The clear hold is removed.

5. At 355 degrees, the cycle starts over.

(f) The 1 output of flip-flop U213B is a logical 0 from 355 degrees to 34.8 degrees (a total of 39.8 degrees) and from 175 to 214.8 degrees (also a total of 39.8 degrees).

(g) The 1 output of flip-flop U213B is applied to OR gate U223C along with the signal from the 0 output of flip-flop U212B. Since flip-flop U212B is in the clear state between 105 and 285 degrees, then only the logical 0 pulse from the 1 output of flip-flop U213B occurring between 355 degrees and 34.8 degrees is coupled through OR gate U223C to become the 0 = ±20° GATE signal.

(h) A 4-stage up/down counter U209 and associated control circuit is used in conjunction with the memory counter. NAND gate U215A is enabled by the 0 = ±20° GATE signal from a time period when the memory counter contains counts equivalent to 34.8 to 355 degrees. When the 15S signal input to single shot U220B occurs

(representative of the 15-Hz amplitude-modulation zero crossing) and this 15S signal is outside the 0 = ±20° GATE, the 3- μsec logical 1 output of U220B is coupled through NAND gate U215A. The output of U215A triggers the divide-by-2 stage of U216. The A output (pin 12) of U216 is provided to the trigger input of the divide-by-2 stage of U219. The A output of U219 is provided to NAND gate U224B. NAND gate U224B is in the count-up trigger input to up/down counter U209. This gate produces a 3- μsec logical 0 output when the output of U220B, the A output (pin 12) of U216, and the A output (pin 12) of U219 are at a logical 1 level. Therefore, after four occurrences of the 15S signal outside the 0 = ±20° GATE, the positive-going edge of the 3- μsec logical 0 output of U224B will provide 1 count-up trigger to the up/down counter.

(i) NAND gate U211C is in the count-down trigger input to up/down counter U209. This gate receives the signal from the 0 output of flip-flop U213B, the signal from the 1 output of flip-flop U212B, and the output from single shot U220B. If the 15S signal (positive-going transition) occurs within the 0 = ±20° GATE, the 3- μsec logical 1 pulse output is coupled through NAND gate U211C and applied to the count down input of U209. If enough 15S signals occur within the 0 = ±20° GATE (a minimum of 15 required), the up/down counter will be triggered to the all zero state. The next count-down trigger results in a logical 0 on the borrow output (BW on pin 13 of U209). This logical 0 is applied to the load (LD on pin 11) input. Since the data inputs (A', B', C', and D') are grounded, a logical 0 borrow clears the counter (all zero state). Once the counter is in the all zero state, additional count-down triggers will have no affect since the logical 0 borrow is applied as the clear input. When the 15S positive-going transition occurs outside the 0 = ±20° GATE four times, then a count-up trigger is applied to U209. When a total of 15 count-up triggers have been applied without the occurrence of a count-down trigger (60 occurrences of the 15S signal outside the 0 = ±20° GATE signal), the up-down counter is in the all 1 state. When the next count-up trigger occurs (4 more occurrences of the 15S signal outside the 0 = ±20° GATE), the carry output (CY on pin 12 of U209) becomes a logical 0. The output of inverter

U207D is a logical 1 and, since the output of single shot U220B is also a logical 1, the memory counter is reset to 9.8 (U218 and U219 in the all zero state, and U216 and U217 in a BCD 9 state).

(j) In addition to selection of the proper 40-degree sector, as previously described, the memory counter introduces a fine phase correction and tracking capability derived from the 135-Hz amplitude modulation and 15-Hz amplitude modulation. The circuit that performs this function consists of up-down counters U203 and U202; single-shots U220B and U220A; NAND gates U201A through U201D, U208D, U208A, and U215B; NOR gate U210B; flip-flops U205A, U205B, U204A, U204B, U206A, and U206B; and exclusive OR gates U214A, U214C, and U214D. The function is performed by adding an extra clock pulse to the 0.2-degree clock input of the memory counter to increase the stored bearing angle by 0.2 degrees, or by deleting one of the 0.2-degree clock pulses to decrease the angle by 0.2 degrees. The process, in detail, is accomplished in the following manner. For normal beacon operation, the 1 = 15 HZ ONLY signal is a logical 0. This signal is obtained from the Panel Unit when the BEARING switch is in the NORMAL position. This logical 0 inhibits NAND gate U215B and enables NOR gate U210B. The 135S signal, indicative of the 135-Hz modulation zero crossing, is coupled through NOR gate U210B and triggers single shot U220A. The resulting 3- μsec logical 1 output of U220A is applied to NAND gates U201A, U201B, U201C, and U201D. NAND gates U201A and U201B, and the data (D) input to flip-flop U205B are controlled by the operation of flip-flop U205A. The trigger input to flip-flop U205A is the output of inverter U207E. Positive-going transitions to the trigger input of U205A occur at 14.8, 34.8, 54.8 degrees and every 20-degree increment thereafter. This data (D) input signal is obtained from exclusive OR gate U214D. This gate receives the M20B output of U218 and the output of a second exclusive OR gate U214C. The M60B and M180 signals are applied to U214C. The output of U214C is a square wave with a period equivalent to 120 degrees. The output of exclusive OR gate U214D is a square wave with a period equivalent to 40 degrees (135 Hz). This square wave is a logical 0 for the first 20 degrees. NAND gate U201A

is therefore enabled for a 20-degree period prior to 14.8 degrees of the memory counter, and for 20-degree periods prior to 54.8, 94.8, and every 40-degree increment thereafter. Since one input to NAND gate U201B is obtained from the 0 output of flip-flop U205A, then U201B is enabled at alternate 20-degree periods from those identified for NAND gate U201A. If the time of occurrence of the positive-going transition of the 135S signal (occurring every 40 degrees) occurs during the 20-degree period before the 14.8, or 54.8 or every 40-degree interval thereafter, the 3- μsec logical 1 output of single shot U220A is coupled through NAND gate U201A and increments the up/down counter U203. Conversely, if the 135S signal occurs during the 20-degree period after the 14.8, or 54.8, or every 40-degree interval therefore, then the output of U220A is coupled through NAND gate U201B and decrements the up/down counter U203. When counter U203 reaches the all zero state, the next down clock pulse results in a logical 0 borrow output (BW at pin 13 of U203). This logical 0 is inverted by U207F and applied to the clear input (RO on pin 14 of U203). The logical 1 on the clear input prevents any additional down clock pulses from changing the state of the counter once the all zero state is reached. When the counter contains a count of 15, the next count up trigger causes a logical 0 output to occur at the carry output (CY on pin 12 of U203). At the trailing edge of this logical 0 (0-to-1 transition), flip-flop U204A is set and the data (D) input to flip-flop U204B becomes a logical 1. The next positive-going transition of the 0.2° CLOCK* triggers U204B to the set state. NAND gate U208D is enabled. The logical 0 from the 0 output of flip-flop U204B clears flip-flop U204A. This logical 0 is also applied to the load input (LD at pin 11) of U203. A logical 0 to the load input sets the counter to the count of 9 when operated in a normal mode (1 = 15 Hz ONLY signal at a logical 0 level) or to the count of 15 when operated in 15-Hz only mode (1 = 15 Hz ONLY signal at a logical 1 level). The second positive-going transition of the 0.2° CLOCK* pulse (occurring after flip-flop U204A is initially set) triggers flip-flop U204B to clear state. NAND gate U208D is inhibited. The output pulse from the 1 output of U204B is 0.2 degrees in duration. During the time interval of the pulse, NAND gate U208D is enabled and

an additional clock pulse obtained from the 0.2° CLOCK input is coupled through U208D and exclusive OR gate U214A. The bearing angle represented by the count in the memory counter is advanced 0.2 degrees. Initially the memory counter is reset to the 9.8 state by the operation of up/down counter U209 (refer to paragraph 2D(4)(g)). The 0 = ±20° GATE signal has a 15 count at the mid-point of this gate signal (355 degrees to 34.8 degrees). The operation of up/down counter U203 adds additional clock pulses until the count in the memory counter is stepped up from the 9.8 count established by the operation of up/down counter U209 to the 15 count. The bearing deviation digital-to-analog converter in the Signal Analyzer Unit requires digital inputs that vary in a linear fashion to provide a minimum of ±10 degree bearing deviation in 0.2-degree increments. The Signal Analyzer Unit then provides an analog voltage representative of the bearing deviation to the COURSE DEVIATION DEGREES meter M7504 and to RECORDER connector J5706. Since these linear inputs cannot be obtained with the memory counter in the all zero state (bearing deviation of 0.2 degrees in one direction would result in outputs changing from all zeros to all ones), the count of 15 is established as the count to represent 0-degrees bearing deviation. For this reason, the memory counter contains a count of 15 at the mid-point of the 0 = ±20° GATE pulse.

(k) The M.2B output of U216 is applied to the trigger input of flip-flop U205B. As previously described, the 0 output of flip-flop U205A is applied to the data (D) input of U205B. The signal at the 1 output of flip-flop U205B is identical to the signal at the 0 output of flip-flop U205A except that it is delayed by a time equivalent to 0.4 degrees. Therefore, except for this 0.4-degree difference, NAND gates U201B and U201D are enabled simultaneously, and NAND gates U201A and U201C are enabled simultaneously. As U203 counts up, U202 counts down and, conversely, as U203 counts down, U202 counts up. Operation of up/down counter U202 and associated circuitry is similar to that previously described for U203; however, flip-flop U206B is triggered by the positive-going transition of the 0.2° CLOCK signal (instead of 0.2° CLOCK* signal) and NAND gate U208A is inhibited by the output of U206B.

The net effect is to remove one clock trigger to the memory counter thus delaying the count of the memory counter by 0.2 degrees.

(l) When the test set is operating in the 15-Hz only mode, the 1 = 15 Hz ONLY signal to the Memory Counter card is a logical 1. NOR gate U210B is inhibited and NAND gate U215B is enabled. The 3- μsec logical 1 output from single shot U220B is coupled through U215B and triggers single shot U220A. Operation of the up/down counters U203 and U202 is the same except that the count triggers are applied at a 15-Hz rate rather than a 135-Hz rate.

(m) Nine outputs from the memory counter are applied to a 9-bit buffer/storage register comprised of U221 and U222. Seven of these bits (M.2B, M.4C, M.8D, M1A, M2B, M4C, and M8D) are applied directly to the data inputs of this storage register. The remaining two bits (M10 and M20B) are applied to the data inputs of the storage register via OR gates U223A and U223B. When the EQ logical 1 pulse occurs (refer to paragraph 2D(3)(h)), the outputs of the memory counter indicative of the bearing angle to the ground beacon are loaded into the buffer/storage register. The nine outputs of this register (D.2B, D.4C, D.8D, D1A, D2B, D4C, D8D, D10, and D20) are applied to the Signal Analyzer Unit for further processing.

(n) Three additional controlling levels (signals) are sampled and stored in the buffer/storage register U221. NAND gate U208B and inverter U207C control the 1 = TO output signal. The 1 = MANUAL signal, a logical 1 when the OBS CONTROL on the Panel Unit is in the MAN position, is applied to NAND gate U208B. The output of NAND gate U208B is provided to inverter U207C. Since NAND gate U208B is enabled, the output of inverter U207C is identical to the signal at the 1 output of flip-flop U212B. This signal is a logical 0 for a count equivalent to a bearing-angle range of 105 to 285 degrees (with respect to an all zero count). However, since a zero-degree bearing angle is actually represented by a count of 15 as previously described, then the 105 to 285 count is actually a bearing-angle range of 90 to 270 degrees. When the bearing deviation

is in a range between 90 to 269.8 degrees from the selected course, the 1 = TO signal becomes a logical 0 when the EQ pulse occurs. When the bearing deviation is in a range between 270 and 89.8 degrees from the selected course, the 1 = TO signal becomes a logical 1 when the EQ pulse occurs. The 1 = TO signal is applied to the Panel Unit to control the LED TO/FROM indicator. This signal is also applied to the Signal Analyzer Unit. When the OBS CONTROL on the Panel Unit is in the AUTO position, the 1 = MANUAL input to the Memory Counter card is a logical 0. This logical 0 inhibits NAND gate U208B thus the output of inverter U207C is a logical 0. The 1 = TO signal is therefore at a continuous logical 0 level thus causing the FROM LED indicator on the Panel Unit to illuminate.

(o) The output of NAND gate U215C controls the level at the clear input (pin 1) of buffer/storage register U222. The 0 output of flip-flop U212A is applied to NAND gate U215C along with the output of exclusive OR gate U214B. The READ signal and the signal from the 0 output of flip-flop U212B are combined in exclusive OR gate U214B to produce a square wave with a period equivalent to 180 degrees. This output is a logical 0 from 15 to 105 degrees and from 195 to 285 degrees. Because of the 15-degree offset between memory counter count and actual bearing angle (0-degree bearing equal 15-degree count), the actual related bearing angle for this output is 0 to 90 degrees and 180 to 270 degrees. The data (D) input to flip-flop U212A is obtained from the 0 output of flip-flop U213B. This data input is a logical 1 from a memory counter count of 355 degrees to 34.8 degrees, and from 175 degrees to 214.8 degrees. The trigger input is the output of inverter U207B, a 20-degree square wave. Positive-going triggers are applied to flip-flop U212A at 0, 20, 40, and every 20-degree increment thereafter. Consequently, the output from the 0 output of flip-flop U212A is a logical 1 from a memory counter count of 40 degrees to 180 degrees, and from 220 degrees to 0 degrees. The output of NAND gate U215C is therefore a logical 0 between memory counter counts of 105 to 180 (bearing angles of 90 to 165 degrees), and between 285 and 0 (bearing angles of 270 to 345 degrees). If the EQ pulse occurs within either of these bearing-angle ranges, a logical 0 is

loaded in buffer/storage register U221 at pin 3, the output at pin 2 is a logical 0, and buffer/storage register U222 is held in the clear state. The six output signals from U222 are logical 0's at least until the next EQ pulse occurs. See area B of figure 7. If the EQ pulse occurs at angles other than between 90 to 165 degrees or between 270 and 345 degrees, the output of U221 pin 2 is a logical 1 and U222 is not cleared. An EQ pulse occurring within these bearing ranges produces an over-range condition since all the output signals of U222 are logical 0's (representing a bearing deviation in excess of 14 degrees).

(p) The second input to OR gates U223A and U223B is obtained from pin 5 of buffer/storage register U221. The output on this pin is controlled by NOR gate U210C. NOR gate U210C is enabled during a time period when the memory counter contains counts from 40 to 180 degrees, and from 220 to 360 degrees (bearing angles from 25 to 165 degrees, and from 205 to 345 degrees). Since the output of exclusive OR gate U214B is applied to NOR gate U210C, then the output of NOR gate U210C is a logical 1 between memory counter counts of 40 and 105 and between 220 and 285 (bearing angles between 25 and 90 degrees, and between 205 and 270 degrees). If the EQ pulse occurs within these bearing angle ranges, then the output on pin 5 of U221 is a logical 1, the outputs of OR gates U223A and U223B are logical 1's, and the D10 and D20 signals become logical 1's. See area A of figure 7. An EQ pulse occurring within these bearing-angle ranges produces an over-range condition since the D10 and D20 signals are the most significant digits and represents a bearing deviation in excess of 15 degrees.

(q) If the EQ pulse appears within the angles defined by the shaded area of figure 7, then the nine output signals (excluding 1 = TO) of the buffer/storage registers U221 and U222 to the Signal Analyzer Unit contain the bearing deviation information in 0.2-degree increments.

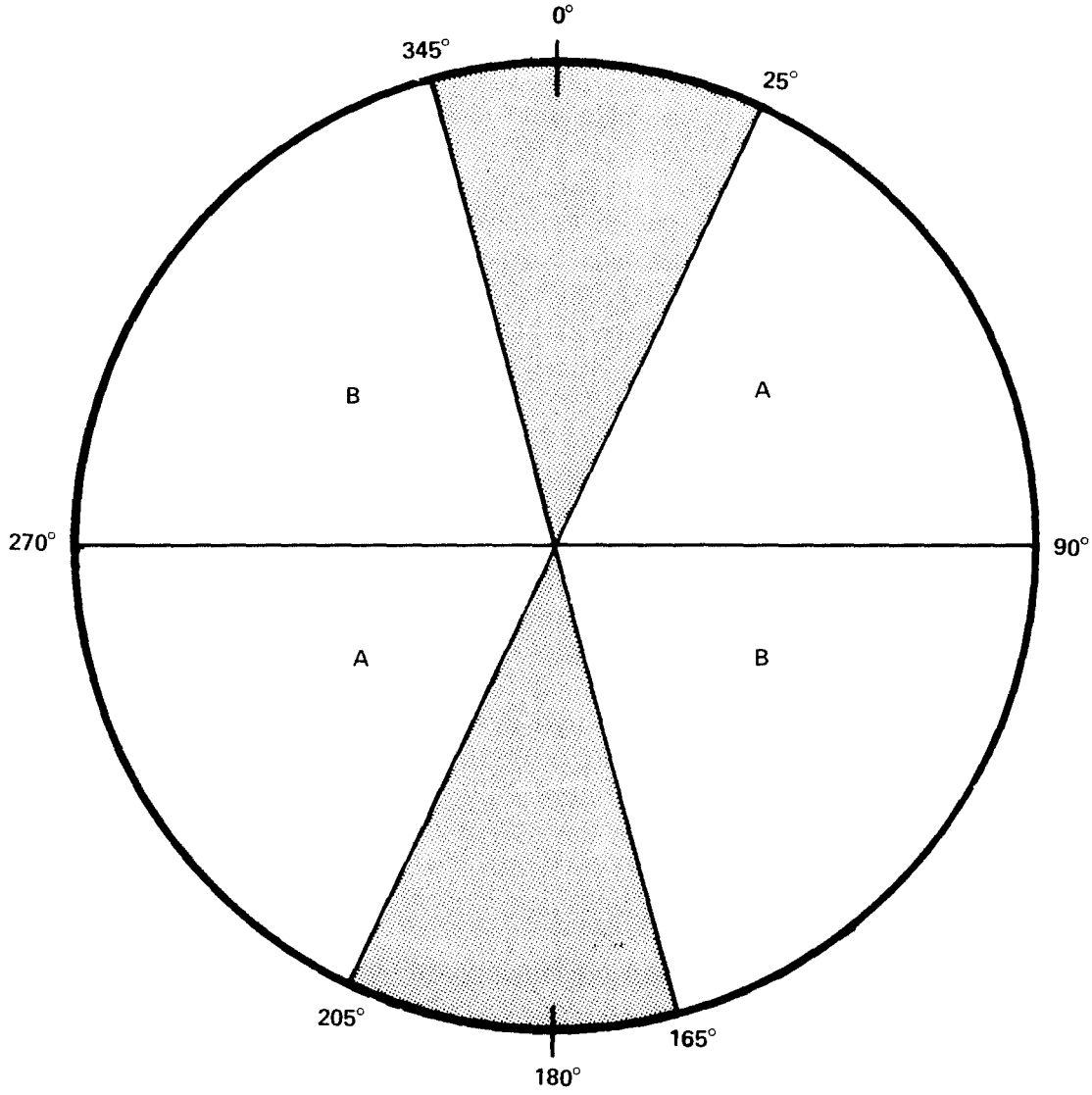
(r) When the system is operated in the automatic mode (OBS CONTROL on Panel Unit in AUTO position), the 1 = MANUAL signal input to the Memory Counter card is at a logical 0 level. This logical 0 level holds

flip-flop U212A in the set state. NOR gate U210C and NAND gate U215C are therefore inhibited. The output of NOR gate U210C is a logical 0 and the output of NAND gate U215C is a logical 1. When the EQ pulse occurs, the output on pin 5 of U221 is a logical 0 and the output on pin 2 of U221 is a logical 1. Buffer/storage register U222 is not cleared and the level of the M10 and M20B outputs of the memory counter are coupled through OR gates U223A and U223B, and applied to the data inputs of U222. The output levels of the nine signals applied to the Signal Analyzer Unit are dependent upon the bearing angle stored in the memory counter when the EQ pulse occurs. As previously indicated, the 1 = TO signal is always a logical 0 in the automatic mode.

(5) Digital Bearing Unit Monitor Card (600)

The Digital Bearing Unit Monitor card continuously monitors the operational status of the other five cards in the Digital Bearing Unit and provides a visual indication of a card failure on one or more light emitting diodes (LED). In addition, any card failure causes the BEARING FAILURE LED on the Panel Unit to illuminate. The Digital Bearing Unit Monitor card utilized in the Digital Bearing Unit can be one of two types. The card is either a 7124-4305-1 or 7124-4305-2. These cards are interchangeable. Theory for the -1 card is given in following paragraphs (a) through (g). The -2 card theory is contained in paragraphs (h) and (i). Figure 920 is the schematic diagram for the -1 card and figure 921 is the schematic diagram for the -2 card.

(a) The +20VDC, +12VDC, -20VDC, and -12VDC outputs of the Power Supply Regulator card are applied to the Digital Bearing Unit Monitor card along with the +5VDC output from the emitter of Q7201 on the main chassis. The +20VDC and -20VDC are applied as operating voltages for dual operational amplifier U609 (see figure 920). The non-inverting input of U609A and the inverting input of U609B are connected to ground. The +12VDC is applied to one end of a voltage-divider network consisting of resistors R608, R609, R617, and R610. The -12VDC is applied to the opposite end of this divider network. Taps at the junction of R609-R617, and R617-R610 supply +0.06 volt and -0.06 volt



NOTES: DEGREES INDICATED ON CIRCLE REPRESENT BEARING DEVIATION (RANGES) WITH RESPECT TO AIRCRAFTS HEADING.

IN BOTH A AREAS, D10 AND D20 OUTPUTS ARE LOGICAL 1'S.

IN BOTH B AREAS, D1A, D2B, D4C, D8D, D10, AND D20 OUTPUTS ARE LOGICAL 0'S.

IN SHADED AREAS, OUTPUTS ARE LINEAR FOR 40-DEGREE RANGE.

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Figure 7. Bearing Deviation Outputs Versus Deviation Ranges (Manual Mode)

to the inverting and non-inverting inputs of U609A and U609B respectively. When the +12 volts and -12 volts are within tolerance, the voltages at these inputs are such that the outputs of U609A and U609B are low. Diodes CR608 and CR606 are thus cut off and U605 LED is not emitting. If either the +12 or -12-volt supplies is out of tolerance, one section of U609 will be high (about +18 volts) and will supply current to illuminate LED U605 (PWR REG) through R602. A high output from either section of U609 will also pull up the anodes of CR613, CR614, and CR615 to +12.7 volts through R607. This will disable comparator U608 to prevent erroneous fault indications from other cards due to a power supply failure. The +5 VDC is applied to the junction of diodes CR609 and CR610. The opposite ends of these diodes connect to the junction of resistors R608 and R609 which provide the precision 5-volt reference level. When the +5 volts d-c input is 5 ± 0.4 volts dc, diodes CR609 and CR610 are reversed biased. If the 5-volt input drops below 4.5 volts or rises above 5.5 volts, then diode CR609 (for +4.5V or less) or CR610 (for +5.5V or more) conducts altering the current flow through the divider network and causing the output of U609A or U609B to become high. LED U605 conducts and the PWR REG indicator illuminates indicating a power supply failure.

(b) The Video Signal Processor card monitoring circuitry checks that the LIMITED VIDEO signal transitions at a normal rate, and that the active bandpass filter circuits are operating properly. The first check is accomplished by toggling retriggerable monostable multivibrator U607A with the LIMITED VIDEO signal. The 3-millisecond period of this one shot, established by R605 and C604, insures that its 0 output will remain low for normal system operation. Failure of the video amplifier, video limiter, peak detector, or AGC amplifier circuits will eliminate LIMITED VIDEO pulses, and will allow the one shot to return to its stable state. The resulting logical 1 on the 0 output is processed by a low-pass filter consisting of R619 and C611 to prevent brief interruptions of LIMITED VIDEO pulses (as might occur during channel changing) from causing a fault indication. However, a continuous high output from the one shot would cause the voltage at the non-inverting

input of comparator U608A, connected to C611 through current limiting resistor R618, to exceed the +0.3-volt reference at its inverting input. (The +0.3 and -0.3-volt references are derived from the +12 and -12-volt supplies by resistor-divider network R614 through R615.) The comparator output will then be pulled up to +12 volts, causing current to be supplied to LED U604 through R601 to illuminate the VID PCR fault indicator.

(c) The active bandpass filter circuits are checked by verifying that they have no d-c output component. The 15- and 135-Hz filter outputs are summed by equal resistors on the Digital Video Signal Processor card, and the resulting FILTER MONITOR signal is applied to C611 to filter out the a-c components of this signal. If either active filter circuit fails, the resulting output d-c component will cause the non-inverting input of U608A to exceed the +0.3-volt reference, or the inverting input of U608B to fall below the -0.3-volt reference. In either case, one of the outputs of U608 will be pulled up, thus illuminating the VID PCR fault indicator.

(d) The Pulse Group Decoder card is monitored by checking that the LIMITED VIDEO signal is being shifted by the 1-MHz clock (derived from the 4-MHz crystal oscillator) down the entire length of the decoder shift register. The output of the last stage of the shift register, called PGD MONITOR, is applied to retriggerable monostable multivibrator U607B. The 0 output of this one shot, having a 3-millisecond astable period determined by R613 and C606, will remain low for normally occurring PGD MONITOR pulses. Should these pulses fail to occur due to a failure on the Pulse Group Decoder card, the level on the 0 output will become a logical 1 and will supply current to LED U603 to illuminate the PLS DEC fault indicator. If, however, PGD MONITOR pulses fail to occur due to missing LIMITED VIDEO information, the level on the 0 output of U607A will also be a logical 1, causing no current to flow through LED U602, thus preventing a false PLS DEC failure indication.

(e) The 8-microsecond EQ pulse occurring approximately every 67 milliseconds is applied to the trigger input of retriggerable monostable multivibrator U606A. The duration of the pulse output of U606A is greater than 67 milliseconds, therefore since this circuit is retriggerable, the 1 output of U606A remains at a logical 1 level as long as the EQ pulse occurs at the 15-Hz rate. When the 1 output of U606A is at a logical 1 level, LED U601 remains extinguished. If the EQ pulse fails to occur, then the 1 output of U606A changes to a logical 0 level, LED U601 conducts and the REF CTR indicator illuminates thereby signifying a failure on the Reference Counter card.

(f) The 180-degree (approximately 33 milliseconds) READ pulse is applied to the trigger input of retriggerable monostable multivibrator U606B. The READ pulse is an output of the Memory Counter card and occurs approximately every 67 milliseconds. The circuit operates identically to the circuit described in paragraph 2 D (5) (h). If the READ pulse fails to occur, LED U602 conducts and the MEM CTR indicator illuminates thereby signifying a failure on the Memory Counter card.

(g) The anode end of each LED fault indicator is coupled to a common node through diodes CR601, CR602, CR604, CR605 and CR607 with R611 providing a ground return. If any failure detection occurs, this node will be pulled up to a logical 1 level and begin to charge C603 through R612. If the fault persists for several seconds, the voltage across C603 becomes sufficiently positive to cause NPN Darlington Q601 to conduct. This grounds the DIGITAL BEARING FAILURE line thus causing the BEARING FAILURE indicator on the Panel Unit to illuminate. Diode CR611 prevents an inductive backswing from damaging Q601 when it becomes non-conductive.

NOTE: Following paragraphs (h) and (i) apply only to a 7124-4305-2 Digital Bearing Unit Monitor card.

(h) The +20VDC, +12VDC, -20VDC, and -12VDC outputs of the Power Supply Regulator card are applied to the Digital Bearing Unit Monitor card along with the +5VDC output from the emitter of Q7201 on the main chassis. The +20VDC and -20VDC are applied as operating voltages for dual operational amplifier U609 (see figure 921). The non-inverting input of U609A and the inverting input of U609B are connected to ground. The +12VDC is applied to one end of a voltage-divider network consisting of resistors R608, R609, R617, and R610. The -12VDC is applied to the opposite end of this divider network. Taps at the junction of R609-R617, and R617-R610 supply +0.06 volt and -0.06 volt to the inverting and non-inverting inputs of U609A and U609B respectively. When the +12 volts and -12 volts are within tolerance, the voltages at these inputs are such that the outputs of U609A and U609B are low. Diodes CR608 and CR606 are thus cut off and U605 LED is not emitting. If either the +12 or -12-volt supplies is out of tolerance, one section of U609 will be high (about +18 volts) and will supply current to illuminate LED U605 (PWR REG) through R602. A high output from either section of U609 will also cause transistor Q602 to conduct, therefore the cathode of diode CR613 is at ground level (approximately). The anode of LED U604 is held at this low level during a power supply failure, thus preventing a VID PCR fault indication. The +5VDC is applied to the junction of diodes CR609 and CR610. The opposite ends of these diodes connect to the junction of resistors R608 and R609 which provide the precision 5-volt reference level. When the +5 volts d-c input is 5 ± 0.4 volts dc, diodes CR609 and CR610 are reversed biased. If the 5-volt input drops below 4.5 volts or rises above 5.5 volts, then diode CR609 (for +4.5 V or less) or CR610 (for +5.5V or more) conducts altering the current flow through the divider network and causing the output of U609A or U609B to become high. LED U605 conducts and the PWR REG indicator illuminates indicating a power supply failure.

(i) The remaining circuits on the Digital Bearing Unit Monitor card 7124-4305-2 are identical to those described for a 7124-4305-1 card. Refer to paragraphs 2D(5)(b) through 2D(5)(g).

(6) Power Supply Regulator Card (100)

The Power Supply Regulator card provides the Digital Bearing Unit with the following voltages:

1. +20 volts dc and -20 volts dc unregulated

2. +12 volts dc and -12 volts dc regulated

3. +5.7 volts dc regulated

(a) A full-wave rectifier/filter comprised of diodes CR101 and CR102 and capacitor C104 converts the 15-volt, 400-Hz input into +20 volts dc (see figure 915). The +20 volts dc is applied to the positive monolithic voltage regulator U101. Transistor Q101 and R101 combine as a 400 ma short-circuit limiter for U101. Capacitor C101 provides frequency compensation, C102 is an output voltage noise filter, and C103 provides low source impedance for high frequency a-c load components. Resistor network R102, R103, and R105 determines the gain of the positive-regulator reference amplifier. The regulated output voltage is set to +12.00 volts dc by adjusting R103.

(b) A similar full-wave rectifier/filter comprised of diodes CR104 and CR105 and capacitor C105 converts the 15V, 400-Hz input into -20 volts dc. The negative monolithic voltage regulator U102 differs from the positive regulator U101 in that only R106 is required to provide a 400 ma short-circuit current limiter for U102. As in the positive regulator circuit, C106 provides frequency compensation, C107 is an output voltage noise filter, and C108 is the output capacitor. Resistor network R107, R108, and R109 determines the gain of the negative regulator reference amplifier. The regulated output voltage is set to -12.00 volts dc by adjusting R108.

(c) The 5.1-volt zener diode VR101 and diode CR103 combine to establish a 5.7-volt d-c level. The stability of this voltage is enhanced by supplying the zener current from the +12-volt d-c regulated supply through R104. The 5.7-volt d-c reference is used to bias the pass-transistor associated with the 5-volt d-c power supply.

(7) Main Frame Mounted Power Supply Circuit Components

The power transformer T7201, full-wave bridge type rectifier CR7201 for 5-volt regulated power supply, filter capacitor C7201, and series regulator for the 5-volt regulated power supply are mounted on the main frame (see figure 914). The 115-volt ac, 400-Hz, single-phase power is applied to the primary winding of transformer T7201. The 15-volt a-c output from one secondary winding is applied to the Power Supply Regulator card. The 7-volt a-c output from a second secondary winding is applied to full-wave bridge type rectifier CR7201. The rectified output of CR7201 is filtered by capacitor C7201 and applied to the collector of series regulator transistor Q7201. The base of Q7201 receives the 5.7-volt d-c reference from the Power Supply Regulator card. The 5-volt d-c regulated output appears on the emitter of Q7201.

E. Signal Analyzer Unit General Theory

(1) The Signal Analyzer Unit receives signals from the Digital Bearing Unit and the DME (see figure 8). Some of the received signals are converted to analog voltages and are provided to meter circuits and also for strip-chart recording. In addition, certain signals are monitored by voltage comparators whose outputs are connected to LED drivers that control OVER and UNDER function indicators on the Panel Unit. Circuit control signals are applied to the Signal Analyzer Unit to permit the analyzing circuits to operate in either the X or Y mode (1 = Y MODE signal), TACAN or DME mode (1 = DME signal), manual or automatic mode (1 = MANUAL signal), and TO or FROM mode (1 = TO signal). The 1 = DME and 1 = MANUAL signals are received from the Panel Unit, the 1 = Y MODE signal is received from the DME, and the 1 = TO signal is received from the Digital Bearing Unit. The operating characteristics of the ground beacon that are checked by the Signal Analyzer Unit are antenna speed, squitter rate, phase coherency, MRG size, ARG size, and ARG count. The results of these signal checks are indicated on OVER and UNDER indicators on the Panel Unit. The analog signals provided to recording equipment are squitter rate, bearing deviation, percent of range replies, phase coherency, and automatic gain control.

(2) Antenna Speed

The antenna speed input signal to the Signal Analyzer Unit is identified as ANT. SPEED. This signal has a range of ±10V dc and corresponds to an antenna speed range of 890 to 910 rpm. A double-limit voltage detector determines if the antenna speed is within ±1.8 rpm.

(3) Squitter Rate

Each successfully decoded pulse pair is represented by a 1-μsec pulse generated in the Digital Bearing Unit. This input signal is identified as PULSE PAIRS BUFFERED and is applied to a clocked one-shot circuit. The ±2° GATE pulse, also from the Digital Bearing Unit, brackets the reference groups and prohibits operation of the clocked one-shot during the reception of reference groups. The 0.2° buffered clock is used to standardize the output width of the one-shot. For each PULSE PAIRS BUFFERED pulse received, the one-shot provides an output to the event-to-voltage converter. The resultant pulse train is

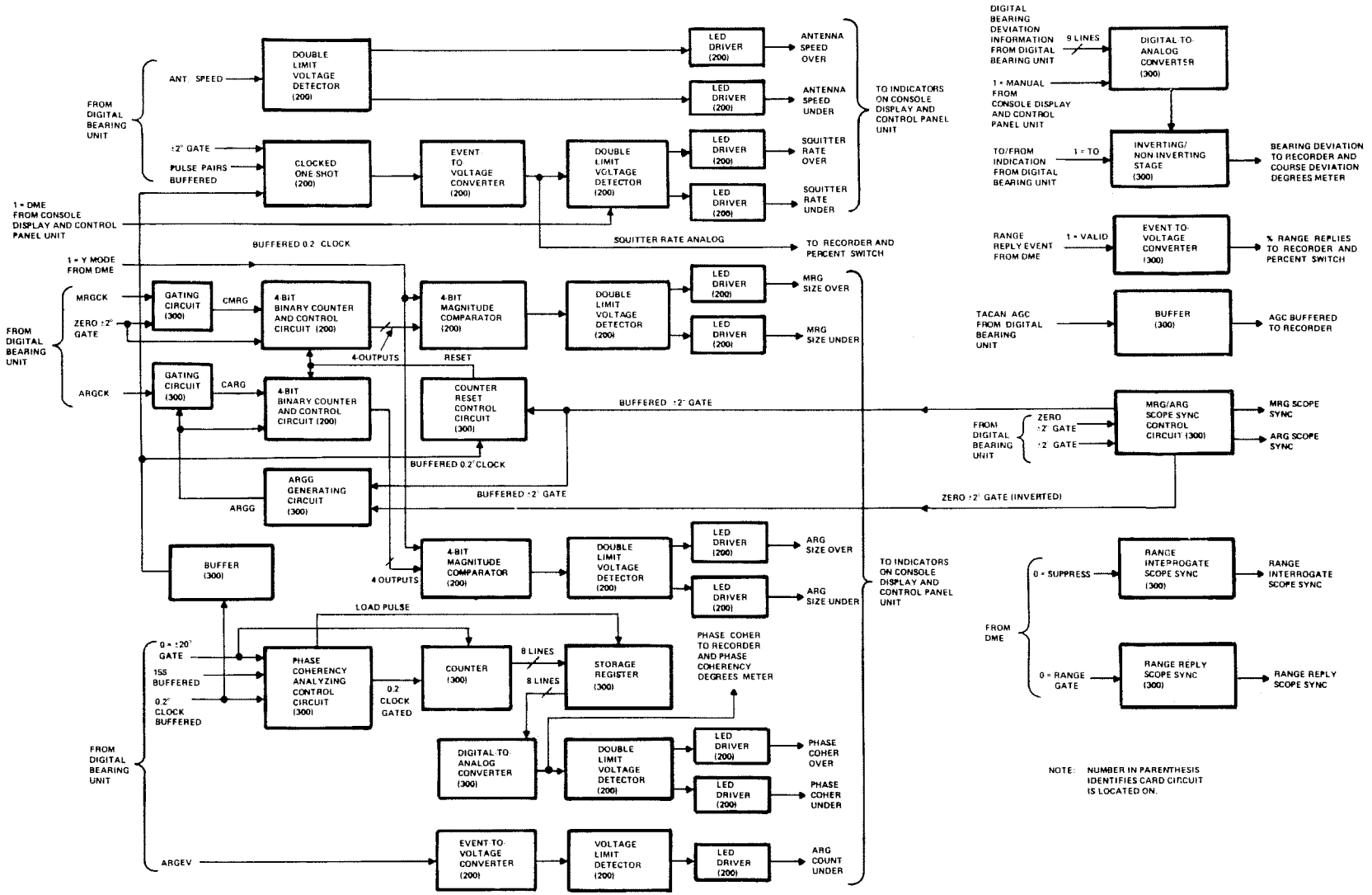

Figure 8. Signal Analyzer Unit Block Diagram

amplified to a precise pulse-height signal which is averaged and further amplified to provide 10V dc for 2700 pulse-pairs per second (actually 2430 pulse-pairs per second since 36 degrees of each cycle are gated out to account for the reference pulse groups), the squitter rate for a TACAN beacon. For a DME only station, the lower threshold limit of the double-limit voltage detector is switched to a lower level by the 1 = DME signal thus changing the squitter pulse limit range from 2700 ±5 percent for TACAN beacons to a range of 700 to 2835 pulse pairs for a DME only beacon. This lower threshold level is controlled by operation of the SQUITTER switch on the Panel Unit.

(4) MRG and ARG Size

The MRG and ARG sizes are monitored by processing the MRGCK and ARGCK outputs of the pulse group decoder in the Digital Bearing Unit. The MRGCK signal is gated by the ZERO ±2° GATE output signal from the Digital Bearing Unit. The resulting CMRG (clock for MRG circuit) signal drives a 4-bit, binary counter that stores the number of decoded pulse pairs occurring within the ZERO ±2° GATE. The ARGCK signal is gated by the ARGG (ARG gate) signal from the ARGG generating circuit. The resulting CARG (clock for ARG circuit) signal drives a 4-bit binary counter that stores the number of decoded pulse pairs occurring within the ARGG signal. The outputs of these counters are applied to 4-bit magnitude comparators that produce a logical 0 output if the proper count is recognized. The output of the 4-bit magnitude comparator is then compared in double-limit voltage detectors. The X-Y mode selection signal (1 = Y MODE) controls operation of the 4-bit magnitude comparator such that the proper output is provided to indicate normal, over, or under MRG or ARG size for X or Y mode of operation. The RESET signal from the counter reset control circuit resets the counters prior to the arrival of the MRGCK and ARGCK pulse groups.

(5) ARG Count Analysis Circuit

The occurrence of each decoded ARG in the Digital Bearing Unit produces a 3.3-millisecond gate (ARGEV) pulse. This ARGEV pulse is applied to an event-to-voltage converter. The output of this converter is applied to a voltage limit detector. Should the number of ARGEV pulses be less than eight per antenna revolution, the LED driver conducts and the ARG COUNT UNDER indicator on the Panel Unit illuminates.

(6) Phase Coherency

The phase coherency measurement is derived from the 15-Hz zero crossing signal (15S BUFFERED) and ±20-degree memory gate (0 = ±20° GATE), both signals are generated in the Digital Bearing Unit. These two signals are provided to the phase coherency analyzing control circuit in the Signal Analyzer Unit along with the 0.2° CLOCK BUFFERED signal. The counter is held in the all zero state until the 0 = ±20° GATE pulse occurs. When this pulse occurs, the 0.2° clock gated signal triggers the counter until the 15S BUFFERED positive-going transition inhibits further triggers. The LOAD PULSE transfers the count from the counter to the storage register. The output of the storage register is applied to a digital-to-analog converter and the PHASE COHER analog output of this converter is applied to the double-limit voltage detector. If the phase coherency remains within ±5 degrees, the LED drivers are cut off and the associated over/under indicators on the Panel Unit remain extinguished. The PHASE COHER signal is provided to recording equipment and to the PHASE COHERENCY DEGREES meter.

(7) Bearing Deviation

The digital bearing deviation information from the Digital Bearing Unit is provided to a digital-to-analog converter. The digital bearing information is compared in the Digital Bearing Unit with the digital output of the COURSE SELECT DEGREES control on the Panel Unit to produce the digital bearing deviation information. The analog output of the digital-to-analog converter is provided to an inverting/non-inverting amplifier stage. The to/from indicator signal (1 = TO) from the Digital Bearing Unit determines that the inverting/non-inverting stage functions as a non-inverter when the 1 = TO signal is a logical 0 and as an inverter when the 1 = TO signal is a logical 1. The 1 = MANUAL signal controls operation of the digital-to-analog converter during manual or automatic mode of operation. Selection of circuit operation is controlled by the OBS CONTROL switch on the Panel Unit. The output from the inverter/non-inverter stage, BEARING DEVIATION, has an accuracy of ±0.2 degrees from zero to ±14 degrees from the selected course. The BEARING DEVIATION signal is provided to the COURSE DEVIATION DEGREES meter and to recording equipment.

(8) Percent Range Replies

The range reply events from the DME (1 = VALID signal) is provided to an event-to-voltage converter in the Signal Analyzer Unit. The % RANGE REPLY output of this stage is an analog signal. It is provided to recording equipment and to the PERCENT meter via the PERCENT switch. This signal covers a range of at least 30-80 percent with an output of 10-percent-per-volt in the 0 to 10V range, and has an averaging time constant of 1 second.

(9) AGC Signal

The TACAN AGC output of the Digital Bearing Unit is applied to a buffer stage in the Signal Analyzer Unit when the TACAN AGC/DME AGC switch is in the TACAN AGC position. This AGC signal is buffered and provided to recording equipment.

(10) MRG and ARG Scope Sync

The ZERO $\pm 2°$ GATE and $\pm 2°$ GATE outputs of the Digital Bearing Unit are applied to a MRG/ARG scope sync control circuit. This circuit provides the MRG and ARG SCOPE SYNC signals to the SYNC connector via the SYNC switch. This circuit also provides the BUFFERED $\pm 2°$ GATE signal to the counter reset control circuit and to the ARGG generating circuit. In addition, the inverted ZERO $\pm 2°$ GATE is provided to the ARGG generating circuit.

(11) Range Interrogate and Range Reply Scope Sync

The 0 = SUPPRESS signal from the DME is inverted by the range interrogate scope sync circuit and becomes the RANGE INTERROGATE SCOPE SYNC signal. Likewise, the 0 = RANGE GATE output of the DME is inverted by the range reply scope sync circuit and becomes the RANGE REPLY SCOPE SYNC signal. These synchronizing signals are applied to the SYNC connector via the SYNC switch.

F. Signal Analyzer Unit Detailed Theory

To accomplish the Signal Analyzer Unit functions described in previous paragraphs 2 E through 2 E (1), three printed-circuit cards are required. These cards are identified as the Signal Processor, Limit Detector, and Power Supply Regulator. Additional electrical parts are mounted on the main frame.

(1) Signal Processor Card (300)

The functions performed by the Signal Processor card are as follows:

1. Process the digital bearing deviation information outputs and the 1 = TO output of the Digital Bearing Unit and provide the analog BEARING DEVIATION signal to a recorder.

2. Provide a phase coherency analog (PHASE COHER) signal to the Limit Detector card, PHASE COHERENCY DEGREES meter, and to a recorder.

3. Analyze the 1 = VALID signal input from the DME and provide the % RANGE REPLY signal to the recorder and to the PERCENT meter via the PERCENT switch.

4. Process the ZERO ±2° GATE, ±2° GATE, 0 = SUPPRESS, and 0 = RANGE GATE input signals and provide four signals (MRG SCOPE SYNC, ARG SCOPE SYNC, RANGE REPLY SCOPE SYNC, and RANGE INTERROGATE SCOPE SYNC) for synchronizing an oscilloscope.

5. Provide a RESET signal to the main reference group clock (MRGCK) and auxiliary reference group clock (ARGCK) counters on the Limit Detector card.

6. Provide the ARGG (auxiliary reference group gate) signal to the Limit Detector card.

7. Gates the MRGCK and ARGCK input signals from the Digital Bearing Unit, and provides the resulting clocks (CMRG and CARG signals) to the main reference group and auxiliary reference group clock counters on the Limit Detector card.

(a) The Digital Bearing Deviation information output signals of the Digital Bearing Unit are provided to the digital-to-analog converter consisting of inverters U301F, U301A, U301B, U317A through U317F; resistors R301, R304, R303, R349, R348, R344, R350, R351, R345, R346, R347, R306, R302, R334, R333, R335, and R307; and integrated circuit U313A (see figure 926). An additional gating circuit consisting of resistor R332, inverters

U311A and U311B, and NAND gates U310A and U310B are controlled by the 1 = MANUAL signal and are located in the input circuit of the digital-to-analog converter. The digital bearing deviation information output signals of the Digital Bearing Unit are identified as follows:

D. 2B (Bearing deviation decode 1 - least significant bit)
D. 4C (Bearing deviation decode 1 - 2nd least significant bit)
D. 8D (Bearing deviation decode 1 - most significant bit)
D1A (Bearing deviation decode 2 - least significant bit)
D2B (Bearing deviation decode 2 - 2nd least significant bit)
D4C (Bearing deviation decode 2 - 3rd least significant bit)
D8D (Bearing deviation decode 2 - most significant bit)
D10 (Bearing deviation decode 3 - least significant bit)
D20 (Bearing deviation decode 3 - most significant bit)

(b) The bearing deviation information on the first three inputs (D. 2B, D. 4C, and D. 8D) is provided in BCD form for binary numbers 0 through 5 with each binary number equal to 0. 2-degree deviation. The bearing information on the next four inputs (D1A, D2B, D4C, and D8D) is also provided in BCD form for binary numbers 0 through 9 with each binary number equal to 1. 0-degrees deviation. The D10 and D20 input bearing information is in BCD form for binary numbers 0 through 3 with each binary number equal to 10 degrees deviation. When the test set is operated in the manual mode (OBS CONTROL on Panel Unit in MAN position), bearing deviation information is provided in a linear fashion in 0. 2-degree increments over a range of +25 degrees to -15 degrees for an on course heading or a heading 180 degrees from course (see figure 7). Since the bearing deviation information must be linear, a bearing count of 15 is used as a bearing deviation of 0 degrees. This allows the digital-to-analog converter to produce a linear output over a bearing deviation range of at least ±10 degrees. Therefore, for 0-degree deviation (or 180-degree deviation), the input level of the nine input signals is as follows:

D. 2B Logical 0 (Least Significant Bit)
D. 4C Logical 0
D. 8D Logical 0

D1A	Logical 1
D2B	Logical 0
D4C	Logical 1
D8D	Logical 0
D10	Logical 1
D20	Logical 0 (Most Significant Bit)

(c) The output of U313A is 0 volts when a zero-degree deviation input is received. The output of U313A is provided to unity-gain inverting/non-inverting amplifier stage U313B.

(d) When the 1 = MANUAL signal is a logical 1, NAND gates U310A and U310B are enabled. The D10 input signal level is coupled through and double inverted by inverter U311B and NAND gate U310A, and applied to inverter U317B. In a similar manner, the D20 input signal level is coupled through and double inverted by NAND gate U310B and inverter U311A, and applied to inverter U317A. When the 1 = MANUAL signal is a logical 1, The D10 and D20 input signal logic levels have an affect upon the d-c level output of the digital-to-analog converter. When the 1 = MANUAL signal is a logical 0, NAND gates U310A and U310B are inhibited. The input to inverter U317B is a logical 1 and the input to inverter U317A is a logical 0. The D10 and D20 inputs to the Signal Analyzer Unit have no affect upon the operation of the digital-to-analog converter when the 1 = MANUAL signal is a logical 0.

(e) The 1 = TO input signal from the Digital Bearing Unit is applied to the emitter of transistor Q304 and controls the operation of the inverting/non-inverting stage U313B. When the 1 = TO signal is a logical 1, transistor Q304 conducts and the gate input of FET Q303 becomes high, Q303 conducts, and U313B operates as a unity-gain inverter. When the 1 = TO signal is a logical 0, transistor Q304 is cut off, FET Q303 is cut off, and U313B operates as a unity-gain non-inverter. The 1 = TO signal is a logical 0 whenever the test set is operated in the automatic mode (OBS CONTROL on Panel Unit in AUTO position). When the test set is operated in the manual mode, the 1 = TO signal is a logical 1 if the aircraft heading is 0 ±90 degrees of the selected heading (selected heading determined by the position of the

COURSE SELECT DEGREES thumbwheel switches on the Panel Unit). If the aircraft heading is 180 ±90 degrees of the selected heading, the 1 = TO signal is a logical 0. The BEARING DEVIATION output signal of U313B is such that for 10-degree deviation, there is 150-microamperes output into a 1000-ohm load. For a 5-degree deviation, the output is 75 microamperes into a 1000-ohm load. Each degree of deviation is equal to a 15-microampere change in output current.

(f) The phase coherency analyzing circuit consists of a control circuit, counter, a buffer storage circuit, and a digital-to-analog converter. The control circuit consists of flip-flops U307A and U307B; NAND gates U312A and U312D; and inverters U314D, U311E, U312B, U301C, and U311F. The counter is an 8-stage counter consisting of two 4-bit binary counters (U305 and U306) connected in series. The eight outputs of the counter are provided to the 8-bit storage register consisting of two 4-bit storage circuits U302 and U303. The outputs of the storage register are applied to the digital-to-analog converter. Flip-flop U307A of the control circuit is held in the clear state by the output of the U314D until the logical zero 0 = ±20° GATE pulse occurs (approximately 7.4 milliseconds in duration occurring every 67 milliseconds). The counter is held in the reset state (all logical 0 outputs to the storage circuit) by the output of inverter U311E except during the duration of the logical zero 0 = ±20° GATE pulse. The 0.2° CLOCK BUFFERED pulse output of the Digital Bearing Unit (a clock pulse occurring approximately every 37.5 microseconds) is inverted by U312B and applied to the trigger input of flip-flop U307A. The clock pulse output of inverter U312B is inverted by U312C and applied as one input to NAND gate U312A. Flip-flop U307B is initially in the clear state as a result of the logical 0 output of NAND gate U312D. When the 0 = ±20° GATE pulse occurs, the 0.2° clock pulse output of inverter U312C is gated through NAND gate U312A and inverter U311F, and increments the 8-stage counter. When the logical 1 15S signal occurs (an output of the Digital Bearing Unit representing the 15-Hz zero crossing), the next positive-going transition of the output of inverter U312B sets flip-flop U307A. The logical 0 from the 0 output of flip-flop U307A inhibits NAND

gate U312A thus the counter is no longer incremented for this cycle. The positive-going transition from the 1 output of flip-flop U307A sets flip-flop U307B. The resulting logical 0 from the 0 output of flip-flop U307B is inverted by U301C and loads the storage register with the binary count contained in the counter. When flip-flop U307B is set, NAND gate U312D couples the next positive-going clock output from inverter U312C through, thus flip-flop U307B is immediately cleared (returned to initial condition). The load pulse to the storage register is therefore a momentary pulse (duration less than 37.5 microseconds). The count that is stored is representative of the time period between the leading edge of the 0 = ±20° GATE pulse and the 15S positive-going transition. When the 15S positive-going transition occurs in the center of the 0 = ±20° GATE pulse, the phase difference is zero. The count contained in the storage register for zero phase difference is 100 (20 degrees from leading edge of 0 = ± 20° GATE pulse, five trigger pulses per degree). For zero phase difference, the PHASE COHER output signal of U308B is 0 volts. For each degree that the 15-Hz zero crossing (15S) occurs earlier than the center of the 0 = ±20° GATE pulse, the count contained in the storage counter is 5 less than 100 and the voltage output of U308B is 0.5V more negative; i.e., for 5 degrees early, the count is 75 and the output is -2.5V. Similarly, for each degree that the 15-Hz zero crossing (15S) occurs after the center of the 0 = ±20° GATE pulse, the count contained in the storage counter is 5 greater than 100 and the voltage output of U308B is 0.5V more positive; i.e., for 5 degrees late, the count is 125 and the output is +2.5V. The PHASE COHER output of U308B is provided to the Limit Detector card (refer to paragraph 2 E (2)), to the PHASE COHERENCY DEGREES meter, and to a recorder.

(g) The percent of range reply circuit is an event-to-voltage converter circuit consisting of transistors Q302 and Q301; resistors R309, R323, R328, R329, R330 and R331; capacitor C301; and integrated circuit U309A. The 1 = VALID signal from the DME is the input to this circuit. This signal is at a logical 1 level for a percentage of time equivalent to the percentage of range replies; i.e., 1 = VALID signal at a logical 1 level for 50 percent of the time if 50 percent range replies are received. The

% RANGE REPLY signal is a d-c level in the range of 0 to +10 volts. The output range covers at least 30 to 80 percent range replies with 3 volts representing 30 percent and 8 volts representing 80 percent. Each 1-volt increment is equal to a 10-percent factor of range replies. This % RANGE REPLY signal is applied to a recorder and to the PERCENT meter via PERCENT switch.

(h) The TACAN AGC input signal from the Digital Bearing Unit is applied to buffer U309B when the TACAN AGC/ DME AGC switch S7505 is in TACAN AGC position. The output of buffer U309B is applied to a recorder via resistors R324 and R310.

(i) The ZERO ±2° GATE logical 1 input pulse from the Digital Bearing Unit is applied to inverter U316F. The resulting logical 0 output of U316F clears flip-flop U315A and the ARG SCOPE SYNC signal becomes a logical 0. The logical 0 output of U316F is inverted by U316E. The output of U316E is identified as MRG SCOPE SYNC. The first logical one ±2° GATE pulse from the Digital Bearing Unit to occur after the ZERO ±2° GATE pulse sets flip-flop U315A. The ±2° GATE pulse is applied to the trigger input of U315A via inverters U316A and U316B. When U315A is set, the ARG SCOPE SYNC signal becomes a logical 1 and remains at the logical 1 level until the next ZERO ±2° GATE pulse occurs. The ARG SCOPE SYNC and MRG SCOPE SYNC signals are used to facilitate oscilloscope display.

(j) The 0 = SUPPRESS and 0 = RANGE GATE input signals from the DME are applied to inverters U316D and U316C respectively. When the 0 = SUPPRESS signal becomes a logical 0, the RANGE INTERROGATE SCOPE SYNC signal becomes a logical 1. Likewise when the 0 = RANGE GATE signal becomes a logical 0, the RANGE REPLY SCOPE SYNC signal becomes a logical 1. The RANGE REPLY SCOPE SYNC and RANGE INTERROGATE SCOPE SYNC signals are used to facilitate oscilloscope display.

(k) The RESET signal generating circuit consists of flip-flop U315B, NAND gate U310D, and inverter U311D. Flip-flop U315B is initially in the clear state. When the ±2° GATE becomes a logical 1, the data (D) input to flip-flop U315B becomes a logical 1 and NAND gate U310D is enabled. The logical 0 output of U310D is inverted by U311D thus the RESET signal becomes a logical 1. The next positive-going transition of the 0.2° clock output of inverter U312C sets flip-flop U315B. NAND gate U310D is inhibited thus the RESET signal returns to a logical 0 level until the next ±2° GATE pulse occurring at a 135-Hz rate appears. Since the 0.2° CLOCK BUFFERED and ±2° GATE signals are both generated from the same timing circuit in the Digital Bearing Unit, and since the 0.2° CLOCK BUFFERED is inverted by U312B on the Signal Processor card, then the pulse duration of the RESET pulse is equivalent to a 0.1-degree time period (approximately 18.5 microseconds).

(l) The ARGG signal generating circuit consists of NAND gate U310C, inverter U311C, resistor R340, and capacitor C306. NAND gate U310C is enabled to couple through and invert the ±2° GATE signal (occurring at a 135-Hz rate) except when the ZERO ±2° GATE signal, is applied after inversion by U316F. The ZERO ±2° GATE occurs at a 15-Hz rate and is in phase with one of the ±2° GATE pulses. Resistor R340 and capacitor C306 provide a 1-microsecond delay to assure that no output occurs from NAND gate U310C when the ZERO ±2° GATE pulse is applied. The ARGG output pulse is a pulse equivalent to 4 degrees in duration and occurring at a 135-Hz rate with every ninth pulse of this pulse train eliminated by the gating action of U310C.

(m) The MRGCK and ZERO ±2° GATE signal outputs of the Digital Bearing Unit are applied to NAND gate U314C. The CMRG output signal of U314C is applied to the Limit Detector card.

(n) The ARGCK signal output of the Digital Bearing Unit is applied to NAND gate U314B along with the ARGG output of inverter U311C. The CARG output of U314B is applied to the Limit Detector card.

(2) Limit Detector Card (200)

The Limit Detector card utilized in the Signal Analyzer Unit can be one of two types. The card is either a 7124-1110-1 or 7124-1110-2. These cards are interchangeable. Theory for the -1 card is given in following paragraphs (a) through (g). Theory for the -2 card is given in following paragraphs (h) through (l). The functions performed by the Limit Detector card are as follows:

1. Analyze the ANT. SPEED signal and provide over and under antenna speed indication signals to the Panel Unit.

2. Analyze the squitter rate and provide over and under squitter rate indication signals to the Panel Unit. It also provides SQUITTER RATE ANALOG signal to recording equipment and to the PERCENT meter via the PERCENT switch.

3. Provide over and under phase coherence indicating signals to the Panel Unit.

4. Analyze the clock for the main reference group (CMRG) and clock for the auxiliary reference group (CARG) and provide over and under MRG and ARG indicating signals to the Panel Unit.

5. Provide the auxiliary reference group count indicating signal to the Panel Unit.

(a) The ANT. SPEED input signal is provided to an attenuator consisting of resistors R238 and R237 (see figure 924). The ANT. SPEED signal is an analog voltage having a range of ±10V dc corresponding to an antenna speed range of 890 to 910 rpm. The attenuator output is approximately 40 percent of the d-c input level and this attenuated level is applied to voltage comparators U207A and U207B. Resistors R214, R215, and R229 form a voltage divider with taps that provide a +0.7 V d-c voltage reference to comparator U207A and -0.7V d-c voltage reference to comparator U207B. If the ANT. SPEED input equals or exceeds 1.8V dc (representing an antenna speed of at least 1.8 rpm over the nominal speed of 900 rpm), the output of the attenuator exceeds the +0.7V reference level to voltage comparator U207A and the output of

U207A becomes a logical 1. LED driver Q201 conducts and the ANT. SPEED OVER signal is a logical 0. This logical 0 causes the ANT. SPEED ±1.8 RPM OVER indicator on the Panel Unit to illuminate. If the ANT. SPEED input equals or exceeds -1.8 Vdc (representing an antenna speed of at least 1.8 rpm less than the nominal speed of 900 rpm), the output of the attenuator exceeds the -0.7 V reference level to voltage comparator U207B, and the output of U207B becomes a logical 1. LED driver Q206 conducts and the ANT. SPEED UNDER signal is a logical 0. This logical 0 causes the ANT. SPEED ±1.8 RPM UNDER indicator on the Panel Unit to illuminate. As long as the ANT. SPEED signal is 0 ±1.8 V dc (representing an antenna speed of 900 ±1.8 rpm), the ANT. SPEED OVER and ANT. SPEED UNDER output signals are both high since LED drivers Q201 and Q206 are both cut off. The ANT. SPEED ±1.8 RPM UNDER and OVER indicators are extinguished.

(b) The ±2° GATE and PULSE PAIRS BUFFERED signal outputs of the Digital Bearing Unit are applied to the squitter rate analyzing circuit along with the 0.2° CD signal (0.2-degree clock pulse) from the Signal Processor card. The squitter rate analyzing circuit consists of a clocked one-shot comprised of flip-flops U213B and U213A and NAND gate U214A, and a time-to-voltage converter circuit consisting of transistors Q215, Q214, integrated circuit U209B, resistors U212B, U212A, R224, R218, R219, and R201, and capacitor C202. The initial state of the clocked one-shot is a logical 0 level at the 1 output of flip-flop U213A as a result of being triggered after a logical 0 output of NAND gate U214A sets flip-flop U213B. The leading edge of the first PULSE PAIRS BUFFERED pulse (after a double inversion by U214D and U214B) clears flip-flop U213B provided the ±2° GATE signal is a logical 0. (A logical 1 ±2° GATE signal inhibits the operation of the squitter analyzing circuit during the time that MRG's and ARG's are being received and processed.) Since the data (D) input to flip-flop U213A is a logical 1 when flip-flop U213B is cleared, then flip-flop U213A is set by the first positive-going transition of the 0.2° CD signal. The logical 0 output of NAND gate U214A sets flip-flop U213B thus the data input to flip-flop U213A is at a logical 0 level. The second positive-going transition of the 0.2° CD signal

clears flip-flop U213A. In summation, for each PULSE PAIRS BUFFERED pulse received, the output of flip-flop U213A becomes a logical 1 for approximately 37.5 microseconds. The 37.5-microsecond time duration is established by the nominal time duration between positive-going transitions of the 0.2° CD signal. The logical 1 output pulse of flip-flop U213A is coupled through and translated to a 37.5-microsecond negative pulse, -14.8V in amplitude by Q215 and Q214. The voltage output of U209B is 10V when the squitter rate is 2700 pulse pairs per second. The voltage output of U209B is established as follows:

$$Eo = (14.8)\left(\frac{R218 + R201}{R224}\right)(\text{Duty Cycle})$$

where duty cycle equal the logical 1 output time period of flip-flop U213A divided by the logical 0 output time period of this output (excluding the disable time period of the circuit when the ±2° GATE is at a logical 1 level).

(c) The output of U209B (SQUITTER RATE ANALOG signal) is provided to an attenuator consisting of resistors R202 and R203. The attenuator output is approximately 40 percent of the d-c input level and this attenuated level is applied to voltage comparators U203A and U203B. Resistors R212 and R209 form a voltage divider with a tap that provides a 4.2V d-c voltage reference to comparator U203A. If the TACAN squitter rate or DME squitter rate exceeds 2835 pulse groups per second, the output of U209B exceeds +10.5V and the output of the attenuator exceeds the 4.2V reference to U203A. The output of U203A becomes a logical 1, LED driver Q203 conducts, The SQUITTER RATE OVER signal becomes a logical 0, and the SQUITTER RATE ±5% OVER indicator on the Panel Unit illuminates. If the TACAN squitter rate falls below 2565 pulse pairs per second, the voltage output of U209B drops below +9.5V. The output of the attenuator (R202/R203) drops below the 3.8V d-c reference level established by resistors R210 and R208 and applied to comparator U203B. The output of U203B becomes a logical 1, LED driver Q208 conducts, the SQUITTER RATE UNDER signal becomes a logical 0, and the SQUITTER RATE ±5% UNDER indicator on the Panel Unit illuminates. As long as the TACAN squitter rate is

2700 ±135 pulse pairs per second, the output of U209B is between 9.5 and 10.5V dc, the output of the double-limit voltage comparators U203A and U203B are logical 0's, LED drivers Q203 and Q208 are cut off, and the SQUITTER RATE OVER and SQUITTER RATE UNDER output signals are high. The SQUITTER RATE ±5% UNDER and OVER indicators remain extinguished. When the SQUITTER switch on the Panel Unit is in the DME position, the 1 = DME signal input to card 200 is a logical 1. Transistor Q209 conducts and resistor R206 is in parallel to ground with resistor R208. The reference voltage level to comparator U203B is changed from 3.8V to 1.0V. The output of U209B is equal to or drops below +2.6V if the DME squitter rate drops below 700 pulse pairs per second. When this happens, the output of comparator U203B becomes a logical 1, LED driver Q208 conducts, the SQUITTER RATE UNDER line becomes a logical 0, and the SQUITTER RATE ±5% UNDER indicator on the Panel Unit illuminates. The SQUITTER RATE ANALOG output of U209B is provided to recording equipment and to the PERCENT meter via the PERCENT switch.

(d) The PHASE COHER signal output of the Signal Processor card is applied to recording equipment, to the PHASE COHERENCY DEGREES meter, and to an attenuator consisting of resistors R230 and R231. The output of this attenuator is applied to the double-limit detector consisting of comparators U208A and U208B, and resistors R216, R217, and R232. The reference voltage levels to these comparators is +1.0V (for U208A) and -1.0V (for U208B). The attenuator output is approximately 40 percent of the PHASE COHER d-c input level. As long as the PHASE COHER signal is between +2.5V and -2.5V level (representing a phase coherency of ±5 degrees), the output of U208A and U208B are logical 0's, LED drivers Q207 and Q202 are cut off, and the PHASE COHERENCY ±5° OVER and UNDER indicators on the Panel Unit remain extinguished. If the PHASE COHER signal equals or exceeds +2.5V, the output of comparator U208A is a logical 1, LED driver Q207 conducts, and the PHASE COHER ±5° OVER indicator illuminates. If the PHASE COHER signal equals or is more negative than -2.5V, the output of comparator U208B is a logical 1, LED driver Q202 conducts, the PHASE COHER UNDER signal becomes a logical 0, and the PHASE COHER ±5° UNDER indicator illuminates.

(e) The CMRG output of NAND gate U314C (on the Signal Processor card) is applied to the trigger input of a 4-bit binary counter U216. The ZERO ±2° GATE input signal is also applied to one reset input of U216. The second reset input of U216 receives the RESET output of the Signal Processor card. When the logical 1 ZERO ±2° GATE occurs, the RESET pulse (0.1 degree in width and occurring essentially concurrent with the leading edge of the ZERO ±2° GATE pulse) resets the 4-bit binary counter U216 to the all 0 state. This counter now counts the number of CMRG pulses occurring for each MRG decoded (X or Y mode) in the Digital Bearing Unit. A properly decoded MRG pulse group is represented by a pulse train of 11 (X mode operation) or 12 (Y mode operation) CMRG pulses occurring within each ZERO ±2° GATE pulse. The count is stored until the next RESET pulse occurs. The 1 = Y MODE signal from the DME is applied to inverter U214C and to pin 14 of U215, the B2 input. The output of inverter U214C is applied to pins 11 and 9 of U215. The outputs of the 4-bit binary counter U216 are applied to a 4-bit magnitude comparator U215. If the count in U216 is 11 (for X mode operation) or 12 (for Y mode operation) ±85 percent, and remains within this tolerance consistantly, then the output of U215 at the non-inverting input of comparator U210A remains below this comparators threshold level, and the output of U215 at the non-inverting input of comparator U210B is also below the threshold level of U210B. Resistor pairs R233-R220 and R234-R221 establishes the reference voltage level inputs to comparators U210A and U210B at 4.5V. If the CMRG inputs represent the correct MRG size, the outputs of U215 are both logical 0's, the outputs of comparators U210A and U210B are logical 0's, LED drivers Q211 and Q204 are cut off, the MRG SIZE OVER and MRG SIZE UNDER signals are high, and the MRG SIZE OVER and UNDER indicators on the Panel Unit remain extinguish. If the MRGCK input to NAND gate U314C represents an oversize MRG pulse group for greater 15 percent of the time, the signal on the non-inverting input of U210A exceeds the 4.5V threshold level, the output of U210A is a logical 1, LED driver Q211 conducts, the MRG SIZE OVER output signal becomes a logical 0, and the MRG SIZE OVER indicator illuminates. In a like manner, an undersize MRG pulse group results in logical 1 output from pin 7 of U215 and the MRG SIZE UNDER indicator illuminates.

(f) The CARG output of NAND gate U314B (on the Signal Processor card) is applied to the trigger input of a 4-bit binary counter U218. The operation of the ARG size analysis circuit consisting of NAND gate U314B 4-bit binary counter U218, 4-bit magnitude comparator U217, comparators U211A and U211B, and LED drivers U212 and U205 is similar in operation to the MRG size analysis circuit described in paragraph 2 F (2) (e). A properly decoded ARG pulse group is represented by a pulse train of 10 (X mode operation) or 11 (Y mode operation) ARGCK pulses occurring within each ARGG pulse. The ARG SIZE UNDER and OVER output signals control operation of the ARG SIZE UNDER and OVER indicators on the Panel Unit.

(g) The ARGEV (auxiliary reference group event) signal output of the Digital Bearing Unit is applied to a event-to-voltage converter consisting of transistors Q216 and Q213; resistors U212D, U212C, R213, R207, and R211; capacitor C201, and integrated circuit U209A. Resistors R205 and R204 establish the voltage reference to the non-inverting input of comparator U204B at +4.6 volts. When the number of ARG's decoded by the Digital Bearing Unit during an antenna revolution time period (67 ms) is eight (eight ARGEV pulses received every antenna revolution), the output voltage of U209A exceeds the 4.6-volt reference level, the output of the voltage comparator U204B is a logical 0, LED driver Q210 is cut off, and the ARG COUNT UNDER indicator on the Panel Unit is extinguished. If the number of ARG's decoded during one antenna revolution time period is less than eight (less than eight ARGEV pulses received in 67 milliseconds), then the output of U209A is less than the 4.6-volt reference level to U204B, the output of comparator U204B is a logical 1, LED driver Q210 conducts, the ARG COUNT UNDER signal is a logical 0, and the ARG COUNT UNDER indicator on the Panel Unit illuminates.

NOTE: Following paragraphs (h) through (l) apply only to a 7124-1110-2 Limit Detector card.

(h) The ANT. SPEED input signal is applied directly to the non-inverting input of comparator U207A and to the inverting input of comparator U207B (see figure 925). The ANT. SPEED signal is an analog voltage having a

range of ±10V dc corresponding to an antenna speed range of 890 to 910 rpm. Resistors, R214, R215, and R229 form a voltage divider with taps that provide a +1.8V d-c voltage reference to comparator U207A and a -1.8V d-c voltage reference to comparator U207B. If the ANT. SPEED input equals or exceeds 1.8V dc (representing an antenna speed of at least 1.8 rpm over the nominal speed of 900 rpm), the output of U207A becomes a logical 1, LED driver Q201 conducts, and the ANT. SPEED OVER signal is a logical 0. This logical 0 causes the ANT. SPEED ±1.8 RPM OVER indicator on the Panel Unit to illuminate. If the ANT. SPEED input equals or exceeds -1.8 Vdc (representing an antenna speed of at least 1.8 rpm less than the nominal speed of 900 rpm), the output of U207B becomes a logical 1, LED driver Q206 conducts, and the ANT. SPEED UNDER signal is a logical 0. This logical 0 causes the ANT. SPEED ±1.8 RPM UNDER indicator on the Panel Unit to illuminate. As long as the ANT. SPEED signal is 0 ±1.8 V dc (representing an antenna speed of 900 ±1.8 rpm), the ANT. SPEED OVER and ANT. SPEED UNDER output signals are both high since LED drivers Q201 and Q206 are both cut off. The ANT. SPEED ±1.8 RPM UNDER and OVER indicators are extinguished.

(i) The theory given in paragraph 2 F (2) (b) is also applicable for a 7124-1110-2 card.

(j) The output of U209B (SQUITTER RATE ANALOG signal) is provided to the non-inverting input of comparator U203A and to the inverting input of U203B. Resistors R212 and R209 form a voltage divider with a tap that provides a 10.5V d-c voltage reference to comparator U203A. If the TACAN squitter rate or DME squitter rate exceeds 2835 pulse groups per second, the output of U209B exceeds the +10.5V reference to U203A. The output of U203A becomes a logical 1, LED driver Q203 conducts, the SQUITTER RATE OVER signal becomes a logical 0, and the SQUITTER RATE ±5% OVER indicator on the Panel Unit illuminates. If the TACAN squitter rate falls below 2565 pulse pairs per second, the voltage output of U209B drops below the +9.5V voltage reference level established by resistors R210 and R208 and applied to comparator U203B. The output of U203B becomes a logical 1, LED driver Q208 conducts, the SQUITTER

RATE UNDER signal becomes a logical 0, and the SQUITTER RATE ±5% UNDER indicator on the Panel Unit illuminates. As long as the TACAN squitter rate is 2700 ±135 pulse pairs per second, the output of U209B is between 9.5 and 10.5V dc, the output of the double-limit voltage comparators U203A and U203B are logical 0's. LED drivers Q203 and Q208 are cut off, and the SQUITTER RATE OVER and SQUITTER RATE UNDER output signals are high. The SQUITTER RATE ±5% UNDER and OVER indicators remain extinguished. When the SQUITTER switch on the Panel Unit is in the DME position, the 1 = DME signal input to card 200 is a logical 1. Transistor Q209 conducts and resistor R206 is in parallel to ground with resistor R208. The reference voltage level to comparator U203B is changed from 9.5V to 2.6V. The output of U209B is equal to or drops below +2.6V if the DME squitter rate drops below 700 pulse pairs per second. When this happens, the output of comparator U203B becomes a logical 1, LED driver Q208 conducts, the SQUITTER RATE UNDER line becomes a logical 0, and the SQUITTER RATE ±5% UNDER indicator on the Panel Unit illuminates. The SQUITTER RATE ANALOG output of U209B is provided to recording equipment and to the PERCENT meter via the PERCENT switch.

(k) The PHASE COHER signal output of the Signal Processor card is applied to recording equipment, to the PHASE COHERENCY DEGREES meter, and to a double-limit threshold detector consisting of comparators U208A and U208B, and resistors R216, R217, and R232. The reference voltage levels to these comparators is +2.5V (for U208A) and -2.5V (for U208B). As long as the PHASE COHER signal is between +2.5V and -2.5V level (representing a phase coherency of ±5 degrees), the output of U208A and U208B are logical 0's, LED drivers Q207 and Q202 are cut off, and the PHASE COHERENCY ±5° OVER and UNDER indicators on the Panel Unit remain extinguished. If the PHASE COHER signal equals or exceeds +2.5V, the output of comparator U208A is a logical 1, LED driver Q207 conducts, and the PHASE COHER ±5° OVER indicator illuminates. If the PHASE COHER signal equals or is more negative than -2.5V, the output of comparator U208B is a logical 1, LED driver Q202 conducts, the PHASE COHER UNDER signal becomes a logical 0, and the PHASE COHER ±5° UNDER indicator illuminates.

(1) The theory given in paragraphs 2 F(2) (e), 2 F (2) (f), 2 F (2) (g) is also applicable for a 7124-1110-2 card.

(3) Power Supply Regulator Card (100)

The Power Supply Regulator card provides the Signal Analyzer Unit with the following voltages:

1. +20V dc and -20V dc unregulated
2. +15V dc and -15V dc regulated
3. +5.7V dc regulated

This card operates identically to the Power Supply Regulator card used in the Digital Bearing Unit (refer to paragraph 2 D (6)) except that +15V and -15V outputs are provided in the regulator card on the Signal Analyzer Unit. To obtain +15V and -15V instead of +12V and -12V, the values of resistors R105, R109, and R104 are changed. See figure 923.

(4) Main Frame Mounted Power Supply Circuit Components

The components mounted on the main frame are identical to those on the main frame of the Digital Bearing Unit (refer to paragraph 2 D (7)). The reference designation of the Signal Analyzer Unit are in the 7300 series rather than the 7200 series.

G. Console Display and Control Panel Unit General Theory

(1) The Console Display and Control Panel Unit (Panel Unit) provides the means to control and monitor the ground beacon signal analysis circuitry. The test set-to-ground beacon range and bearing information is displayed on the Panel Unit. Most of the functions on the panel are self explanatory and are discussed in detail in the applicable theory paragraphs. Test set operation is activated when the POWER switch is set to the ON position.

(2) The RANGE NAUTICAL MILES indicators (LEDS) are controlled by the SERIAL BCD CLOCK, SERIAL BCD DIST DATA, SERIAL BCD WORD SYNC, 27.5V DC FLAG ALARM and MANUAL STANDBY signals from the DME. See figure 9. If the test set is in standby mode or has failed, then the MANUAL STANDBY or 27.5V DC FLAG ALARM signal, as applicable, causes the selector control circuit to produce a SELECT signal level that

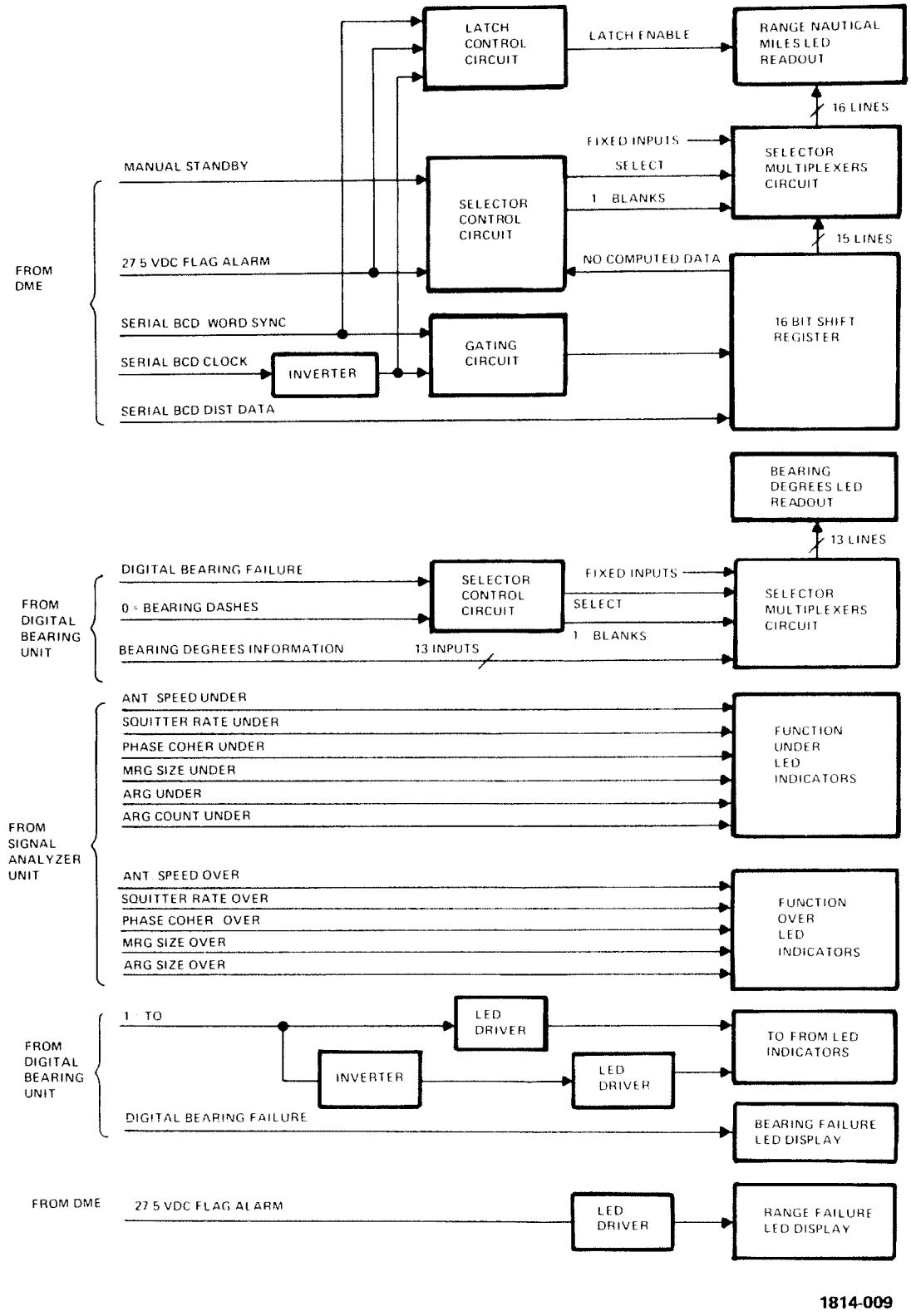

Figure 9. Console Display and Control Panel Unit Block Diagram

couples the fixed inputs and a logical one 1 = BLANKS input signal through the selector multiplexers circuit thus the RANGE NAUTICAL MILES readout is blank. If the "no computed data bit" of the SERIAL BCD DIST DATA signal indicates that the DME has not computed data, then the fixed inputs and a logical 0 1 = BLANKS input are gated through the selector multiplexers circuit and the RANGE NAUTICAL MILES readout displays dashes. The SERIAL BCD WORD SYNC pulse gates the SERIAL BCD CLOCK pulses through a gating circuit thus allowing the SERIAL BCD DIST DATA signal to be loaded into the 16-bit shift register. If data has been computed, the output of the 16-bit shift register is coupled through the selector multiplexers circuit and the RANGE NAUTICAL MILES indicator displays miles to beacon (up to 399.9 nautical miles). The latch control circuit output provides the LATCH ENABLE signal that permits the LEDS to retain previous input data when the LATCH ENABLE signal is high, and loads in new data when the LATCH ENABLE signal is low. The LATCH ENABLE signal is low for one-clock period after the SERIAL BCD WORD SYNC pulse returns to a low level.

(3) The BEARING DEGREES indicators (LEDS) are controlled by the 13 bearing degree information inputs, DIGITAL BEARING FAILURE, and 0 = BEARING DASHES signals from the Digital Bearing Unit. If the DIGITAL BEARING FAILURE and 0 = BEARING DASHES input signals are high, the 13 bearing information inputs are coupled through the selector multiplexers circuits and displayed on the BEARING DEGREES indicators. If the DIGITAL BEARING FAILURE signal is low representing a failure in the Digital Bearing Unit, the selector control circuit provides a SELECT signal that causes the fixed inputs and a logical 1 1 = BLANKS input to be gated through the selector multiplexers circuit thus causing the BEARING DEGREES indicator to become blank. If the 0 = BEARING DASHES signal is low (representing no computed bearing data), then the fixed inputs and a logical 0 1 = BLANKS signal is coupled through the selector multiplexers circuit causing the BEARING DEGREES indicator to display all dashes. The 1 = TO signal from the Digital Bearing Unit is provided to an inverter and LED driver. This signal causes either the TO or FROM indicator (LED) to illuminate.

(4) Six FUNCTION UNDER indicators (LEDS) receive signals from the Signal Analyzer Unit. A logical 0 on any of these six inputs causes the applicable FUNCTION UNDER indicator to illuminate.

Five FUNCTION OVER indicators (LEDS) also receive signals from the Signal Analyzer Unit. A logical 0 on any of these five lines causes the applicable FUNCTION OVER indicator to illuminate.

(5) The COURSE SELECT DEGREES control consists of three thumbwheel switches that provide 10 signals that contain the reference bearing information to the Digital Bearing Unit for computation of bearing deviation. The COURSE SELECT DEGREES control operates in conjunction with the OBS CONTROL. The 10 signals contain bearing information only when the OBS CONTROL is set to the MAN position. When the OBS CONTROL is set in the AUTO position, the 1 = MANUAL signal and the COURSE SELECT DEGREES control output signals are at a logical 0 level.

(6) In the event of a Digital Bearing Unit failure, the DIGITAL BEARING FAILURE input signal causes the BEARING FAILURE indicator to illuminate. If the DME fails, the 27.5V DC FLAG ALARM signal causes the RANGE FAILURE indicator to illuminate.

H. Console Display and Control Panel Unit Detailed Theory

The detail theory for the Console Display and Control Panel Unit is subdivided into the functional circuits as follows:

1. Range Indicating Circuit
2. Bearing Indicating Circuit
3. LED Control Circuits
4. Switch Circuits
5. Power Circuits

The detailed theory for these circuits is given in following paragraphs (1) through (5).

(1) Range Indicating Circuit

The components that form the range indicating circuit are located on the LED Display card (100) and LED Logic card (200). Figure 10 illustrates the circuit and the component reference designation identifies the card upon which the component is located; i.e., a reference designation in the 100

series is located on the LED Display card, and one in the 200 series is located on the LED Logic card.

(a) The SERIAL BCD DIST DATA, SERIAL BCD WORD SYNC, and SERIAL BCD CLOCK inputs to the Panel Unit are generated in the DME. The high level of these signals is +12 +3/-0.2V and the low level is 0 ±1V. The description of the generation of these signals is contained in the Maintenance and Overhaul Manual for the KDM 7000 Digital DME. The SERIAL BCD CLOCK input is in the form of a square wave with a frequency of 11 ±3.5 KHz. The SERIAL BCD CLOCK input is applied continuously and the SERIAL BCD DIST DATA and SERIAL BCD WORD SYNC inputs are synchronous with it.

(b) Since logic levels of the three aforementioned inputs are not compatible with the logic levels required for proper operation of the Panel Unit, resistor pairs R108-R109 (for SERIAL BCD DIST DATA input), R202-R115 (for SERIAL BCD WORD SYNC input), and R203-R114 (for SERIAL BCD CLOCK input) divide the voltage levels down to those required for the Panel Unit logic circuits. The SERIAL BCD CLOCK input is applied to NAND gate U204A via inverter U203E. When the SERIAL BCD WORD SYNC input to NAND gate U204A is high, the SERIAL BCD CLOCK signal is applied to the 16-bit shift register consisting of two 8-bit shift registers (U123 and U129) connected in series. The SERIAL BCD DIST DATA is then loaded into the registers. When the SERIAL BCD WORD SYNC input changes to a low level, NAND gate U204A is inhibited, the SERIAL BCD CLOCK is removed and the last 16 bits of the SERIAL BCD DIST DATA word are stored in the shift register. The parallel outputs of the shift register are applied to four quadruple 2-input data selector/multiplexers (U111, U112, U115, and U116). The parallel outputs X1, X2, X4, and X8 of U111, U112, U115, and U116 are provided in BCD form to their applicable LED displays U101, U102, U103, and U104. These LED displays are identified on the front panel as RANGE NAUTICAL MILES. When the LATCH ENABLE output of NAND gate U204B goes to a logical 0, the RANGE NAUTICAL MILES readout stores and displays the range to beacon as represented by the BCD input to each LED display.

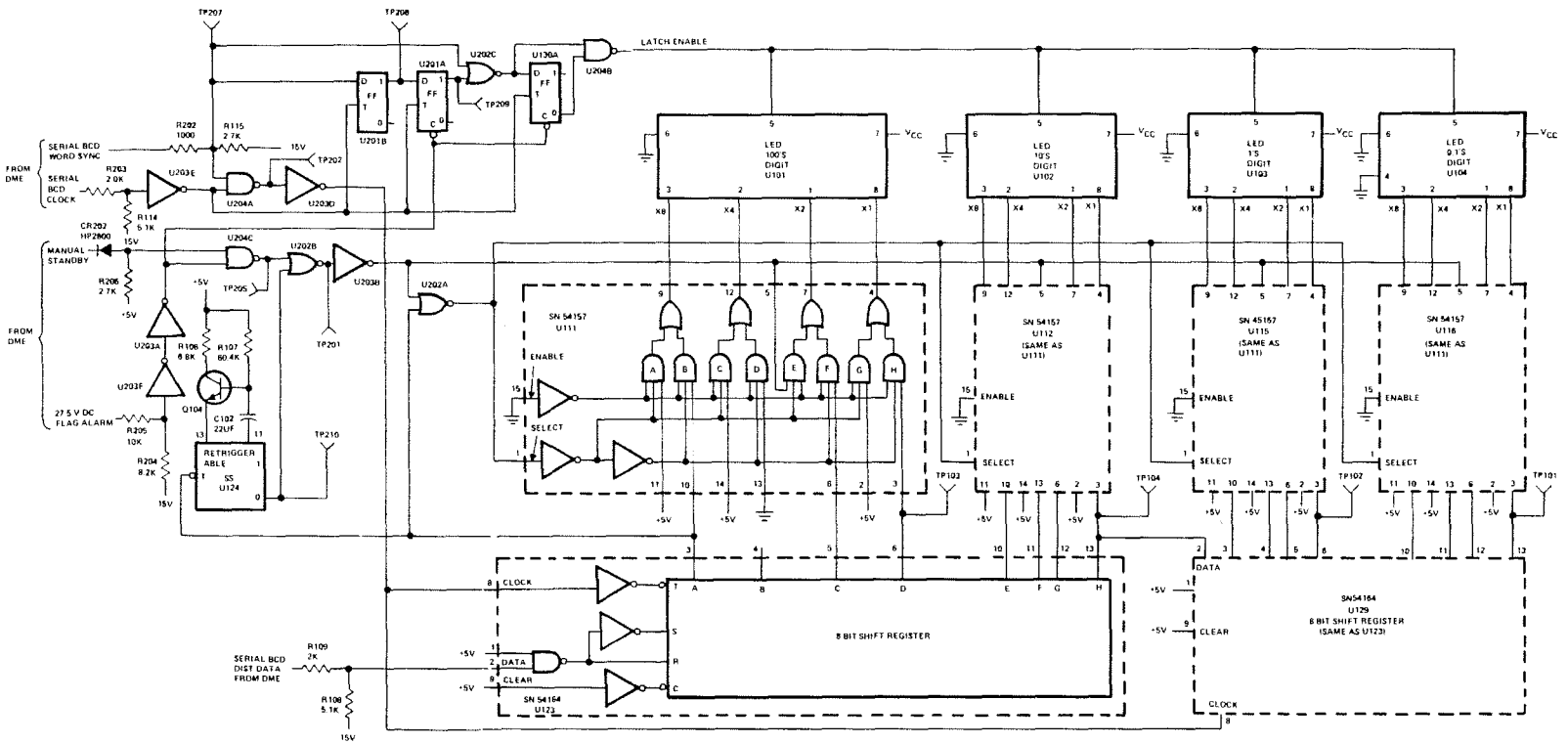

Figure 10. Range Indicating Circuit Simplified Schematic Diagram

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(c) An additional circuit consisting of NAND gate U204C; a retriggerable single shot comprised of U124, Q104, R106, R107, and C102; NOR gates U202B and U202A; and inverter U203B controls the selection performed by U111, U112, U115, and U116. When the MANUAL STANDBY and 27.5V DC FLAG ALARM input signals from the DME are at a high level, both inputs to NAND gate U204C are at a logical 1 level and the output of U204C is a logical 0. The output of NOR gate U202B is then dependent upon the operation of the retriggerable single shot. The first and eighth bit of the SERIAL BCD DIST DATA word, the DME label, are at a high level. As these bits are driven through the 16-bit shift register, the retriggerable single shot U124 is triggered resulting in a logical 0 from the 0 output. Resistor R107 and capacitor C102 determines that the period of U124 is approximately 350 milliseconds in duation. For each pulse applied, the duration is extended an additional 350 milliseconds. The logical 0 output of single shot U124 is applied to NOR gate U202B. The logical 1 output of U202B is inverted by U203B and applied to NOR gate U202A. When the last 16 bits of the 32-bit SERIAL BCD DIST DATA word is loaded into 16-bit shift register, and the "no computed data bit" (the 32nd bit of the DATA word) is a logical 0 (indicating that data was computed in the DME), then both inputs to NOR gate U202A are logical 0's and the output of U202A is a logical 1. This logical 1 is provided as the SELECT input (pin 1) to U111, U112, U115, and U116. When the SELECT input is a logical 1, gates A, C, E, and G of U111; and similar gates of U112, U115, and U116 are inhibited. Gates B, D, F, and H of U111 and similar gates of U112, U115, and U116 are enabled. The outputs of the 16-bit shift register are coupled through U111, U112, U115, and U116 and applied to the associated digit of the LED display.

(d) If the "no computed data bit" is at a high level (indicating that the DME computed no data), then the resulting logical 1 on the A output of U123 (pin 3) is coupled through NOR gate U202A resulting in a logical 0 SELECT input to U111, U112, U115, and U116. Gates A, C, E, and G of U111 and similar gates of U112, U115, and U116 are enabled. The +5V applied to pins 11, 14, and 2 of U111, U112, U115, and U116 determines that the X8, X4, and X1 output of these circuits are at a logical 1 level. The

X2 output of U111, U112, U115, and U116 depends upon the logic level applied to pin 5 of these circuits. The input to pin 5 of these circuits is obtained from inverter U203B. If the first and eighth bits of the SERIAL BCD DIST DATA word were high, then single shot U124 is triggered and a logical 0 is applied to NOR gate U202B. If the MANUAL STANDBY and 27.5V DC FLAG ALARM signals are high, then the second input to NOR gate U202B is a logical 0. The output of inverter U203B is a logical 0 and the X2 outputs of U111, U112, U115, and U116 are logical 0's. When the X1, X4, and X8 outputs of U111, U112, U115, and U116 are logical 1's, and the X2 output is a logical 0, each digit displays a dash (—). Dashes on each RANGE NAUTICAL MILES digit indicates the absence of computed data.

(e) When the test set is operating in the Standby mode (MANUAL STANDBY signal at a low level) or if there is a failure (27.5V DC FLAT ALARM signal at a low level), then the output of NAND gate U204C is a logical 1. This logical 1 results in a logical 1 output of inverter U203B and a logical 0 output of NOR gate U202A. The SELECT signal input to U111, U112, U115, and U116 is a logical 0. Gates A, C, E, and G are enabled. The X1, X2, X4, and X8 outputs of U111, U112, U115, and U116 are logical 1's. The RANGE NAUTICAL MILES display is blank indicating Standby mode or DME failure.

(f) A circuit consisting of flip-flops U130A, U201A, and U201B; NAND gate U204B; and NOR gate U202C generates the LATCH ENABLE signal to LED displays U101 through U104. When the SERIAL BCD WORD SYNC signal is low, flip-flops U201A, U201B, and U130A are in their initial state. The clock output of inverter U203E is always occurring therefore U201A and U201B are in the clear state. Since the SYNC signal is low and flip-flop U201A is in the clear state, the output of NOR gate U202C is a logical 1 and flip-flop U130A is in the set state. The logical 0 from the 0 output of flip-flop U130A is applied to NAND gate U204B thus the LATCH ENABLE signal is at a logical 1 level. When the LATCH ENABLE signal is a logical 1, the range data is held in memory by the LED displays U101 through U104. When the SERIAL BCD WORD SYNC input signal goes high, the data (D) input to flip-flop U201B is at a logical 1 level. The SERIAL BCD

WORD SYNC input signal is applied to NOR gate U202C thus the data (D) input to flip-flop U130A is at a logical 0 level. The first positive-going clock output from inverter U203E sets flip-flop U201B and clears U130A. The LATCH ENABLE signal still remains at a logical 1 level as a result of the logical 0 output of NOR gate U202C. The second positive-going transition output of inverter U203E to occur after the SERIAL BCD WORD SYNC signal goes high sets flip-flop U201A. The logical 1 from the 1 output of U201A is applied to NOR gate U202C. The resulting logical 0 output of U202C assures that the LATCH ENABLE output of NAND gate U204B remains at a logical 1 level even when the SERIAL BCD WORD SYNC signal momentarily changes to a low level during data bit number 8.

(g) When the SERIAL BCD WORD SYNC signal reverts to a low level at the end of the data message, the data (D) input to flip-flop U201B becomes a logical 0 and the next positive-going transition from inverter U203E clears U201B. One clock period later, flip-flop U201A is cleared by the output of U203E. When U201A is cleared, both inputs to NOR gate U202C are logical 0's and the output is a logical 1. Both inputs to NAND gate U204B are now logical 1's and the LATCH ENABLE signal becomes a logical 0. One clock period later, flip-flop U130A is set by the output of U203E since the data (D) input is at a logical 1 level. The LATCH ENABLE signal becomes a logical 1. The three flip-flops are now in their initial state.

(h) In summation, the LATCH ENABLE signal becomes a logical 0 for 1-clock period (approximately 100 microseconds) starting one and one-half clock periods after the SERIAL BCD WORD SYNC pulse changes to a low level at the end of the data message. The logical 0 LATCH ENABLE pulse loads the updated range data into the RANGE NAUTICAL MILES display U101 through U104. This control circuit prevents the LED displays from blinking as new range data is shifted through the two 8-bit shift registers.

(2) Bearing Indicating Circuit

The components that form the bearing indicating circuit are located on the LED Display card (100) and LED Logic card (200). Figure 11 illustrates the circuit, and the component reference designation identifies the card upon which the component is located; i.e., a reference designation in the 100 series is located on the LED Display card, and one in the 200 series is located on the LED Logic card.

(a) The bearing indicating circuit consists of a display circuit and a control circuit. The display circuit consists of four quadruple 2-input data selector/multiplexers U117, U118, U121, and U122; and four LED displays U107 through U110. The LED displays are identified as BEARING DEGREES on the Panel Unit. The control circuit consists of resistors R201, R207, and R208; inverter U203C; NAND gate 204D; and NOR gate U202D. The control circuit determines the logic level of the inputs on pin 1 (SELECT) and pin 5 of U117, U118, U121, and U122. When the SELECT input is a logical 1, gates A, C, E, and G of U117 are inhibited and gates B, D, F, and H are enabled. Similar gates of U118, U121 and U122 are enabled and/or inhibited in a like manner. The signals levels on the digital bearing inputs from the Digital Bearing Unit are coupled through U117, U118, U121, and U122 and applied to the LED displays U107 through U110. Pins 10 and 13 of U117 are grounded thus the X4 and X8 outputs of U117 are normally logical 0's. The 100's digit LED display U107 can therefore display only a 0, 1, 2, or 3 since the parallel X1, X2, X4, and X8 signals are in binary coded decimal form with the X4 and X8 signals held at a logical 0 level. Pin 3 of U122 is grounded therefore the X1 output is a logical 0. The 0.1 digit LED display U110 can only display the even numerals 2, 4, 6, and 8. The ground applied to pin 4 of LED display U110 causes the decimal point of U110 to illuminate. Since the 10's and 1's digits LED display U108 and U109 respectively can indicate the numerals 0 through 9, then bearing information from 0 to 359.8 degrees in 0.2-degree increments can be displayed on the BEARING DEGREES indicator.

(b) When the 0 = BEARING DASHES input signal from the Digital Bearing Unit is a logical 0, the output of inverter U203C is a logical 1. The logical 1 output of U203C is

applied to NOR gate U202D and the SELECT signal on pin 1 of U117, U118, U121, and U122 is a logical 0. Gates A, C, E, and G of U117, U118, U121, and U122 are enabled and gates B, D, F, and H are inhibited. The X8, X4, and X1 outputs of U117, U118, U121, and U122 are logical 1's since pins 11, 14, and 2 of each of these circuits is connected to +5V. The X2 output of these circuits depends upon the output of NAND gate U204D. If the DIGITAL BEARING FAILURE input to NAND gate U204D is logical 1, then the output of U204D is a logical 0 and the X2 outputs of U117, U118, U121, and U122 are a logical 0. When the X8, X4, X2, and X1 signals are a 1, 1, 0, 1 respectively, a dash is displayed on each of the LED displays U107 through U108. This represents an operating test set with no computed data in the Digital Bearing Unit (0 = BEARING DASHES signal a logical 0 level and DIGITAL BEARING FAILURE signal a logical 1 level). When the DIGITAL BEARING FAILURE signal is a logical 0, the output of U204D is a logical 1. The output of NOR gate U202D is a logical 0. The X1, X2, X4, and X8 are all logical 1's since the input at pins 11, 14, 5, and 2 of U117, U118, U121, and U122 is a logical 1.

(3) LED Control Circuits

(a) The logical 0 output of inverter U203A (see figure 10) occurring when the 27.5V DC FLAG ALARM signal is at a low level clears flip-flops U201A and U130A. When the 27.5V DC FLAG ALARM signal is low, the SERIAL BCD WORD SYNC and SERIAL BCD CLOCK input signals are inhibited and assume a logical 0 level. Both inputs to NOR gate U202C are logical 0's therefore, the output to NAND gate U204B is a logical 1. Since flip-flop U130A is in the clear state, the LATCH ENABLE signal becomes a logical 0 thus, the RANGE NAUTICAL MILES readout is changed from a digital readout to all blanks when the 27.5V DC FLAG ALARM signal drops to a low level indicating a failure. When the failure is corrected, flip-flops U201B, U201A, and U130A operate as previously described.

(b) A second LED control circuit consisting of transistor Q106 and Q107 provides control for the ANT. SPEED ±1.8 RPM OVER and UNDER indicators U120 and U114, PHASE COHER ±5° OVER and UNDER indicators U132 and U126, MRG SIZE OVER and UNDER indicators U133 and U127,

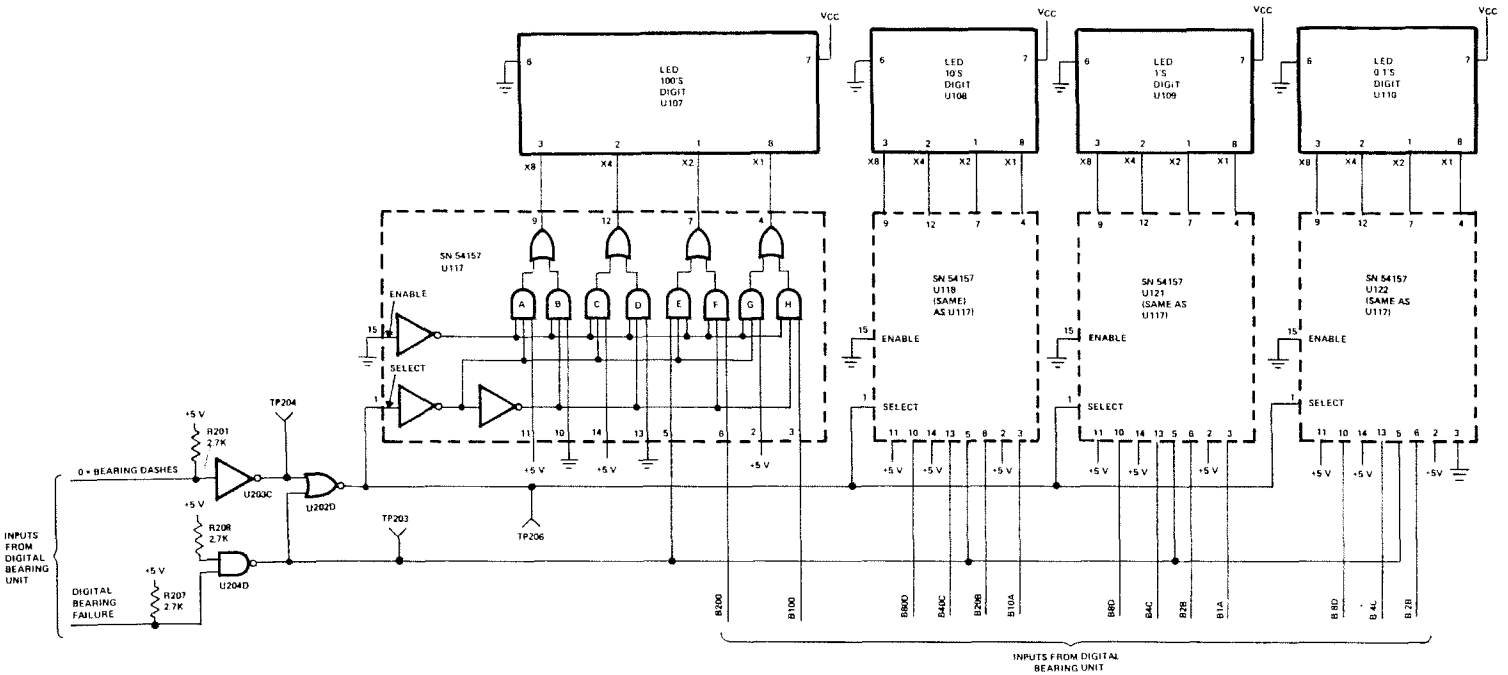

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Figure 11. Bearing Indicating Circuit Simplified Schematic Diagram

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ARG SIZE OVER and UNDER indicators U137 and U135, ARG COUNT UNDER indicator U136, and the TO and FROM indicators U105 and U106. See figure 928. The 0 = BEARING DASHES input signal is applied to the base of transistor Q106 via resistor R113. When this signal is at a logical 1 level indicating Digital Bearing Unit normal operation, transistor Q106 is cut off and transistor Q107 conducts. The anodes of the previously identified indicators are provided with +5V dc thus,the indicators will illuminate if the input signal to the cathode is a logical 0. All indicators identified in this paragraph have identical circuits except to the TO and FROM indicators U105 and U106. These indicators have a common input (1 = TO) and the input circuit is controlled by transistors Q101, Q102, and Q103. When the 1 = TO input is a logical 1, transistors Q101 and Q103 conduct and transistor Q102 is cut off. The TO indicator U105 illuminates. When the 1 = TO input is a logical 0, transistors Q101 and Q103 are cut off, transistor Q102 conducts, and the FROM indicator U106 illuminates.

(c) The 27.5V DC FLAG ALARM signal is applied to the base of transistor Q105 via resistor divider R110/R111. When this signal changes to a low level indicating a DME failure, transistor Q105 conducts and the RANGE FAILURE indicator U113 illuminates. If the DIGITAL BEARING FAILURE input signal is at a logical 0 level indicating a failure in the Digital Bearing Unit, the BEARING FAILURE indicator U119 illuminates.

(4) Switch Circuits

The switch circuits are shown on figure 12. The circuits for the BEARING switch S7404, OPERATE/CALIBRATE switch S7402, and SQUITTER switch S7403 are illustrated in figure 12. Pull-up resistors for obtaining the logical 1 level implied by the output signal names are located in the Signal Analyzer Unit (for 1 = DME signal) or Digital Bearing Unit (for 1 = 15 HZ ONLY and 0 = CALIBRATE). When the OBS CONTROL switch S7406 is in the MAN position, the 1 = MANUAL signal is open-circuited in the Panel Unit. The pull-up resistor for the logical 1 level is located in the Digital Bearing Unit. The second output from S7406 is also open-circuited. This allows the COURSE SELECT DEGREES thumbwheel switches to provide the selected bearing information on 10 lines to the Digital Bearing Unit.

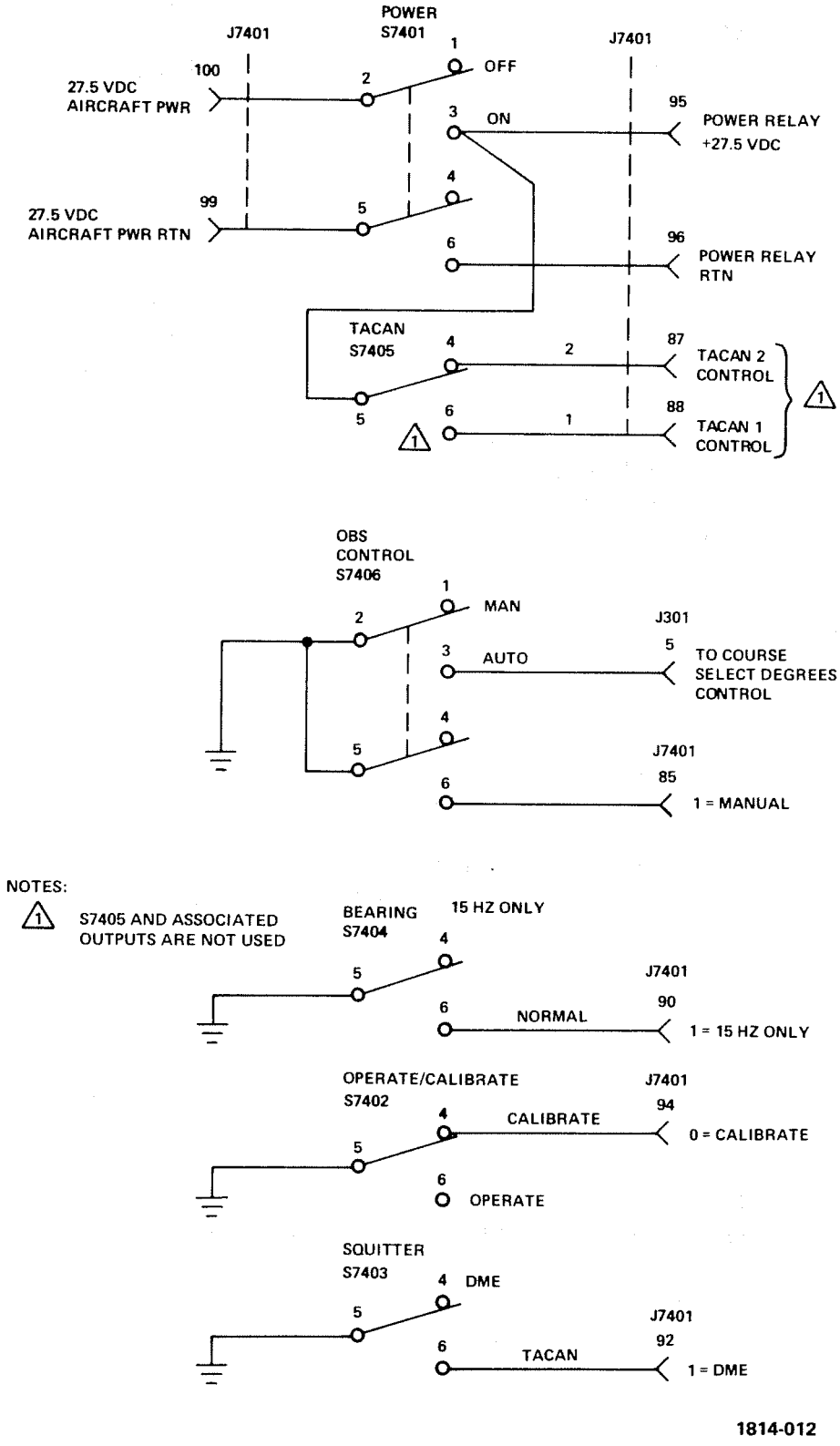

Figure 12. Switch Circuit Schematic Diagram

See figure 13 for a description of these outputs-versus-control position. When the OBS CONTROL switch S7406 is in the AUTO position, the 1 = MANUAL signal is at ground level, and a ground is also applied to the COURSE SELECT DEGREES thumbwheel switches. The 10 output lines of these thumbwheel switches are at ground level. Operation of the POWER switch S7401 is described in paragraphs 2 B (1) through 2 B (5).

(5) Power Circuits

The 115V 400 HZ is applied to the primary winding of transformer T7401 (see figure 927). One secondary winding of T7401 provides a nominal 5V ac to a full-wave bridge-type rectifier CR7401. The nominal +5V d-c output of CR7401 is applied to series regulator Q7401 and filter capacitor C7401. A second secondary winding provides a nominal 15V ac to a full-wave bridge-type rectifier CR7402. The nominal 15V d-c output of CR7402 is filtered by C7402 and applied to the operating circuits of the Panel Unit.

I CHANNEL/MODE Selector Detailed Theory

(1) The CHANNEL/MODE selector consists of a channel select card A7505 (see figure 930) and a thumbwheel switch S7506 (see figure 912). The CHANNEL/MODE selector permits the test set operator to select the desired frequency channel and either the X or Y operating mode. The operating frequency of the test set is determined by a 2 out of 5 ARINC code. The code is provided to the DME on 12 lines and is representative of the paired VHF navagational frequencies as given in Maintenance/Overhaul Manual KDM 7000 Digital DME. The signal outputs of card A7505 that control the operating frequency are identified as 10A SELECT, 10E SELECT, 1A through 1E SELECT (5 signals), and .1A through .1E SELECT (5 signals). These control lines are either at ground level or at a logical 1 level.

(2) The CHANNEL/MODE select switch S7506 plugs into connectors J2001, J2002, J2003, and J2004 on card A7505 (see figure 930). The units thumbwheel switch outputs are applied to connector J2004. Five of the outputs from the units switch are coupled to the DME via card A7505. These outputs are identified as .1A - .1E SELECT and are in the 2 out of 5 ARINC code format. The units switch has 10 positions identified as 0 through 9. The outputs from the switch versus the switch

COURSE SELECT DEGREES Position			Signal Names and Logic Levels									
			Hundreds Switch		10's Switch				Units Switch			
100's	10's	Units	T200	T100	T80D	T40C	T20B	T10A	T8D	T4C	T2B	T1A
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	1	0	0	0	1
2	2	2	1	0	0	0	1	0	0	0	1	0
3	3	3	1	1	0	0	1	1	0	0	1	1
0	4	4	0	0	0	1	0	0	0	1	0	0
1	5	5	0	1	0	1	0	1	0	1	0	1
2	6	6	1	0	0	1	1	0	0	1	1	0
3	7	7	1	1	0	1	1	1	0	1	1	1
0	8	8	0	0	1	0	0	0	1	0	0	0
1	9	9	0	1	1	0	0	1	1	0	0	1

Notes:

1. The outputs from the tens and units section of the control contain the binary code for numerals 0 through 9 corresponding to the switch position. The outputs from the hundreds section of the control contain the binary code for numerals 0 through 3 corresponding to the switch position.
2. A logical 1 is defined as a voltage level between 4.5 and 5.5 Vdc.
3. A logical 0 is defined as a voltage level between 0 and +0.4 Vdc.

Figure 13. Course Select Degrees Control Output Signals

position are given in figure 14. Ground is applied to the common element of the units switch via pin F of J2004. The sixth output of the units switch is applied to terminal 3 of U2001 on card A7505 via J2004, pin D.

(3) The tens switch provides four inputs to the special programmed integrated circuit U2001. These outputs are identified as 10A, 10B, 10C, and 10D (see figure 930). A logical 1 level is applied to the tens switch via resistor R2002 and J2002 pin E on card A7505. Ground is applied to the tens switch via J2002,pin F. The tens switch position versus the outputs are given in figure 15.

(4) The hundreds switch provides one output to the special programmed integrated circuit U2001. When the hundreds switch is in the 0 position, ground from pin F of J2003 is connected through the hundreds switch to pin E of J2003 and then to terminal 10 of U2001. When the hundreds switch is in the 1 position, the connection between F and F of J2003 is open circuited and a logical 1 is applied to terminal 10 of U2001 via R2006.

(5) The X/Y MODE control signal is applied to the DME. This line is either an open circuit (X mode) or at ground (Y mode) and is controlled by the thumbwheel switch S7506.

(6) The 1 = STANDBY signal from the TRANSMIT pushbutton/indicator switch S7503 is provided to channel select card A7505, pin 14. When the 1 = STANDBY signal is at a logical 1 level (TRANSMIT pushbutton/indicator extinguished), the MANUAL STANDBY output signal on pin 16 of A7505 is at a logical 0 level. When the 1 = STANDBY signal is at a logical 0 level (TRANSMIT pushbutton/indicator illuminated), the MANUAL STANDBY signal level is dependent upon the channel selected by the CHANNEL/MODE thumbwheel switch S7506. When channels 000, 127, 128, or 129 are selected, the MANUAL STANDBY signal is at a logical 0 level. When any channel from 001 to 126 is selected, the MANUAL STANDBY signal is at a logical 1 level.

(7) The special programmed integrated circuit U2001 receives the address inputs on pins 3, 4, 5, 8, 9, and 10 (see figure 930). The outputs for a given input are identified in figure 16. Each output of U2001 is applied to a separate inverter. The outputs of these inverters are identified as the SELECT outputs (7) and

the MANUAL STANDBY signal. When an X (burnout link) is indicated in figure 16, a logical 1 is applied to the applicable inverter resulting in a logical 0 on the associated output. The lack of an X indicates a low output resulting in a logical 1 at the associated output pin of P2001.

SWITCH LEGEND	COMMON CONNECTS TO J2004					
	PIN 6	PIN E	PIN 5	PIN 4	PIN 3	PIN D
0		●	●			●
1		●		●		●
2			●	●		●
3			●		●	●
4				●	●	●
5	●			●		●
6	●				●	●
7		●			●	
8	●	●				
9	●		●			
SIGNAL NAMES	.1A SELECT	.1B SELECT	.1C SELECT	.1D SELECT	.1E SELECT	—
AT P2001	6	10	7	8	9	—

NOTE: ● = GROUND

Figure 14. CHANNEL/MODE Selector Unit Switch Outputs

	COMMONS X (O) AND Y (●) CONNECT TO J2002			
SWITCH LEGEND	PIN A	PIN B	PIN C	PIN D
0	●	●	●	●
1	●	●	●	○
2	●	●	○	●
3	●	●	○	○
4	●	○	●	●
5	●	○	●	○
6	●	○	○	●
7	●	○	○	○
8	○	●	●	●
9	○	●	●	○

NOTES: ● = GROUND (Applied to Switch Via J2002, Pin F)
○ = LOGICAL 1 (Applied to Switch Via J2002, Pin E)

Figure 15. CHANNEL/MODE Selector Ten Switch Outputs

ADDRESS PINS						OUTPUT PINS							
10	9	8	5	4	3	22	21	20	19	18	17	16	15
0	0	0	0	0	0		X		X				
0	0	0	0	0	1			X	X				
0	0	0	0	1	0			X	X				
0	0	0	0	1	1	X			X			X	
0	0	0	1	0	0	X			X			X	
0	0	0	1	0	1	X				X		X	
0	0	0	1	1	0	X				X		X	
0	0	0	1	1	1		X			X	X		
0	0	1	0	0	0		X			X	X		
0	0	1	0	0	1	X	X				X		
0	0	1	0	1	0	X	X				X		
0	0	1	0	1	1	X		X			X		
0	0	1	1	0	0		X	X					
0	0	1	1	0	1		X		X				
0	0	1	1	1	0	X		X			X		
0	0	1	1	1	1		X	X			X		
0	1	0	0	0	0		X	X			X		
0	1	0	0	0	1		X		X		X		
0	1	0	0	1	0		X		X		X		
0	1	0	0	1	1			X	X		X		
1	0	0	0	0	0			X	X		X		
1	0	0	0	0	1			X		X	X		
1	0	0	0	1	0			X		X	X		
1	0	0	0	1	1				X	X	X		
1	0	0	1	0	0				X	X	X		
1	0	0	1	0	1								X
1	0	0	1	1	0								X
1	0	0	1	1	1								X
1	0	1	0	0	0								X
1	0	1	0	0	1								X
1	0	1	0	1	0								X
1	0	1	0	1	1								X
1	0	1	1	0	0								X
1	0	1	1	0	1								X
1	0	1	1	1	0								X
1	0	1	1	1	1								X
1	1	0	0	0	0								X
1	1	0	0	0	1								X
1	1	0	0	1	0								X
1	1	0	0	1	1								X

0 = LOW LEVEL 1 = HIGH LOGIC LEVEL Y = BURNOUT LINK

Figure 16. U2001 Input-To-Output Relationship

CONTENTS
OPERATING PROCEDURES

Paragraph		Page
1.	General	101
2.	Operating Controls and Indicators	101
3.	Pre-Operational Checks	101
4.	Operational Checks	115

OPERATING PROCEDURES

1. GENERAL

This section contains a description of operating controls and indicators, pre-operational checks, and operational checks. The pre-operational checks consist of a self test of the test set that includes a calibration check.

2. OPERATING CONTROLS AND INDICATORS

The operating controls and indicators are identified on figure 101. The description and function of each control, indicator, and connector is identified on figure 102.

3. PRE-OPERATIONAL CHECKS

Perform following steps A through Z before using the test set to verify operation of a ground beacon.

A. On Console Display and Control Panel Unit (Panel Unit), set POWER switch to OFF position.

B. Determine primary power available for test set operation and select appropriate cable as follows:

Power Source Available	Use Cable Part No.
28 VDC	7124-2529-3
115 VAC 60 Hz	7124-2529-1
115 VAC 400 Hz	7124-2529-2
115 VAC 400 Hz (Rack Mounted Variation)	7124-2529-4

NOTE: If test set does not contain a rear panel assembly part No. 7124-2523-1, then test set can only be operated from a power source of 115 VAC 400 Hz. In this instance, use cable part No. 7124-2529-4 connected between test set connector J7513 (POWER IN on side of Digital Bearing Unit mounting rack of panel and chassis assembly) and power source.

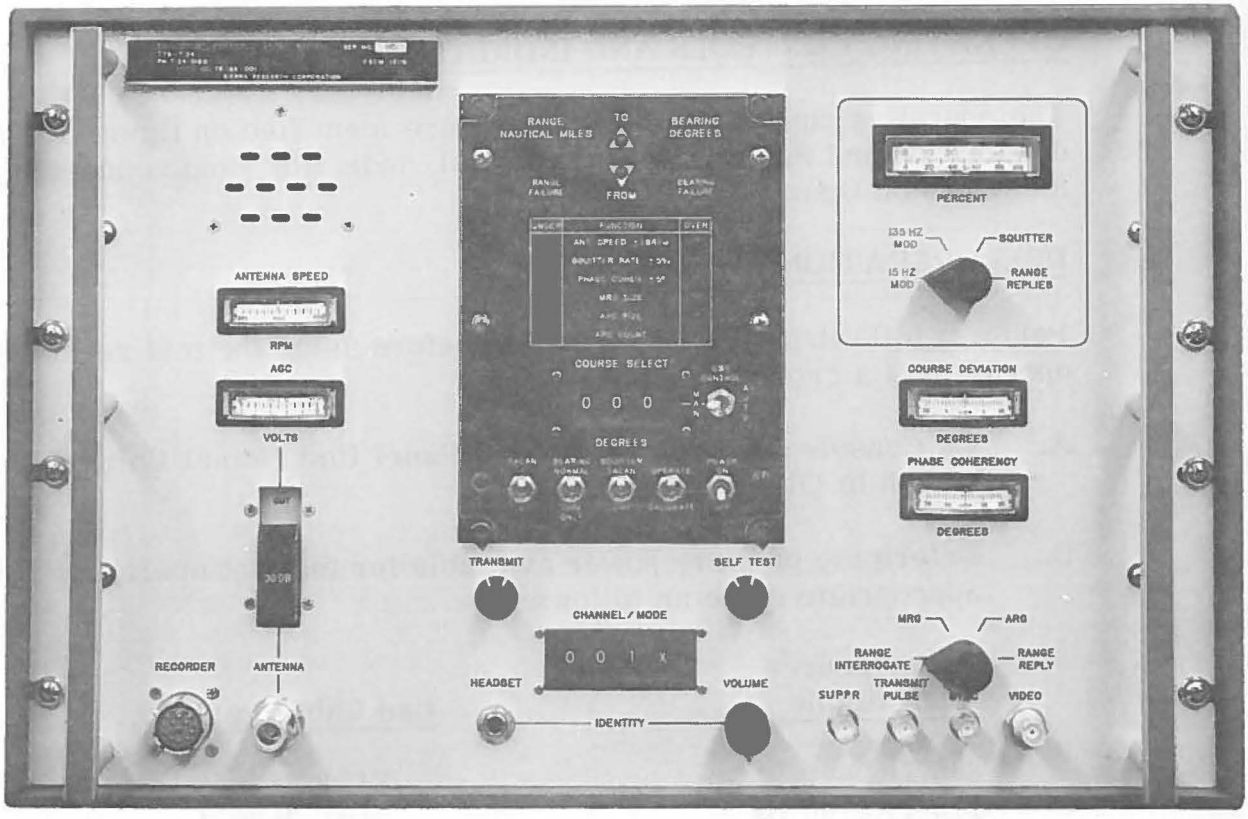

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Figure 101. Operating Controls and Indicators

Control/Indicator/ Connector	Description	Function
Distance Measuring Equipment - Refer to Maintenance/ Overhaul Manual for KDM-7000 Digital DME, for the DME SRU-7000D.		
Console Display and Control Panel Unit		
POWER	Toggle Switch	Controls application of 115V, 400 Hz to DME, Digital Bearing Unit, Signal Analyzer Unit, and Console Display and Control Panel Unit.
TACAN	Toggle Switch	Outputs of switch are not connected. Switch has no function in this application.
BEARING	Toggle Switch	Determines that test set performs analysis on normal beacon signal parameters (15-Hz and 135-Hz modulation) when in NORMAL position, and 15-Hz modulation only beacons when in 15 Hz ONLY position.
SQUITTER	Toggle Switch	Determines that test set performs analysis on TACAN squitter rate when in TACAN position or DME squitter rate when in DME position.
OPERATE/ CALIBRATE	Toggle Switch	Determines that test set performs analysis of beacon signal parameters when in OPERATE position. When in CALIBRATE position, test set is in self test mode and certain calibrations can be performed.

Figure 102. Controls, Indicators, and Connectors (Sheet 1 of 9)

Control/Indicator/ Connector	Description	Function
OBS CONTROL	Toggle Switch	Allows the selected course information (as determined by the COURSE SELECT DEGREES thumbwheel switches) to be provided to the Digital Bearing Unit when in the MAN position. Bearing course deviation (from the selected course) is provided to a recorder and to the COURSE DEVIATION DEGREES meter. When in the AUTO position, course deviation to the recorder and to the COURSE DEVIATION DEGREES meter is from the nearest cardinal (multiples of 10 degrees) radial. In the AUTO position, COURSE SELECT DEGREES thumbwheel switch position does not affect circuit operation.
COURSE SELECT DEGREES	Thumbwheel Switches	Provides selected course information (from 000 to 359) to the Digital Bearing Unit in one-degree, 10-degree, or 100-degree increments when OBS CONTROL is in MAN position.
RANGE NAUTICAL MILES	LED Display	Displays test set range-to-beacon in hundreds, tens, units, and tenths nautical miles for distances up to 399.9 nautical miles. When the test set is operated in the transmit/receive mode and

Figure 102. Controls, Indicators, and Connectors (Sheet 2 of 9)

Control/Indicator/ Connector	Description	Function
RANGE NAUTICAL MILES (cont)		there is an absence of computed data, the RANGE NAUTICAL MILES indicator displays dashes. In test set standby, test set off, or DME failure, the RANGE NAUTICAL MILES indicator is blank (except for decimal point).
BEARING DEGREES	LED Displays	Displays test set bearing from beacon from 000.0 to 359.8 degrees in 0.2-degree increments in test set standby or transmit/receiver modes. In test set off mode, or if Digital Bearing Unit fails, BEARING DEGREES indicator is blank. Displays dashes when test set is in search mode.
RANGE FAILURE	LED Indicator	Illuminates when there is a DME failure.
BEARING FAILURE	LED Indicator	Illuminates when there is a Digital Bearing Unit failure.
TO/FROM	LED Indicators	Indicators illuminate to resolve course deviation ambiguity. Both indicators are extinguished when signal is not received. When OBS CONTROL is in AUTO position, FROM indicator is illuminated. When OBS CONTROL is in MAN position, FROM indicator is illuminated if bearing heading is between 270 and 90 degrees

Figure 102. Controls, Indicators, and Connectors (Sheet 3 of 9)

Control/Indicator/ Connector	Description	Function
TO/FROM (cont)		of selected course, and TO indicator is illuminated if bearing heading is between 90 and 270 degrees of selected course.
ANT. SPEED ±1.8 RPM UNDER	LED Indicator	Illuminates if the ground beacon antenna speed is under specified limit.
ANT. SPEED ±1.8 RPM OVER	LED Indicator	Illuminates if the ground beacon antenna speed is over specified limit.
SQUITTER RATE ±5% UNDER	LED Indicator	Illuminates if the ground beacon squitter rate is under specified limit.
SQUITTER RATE ±5% OVER	LED Indicator	Illuminates if the ground beacon squitter rate is over specified limit.
PHASE COHER ±5° UNDER	LED Indicator	Illuminates if the positive slope point of inflection of the 135-Hz modulation occurs more than 5 degrees after the positive slope point of inflection of the 15-Hz modulation.
PHASE COHER ±5° OVER	LED Indicator	Illuminates if the positive slope point of inflection of the 135-Hz modulation occurs more than 5 degrees before the positive slope point of inflection of the 15-Hz modulation.
MRG SIZE UNDER	LED Indicator	Illuminates if the size of the MRG is less than a normal pulse group.

Figure 102. Controls, Indicators, and Connectors (Sheet 4 of 9)

Control/Indicator/ Connector	Description	Function
MRG SIZE OVER	LED Indicator	Illuminates if the size of the MRG is greater than a normal pulse group.
ARG SIZE UNDER	LED Indicator	Illuminates if the size of the ARG is less than a normal pulse group.
ARG SIZE OVER	LED Indicator	Illuminates if the size of the ARG is greater than a normal pulse group.
ARG COUNT UNDER	LED Indicator	Illuminates if the number of ARG's per antenna revolution is less than 8.
Test Set Front Panel Controls, Indicators, and Connectors		
ANTENNA SPEED	Meter	Indicates ground beacon antenna speed from 895 to 905 rpm.
AGC VOLTS	Meter	Indicates AGC level (either digital TACAN AGC or DME AGC depending upon position of AGC switch S7505) over a range of 0 to 10 volts.
PERCENT	Meter	Indicates 15-Hz modulation or 135-Hz modulation (depending upon position of PERCENT switch) over a range of 0 to 50 percent. Indicates percent of squitter rate or range replies (depending upon position of PERCENT switch) over a range of 0 to 100 percent.

Figure 102. Controls, Indicators, and Connectors (Sheet 5 of 9)

Control/Indicator/ Connector	Description	Function
PERCENT	Switch	Selects percent of 135-Hz modulation, 15-Hz modulation, squitter rate, or range replies for display on PERCENT meter.
COURSE DEVIATION DEGREES	Meter	Indicates amount of course deviation over a range of + or - 10 degrees.
PHASE COHERENCY DEGREES	Meter	Indicates amount of phase coherence (positive slope point of inflection of 135-Hz modulation with respect to positive slope point of inflection of 15-Hz modulation) over a range of ±20 degrees. If indication is plus degrees, positive slope point of inflection of 135-Hz modulation occurs after positive slope point of inflection of 15-Hz modulation. Conversely, if indication is minus degrees, positive slope point of inflection of 135-Hz modulation occurs before positive slope point of inflection of 15-Hz modulation.
HEADSET	Jack	Facilitates connecting a headset to test set to permit monitoring audio identity tone.
Loudspeaker	—	Provides audio indication of identity tone when headset is not connected.

Figure 102. Controls, Indicators, and Connectors (Sheet 6 of 9)

Control/Indicator/ Connector	Description	Function
VOLUME	Variable resistor	Controls volume of audio identity tone on headset (when connected) or loudspeaker.
ANTENNA	Jack	Antenna connection to test set.
30 DB	Attenuator	Provides capability of inserting 30-db of attenuation between ANTENNA input jack and antenna input of DME.
SYNC	Jack	Facilitates connecting synchronizing input to oscilloscope from test set. Synchronizing signal at SYNC jack is dependent upon position of SYNC switch.
SYNC	Switch	Selects MRG, ARG, RANGE INTERROGATE or RANGE REPLY synchronizing signal to oscilloscope via SYNC jack.
TRANSMIT PULSE	Jack	Permits monitoring transmit pulse waveform to DME.
VIDEO	Jack	Permits monitoring amplified video output of Digital Bearing Unit.
SUPPR	Jack	Permits blanking external equipment during test set transmissions.
CHANNEL/MODE	Assembly	Determines operating frequency (channel selection) and X or Y mode of operation of test set.

Figure 102. Controls, Indicators, and Connectors (Sheet 7 of 9)

Control/Indicator/ Connector	Description	Function
RECORDER	Connector	Facilitates connecting a recorder to obtain a permanent record of ground beacon signal parameters such as 15-Hz level, 135-Hz level, squitter rate analog, percent of range replies, bearing deviation, agc, and phase coherency.
TRANSMIT	Pushbutton switch/ LED indicator	Controls logic level of 1 = STANDBY signal input to CHANNEL/MODE selector (logical 1 for standby and logical 0 for transmit) thereby controlling test set standby/transmit mode of operation. Pushbutton switch/indicator illuminates when test set is in TRANSMIT mode.
SELF TEST	Pushbutton switch/ LED indicator	Controls test set operate/ self test mode of operation. When pushbutton switch/ indicator is illuminated, test set is in SELF TEST mode.
Additional Controls and Connectors		
DME AGC/ TACAN AGC	Toggle Switch (located on left inside of test set enclosure frame)	Applies DME AGC to DME, AGC VOLTS meter, and Signal Analyzer Unit when in DME AGC position. Applies TACAN AGC to DME, AGC VOLTS meter, and Signal

Figure 102. Controls, Indicators, and Connectors (Sheet 8 of 9)

Control/Indicator/ Connector	Description	Function
DME AGC/TACAN AGC (cont)		Analyzer Unit when in TACAN AGC position. NOTE: Should be in TACAN AGC position for normal test set operation.
POWER J1	Connector (located on rear panel)	Facilitates connecting power cable 7124-2529-1 (for 115 VAC, 60 Hz), cable 7124-2529-2 (for 115 VAC, 400-Hz), or cable 7124-2529-3 (for 28 VDC) to test set.
POWER J7513	Connector (located on rear of test set panel and chassis assembly)	Facilitates connecting P7513 of rear panel to panel and chassis assembly or cable 7124-2529-4 for 115 VAC, 400-Hz operation when rear panel is not used.

Figure 102. Controls, Indicators, and Connectors (Sheet 9 of 9)

C. For test sets containing a rear panel assembly part No. 7124-2523-1, connect cable assembly selected in step B to connector J1 on rear panel assembly. Insert opposite end of selected cable into proper power source.

D. On Panel Unit, set controls as follows:

Control	Position
OPERATE/CALIBRATE	OPERATE
BEARING	NORMAL
SQUITTER	TACAN
OBS CONTROL	MAN
COURSE SELECT DEGREES	000

E. On test set front panel, set 30 DB attenuator to IN position and connect antenna to ANTENNA connector.

F. Set CHANNEL/MODE selector control to any unused channel, X or Y mode.

G. Determine that TACAN AGC/DME AGE switch, located on left inside of test set panel and chassis assembly, is set to TACAN AGC position.

H. On Panel Unit, set POWER switch to ON position.

I. Observe that TRANSMIT and SELF TEST pushbutton/indicators are extinguished. If not extinguished, depress pushbutton/indicator to extinguish it.

J. Observe for the following search indication on Panel Unit:

RANGE NAUTICAL MILES indicator displays all blanks (decimal point illuminated)

BEARING DEGREES indicator displays all dashes (decimal point illuminated)

SQUITTER RATE ±5% UNDER indicator illuminated

All other indicators on Panel Unit are extinguished

K. Observe for an AGC VOLTS meter indication of greater than 7 volts (indicating DME receiver at maximum sensitivity).

L. Sequentially position PERCENT switch through all four positions while observing for a nominal zero indication on PERCENT meter for each switch position.

M. Depress TRANSMIT pushbutton/indicator and observe that pushbutton/indicator illuminates.

N. Observe that RANGE NAUTICAL MILES indicator changes from all blanks to all dashes. All other indications remain the same as described in steps J through L.

O. Rotate IDENTITY VOLUME control fully clockwise.

P. Depress SELF TEST pushbutton/indicator and observe that pushbutton/indicator illuminates.

Q. Observe the following indications on the Panel Unit:

BEARING DEGREES indication changes from all dashes to 000.0 ± 0.2 degrees within five seconds

RANGE FAILURE indicator will illuminate for one second and then extinguish

RANGE NAUTICAL MILES indicator will change from all dashes to an indication of 000.0 ± 0.1 nautical miles within three seconds

FROM indicator is illuminated

SQUITTER RATE ±5% UNDER indicator is illuminated

MRG SIZE UNDER indicator is illuminated

ARG SIZE UNDER indicator is illuminated

PHASE COHER ± 5° OVER indicator is illuminated

All other indicators on Panel Unit are extinguished

A 1350-Hz tone emanates from speaker.

R. Vary IDENTITY VOLUME control and observe that level of audio tone from speaker changes.

S. Observe that RANGE FAILURE and BEARING FAILURE indicators remain extinguished throughout remainder of self test.

T. Observe that indication on AGC VOLTS meter is approximately 7 volts.

U. Observe that indication on PERCENT meter for each PERCENT switch position is as follows:

Switch Position	Meter Indication
15 HZ MOD	25%
135 HZ MOD	25%
SQUITTER	40%
RANGE REPLIES	100%

V. Set COURSE SELECT DEGREES control to 010. Observe that COURSE DEVIATION DEGREES meter indicates +10 ± 0.5 degrees.

W. Set COURSE SELECT DEGREES control to 350. Observe that COURSE DEVIATION DEGREES meter indicates -10 ± 0.5 degrees.

X. Observe that PHASE COHERENCY DEGREES meter indicates +10 ± 1.2 degrees.

Y. On Panel Unit, set COURSE SELECT DEGREES control to 180 and observe that FROM indicator extinguishes and TO indicator illuminates.

Z. On Panel Unit, set BEARING switch to 15 Hz ONLY position and observe the following indications:

BEARING DEGREES indication changes to 010.0 ± 001.0 degrees within three seconds

PHASE COHER ± 5° OVER indicator extinguishes

TO indicator remains illuminated

SQUITTER RATE ± 5% UNDER indicator remains illuminated

MRG SIZE UNDER indicator remains illuminated

ARG SIZE UNDER indicator remains illuminated.

4. OPERATIONAL CHECKS

The operational check procedure consists of the basic steps required to verify operation of a ground beacon. Refer to following steps A through F.

A. To verify test set operation, perform pre-operational checks described in paragraph 3.

B. Connect recording equipment to RECORDER connector if permanent record of beacon test is required or desirable.

C. If headset is to be used, insert headset jack into HEADSET connector.

D. Set test set control to initial positions as follows:

Control	Position/Condition
POWER	ON
30 DB	OUT
CHANNEL/MODE	To channel number and mode assigned to ground beacon under test
TRANSMIT pushbutton/indicator	Illuminated
SELF TEST pushbutton/indicator	Extinguished
BEARING	Depends upon type of ground beacon under test
SQUITTER	Depends upon type of ground beacon under test
OPERATE/CALIBRATE	OPERATE
OBS CONTROL	Depends upon planned beacon test mission
COURSE SELECT DEGREES	Depends upon planned beacon test mission

E. Beacon identity tone is monitored on headset (if connected) or speaker. Adjust IDENTITY VOLUME control for a comfortable audio listening level.

F. Observe front panel meters, Panel Unit indicators, and recording equipment during beacon test period for analysis of ground beacon operation.

CONTENTS

DISASSEMBLY

Paragraph		Page
1.	General	201
2.	Disassembly Techniques and Precautions	201
3.	TACAN Beacon Test Set Disassembly Procedures	201
	A. Panel and Chassis Assembly Disassembly Procedures	201
	B. Rear Panel Assembly Disassembly Procedures	201
	C. Console Display and Control Panel Unit (Panel Unit) Disassembly Procedures	202
	D. Distance Measuring Equipment (DME) Disassembly Procedures	202
	E. Digital Bearing Unit Disassembly Procedures	202
	F. Signal Analyzer Unit Disassembly Procedures	203

DISASSEMBLY

1. GENERAL

Disassemble only to the extent necessary to effect repair and test. The following instructions include procedures that are necessary to remove and disassemble the TACAN Beacon Test Set and the major subassemblies of this test set.

2. DISASSEMBLY TECHNIQUES AND PRECAUTIONS

To facilitate reassembly, tag all disconnected wires.

CAUTION: VERIFY THAT POWER IS REMOVED FROM TEST SET BEFORE DISASSEMBLING ANY PART OF THE TEST SET.

3. TACAN BEACON TEST SET DISASSEMBLY PROCEDURES

A. Panel and Chassis Assembly Disassembly Procedures

Perform following steps (1) through (4) to disassemble the panel (front) and chassis assembly from the TACAN Beacon Test Set case.

(1) Remove eight screws that secure panel (front) and chassis assembly to case.

(2) Gently slide panel and chassis assembly from case far enough to permit access to power cable connector P7513.

(3) Disconnect P7513 from power connector mounted to Digital Bearing Unit mounting rack.

(4) Remove panel and chassis assembly from case.

B. Rear Panel Assembly Disassembly Procedures

Perform following steps (1) through (4) to disassemble the rear panel assembly from the TACAN Beacon Test Set case.

(1) Remove eight screws that secure rear panel assembly to case.

(2) Gently slide rear panel assembly from case far enough to permit access to power cable connector P7513.

(3) Determine that connector P7513 has been disconnected from power connector mounted to Digital Bearing Unit mounting rack.

(4) Remove rear panel assembly from case.

C. Console Display and Control Panel Unit (Panel Unit) Disassembly Procedures

Perform following steps (1) through (6) to disassemble Panel Unit.

(1) Disconnect four Dzus fasteners that secure Panel Unit to Test Set front panel.

(2) Remove Panel Unit from Test Set.

(3) Disconnect test set connector J7504 from Panel Unit connector J7401 (rear of Panel Unit) by disengaging slip lock.

(4) Remove dust cover from rear of Panel Unit by removing three screws, lockwashers, and flat washers (see figure 1223).

(5) Remove transformer mounting plate by removing eight screws from perimeter of transformer mounting plate.

(6) Position transformer mounting plate to permit access to components mounted within main chassis.

D. Distance Measuring Equipment (DME) Disassembly Procedures

Perform following steps (1) and (2) to disassemble DME.

(1) Remove DME from DME mounting rack by loosening knurled knobs on front of mounting rack.

(2) For further disassembly procedures, refer to Overhaul Manual for KDM-7000 Digital DME.

E. Digital Bearing Unit Disassembly Procedures

Perform following steps (1) through (4) to disassemble Digital Bearing Unit.

(1) Remove Digital Bearing Unit from mounting rack by loosening knurled knob on front of mounting rack.

(2) Loosen two captive screws at rear of Digital Bearing Unit.

(3) Slide cover from Digital Bearing Unit.

(4) To remove printed-circuit cards, remove two screws at top of cards and pull card straight up. Note that the 300 and 400 cards have captive screw fasteners in center of card as well as top of card.

F. Signal Analyzer Unit Disassembly Procedures

The Signal Analyzer Unit disassembly procedures are essentially identical to those of the Digital Bearing Unit (refer to paragraph 3E).

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CLEANING

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CLEANING

1. GENERAL

The cleaning procedures for the components of the TACAN Beacon Test Set are identical and are as follows:

A. Using a clean lint-free cloth lightly moistened with an approved cleaning solvent, remove any foreign matter. Wipe dry using a clean, lint-free cloth.

B. Using a hand-controlled dry air jet (not more than 15 psi), blow dust from inaccessible areas. Exercise caution to prevent damage caused by air blast.

C. Clean receptacles and plugs with a hand-controlled dry air jet (not more than 25 psi) and a clean lint-free cloth lightly moistened with an approved cleaning solvent. Wipe dry with a clean, dry, lint-free cloth.

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INSPECTION/CHECK

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	I. Terminal Connections, Soldered	402
	J. Transformer	402
	K. Wiring	403

INSPECTION/CHECK

1. GENERAL

This section contains instructions for inspecting the condition of assemblies of the TACAN Beacon Test Set. Defects resulting from wear, physical damage, deterioration, or other causes can be found by performing these inspection procedures. Inspection/check procedures for the Distance Measuring Equipment are given in the Overhaul Manual for KDM-7000 Digital DME.

2. INSPECTION PROCEDURE

Inspect the following mechanical and electrical parts for the conditions specified in each paragraph.

A. Main Frame

Inspect the main frame for deformation, dents, punctures, badly worn surfaces, damaged connectors, damaged fastener devices, damaged handles, component corrosion, and damage to the finish.

B. Connectors

Inspect connectors for broken parts, deformed shell or clamps, and other irregularities. Inspect for cracked or broken insulation and for contacts that are broken, deformed or out of alignment. Also check for corroded or damaged plating on contacts and for loose, improperly soldered, broken or corroded terminal connections.

C. Capacitors

Inspect capacitors for case damage, body damage, and cracked, broken or charred insulation. Check for loose, broken or corroded terminal studs, lugs or leads. Inspect for loose, broken or improperly soldered connections.

D. Cover

Inspect cover for punctures, deep dents and badly worn surfaces. Also check for damaged fastener devices, corrosion and damage to finish.

E. Indicators and Meters

Inspect fault indicators and meters for cracked or broken face plate or housing.

F. Variable Resistors

Inspect all variable resistors for evidence of damage, cracked insulation, or other irregularities.

G. Printed Circuit Cards

Inspect all printed circuit cards for broken leads of components mounted on each card. Check for damaged integrated circuits. Cards should be free of all foreign material.

H. Resistors

Inspect fixed resistors for cracked, broken, blistered or charred bodies and loose, broken or improperly soldered or corroded terminal connections.

I. Terminal Connections, Soldered

(1) Inspect for cold-soldered or resin joints. These joints present a porous or dull, rough appearance. Check for strength of bond using the point of a tool.

(2) Examine terminals for excess solder, protrusions from joint, pieces adhering to adjacent insulation and particles lodged between joints, conductors or other components.

(3) Inspect for insufficient solder and unsoldered strands of wire protruding from conductor at terminal. Check for insulation that is stripped back too far from terminal.

(4) Inspect for corrosion at terminal.

J. Transformer

(1) Inspect for signs of excessive heating, physical damage to case, cracked or broken insulation, and other abnormal conditions.

(2) Inspect for corroded, poorly soldered, or loose connecting wires.

K. Wiring

Inspect wiring of main frame and subassemblies for breaks in insulation, conductor breaks, cut or broken lacing and improper dress in relation to adjacent wiring or frame.

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REPAIR

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	B. Wiring	501
	C. Multilayer Cards	501
	D. Switches and Meters	501

REPAIR

1. GENERAL

This section describes the procedure, along with any special techniques required, for replacing any damaged or defective components of the TACAN Beacon Test Set. Detailed repair procedures for the Distance Measuring Equipment are given in Overhaul Manual for KDM-7000 Digital DME.

2. REPAIR PROCEDURES

A. Semiconductors and Integrated Circuits

Refer to TEST AND ALIGNMENT section for removal and replacement instructions.

B. Wiring

When repairing a wire that has broken from its terminal, remove all old solder and pieces of wire from the terminal, restrip wire to necessary length and resolder wire to terminal. Replace damaged wire with wire of same size and color code.

C. Multilayer Cards

Refer to TEST AND ALIGNMENT section for repair information for multilayer cards.

D. Switches and Meters

When replacing defective switches or meters, tag wires as defective switch or meter is removed. Remove defective switch or meter and replace with new one. Connect wires to new component maintaining proper wiring configuration.

CONTENTS
ASSEMBLY

Paragraph		Page
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ASSEMBLY

1. GENERAL

Assembly procedures for the TACAN Beacon Test Set are essentially the reverse of the disassembly procedures. For assembly procedures of the Distance Measuring Equipment, refer to Overhaul Manual for KDM-7000 Digital DME.

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TEST AND ALIGNMENT

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TEST AND ALIGNMENT

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TEST AND ALIGNMENT

1. GENERAL

This section contains the necessary procedures required to verify that the TACAN test set is operating properly. In addition, the adjustment procedures for the test set are given in paragraphs 4 and 5. Because of the extensive utilization of semiconductors in this test set, some special techniques are necessary in performing the maintenance procedures. In solid state circuits, the impedances and resistances encountered are of much lower values than those encountered in electronic-tube circuits. Therefore, a few ohms discrepancy can greatly affect the performance of the test set. Also, coupling and filter capacitors are of larger values and usually are of the tantalum type. Hence, when measuring values of capacitors, an instrument accurate in the high ranges must be employed. Capacitor polarity must be observed when measuring leakage resistance. Usually more accurate measurements can be obtained if the semiconductors are removed or disconnected from the circuit.

2. SEMICONDUCTOR AND INTEGRATED CIRCUIT INFORMATION

A. Semiconductor Test Equipment

Damage to semiconductors by test equipment is usually the result of accidentally applying too much current or voltage to the elements. Common causes of damage from test equipment are discussed in the following paragraphs B through E.

B. Transformerless Power Supplies

Test equipment with transformerless power supplies is one source of high current. However, this type of test equipment can be used by employing an isolation transformer in the a-c power line.

C. Line Filter

It is still possible to damage semiconductors from line current (even though the test equipment has a power transformer in the power supply), if the test equipment is provided with a line filter. This filter may function as a voltage divider and apply half voltage to the semiconductor. To eliminate this condition, connect a ground wire from the chassis of the test equipment to the chassis of the equipment under test before making any other connections.

D. Low-Sensitivity Multimeters

Another cause of semiconductor damage is a multimeter that requires excessive current to provide adequate indications. Multimeters with sensitivities of less than 20,000-ohms-per-volt should not be used on semiconductors. A multimeter with low sensitivity will draw too much current through many types of small semiconductors causing damage. When in doubt as to the amount of current supplied by a multimeter, check the multimeter circuits on all scales with an external, low-resistance multimeter connected in series with the multimeter leads. If more than one milliampere is drawn on any range, this range cannot be safely used on small semiconductors.

E. Power Supply

When using a battery-type power supply, always use fresh batteries of the proper value. Make certain that the polarity of the power supply is correct for the equipment under test. Do not use power supplies having poor voltage regulation.

F. Semiconductor Voltage and Resistance Measurements

When measuring voltage or resistances in circuits containing semiconductor devices, remember that these components are polarity and voltage conscious. Since the values of capacitors used in semiconductor circuits are usually large (especially in audio, servo, or power circuits), time is required for the measuring device to charge these capacitors. Thus, any reading obtained is subject to error if sufficient time is not allowed for the capacitor to fully charge. When in doubt, isolate the components in question and measure them individually.

G. Transistor Testing

A transistor checker should be used to properly evaluate transistors. If a transistor tester is not available, a good multimeter may be used. Make sure that the multimeter meets the requirements outlined in paragraph D.

CAUTION: IF A TRANSISTOR IS FOUND TO BE DEFECTIVE, MAKE CERTAIN THAT THE CIRCUIT IS IN GOOD OPERATING ORDER BEFORE INSTALLING A REPLACEMENT TRANSISTOR. IF A SHORT CIRCUIT EXISTS IN THE CIRCUIT, PUTTING IN ANOTHER

CAUTION: (Cont) TRANSISTOR WILL MOST LIKELY RESULT IN BURNING OUT THE NEW COMPONENT. DO NOT DEPEND UPON CIRCUIT BREAKERS TO PROTECT TRANSISTORS.

H. PNP Transistor

To check a PNP transistor, connect the positive lead of the multimeter to the base of the transistor and the negative lead to the emitter. Generally, a resistance reading of 50,000 ohms or more should be obtained. Connect the multimeter with the negative lead to the base. With the positive lead connected to the emitter, a resistance value of 500 ohms or less should be obtained.

I. NPN Transistor

Similar tests made on an NPN transistor should produce the following results: With the negative lead of the multimeter connected to the base of the transistor, the value of resistance between the base and collector should be high. With the positive lead of the multimeter connected to the base, the value of resistance between the base and collector should be low. If these results are not obtained, the transistor is probably defective and should be replaced.

J. Bias Resistance

Always check the value of the bias resistance in series with the various transistor elements. A transistor is very sensitive to improper bias voltage; therefore, a short or open circuit in the bias resistance may damage the transistor. For this reason, do not troubleshoot by shorting the various points in the circuit to ground.

K. Replacing Semiconductors

Never remove or replace a semiconductor with the supply voltage turned on. Transients thus produced may damage the semiconductor or others remaining in the circuit. If a semiconductor is to be evaluated in an external test circuit, be sure that no more voltage is applied to the semiconductor than normally is used in the circuit from which it came.

(1) Use only a low heat soldering iron (25 watts or less) when installing or removing soldered parts. When installing or removing a soldered semiconductor, grasp the lead to which heat is applied between the solder joint and the semiconductor with

a long-nosed pliers. This will dissipate some of the heat that would otherwise conduct into the semiconductor from the soldering iron. Ascertain that all wires soldered to semiconductor terminals have been properly tinned so that the necessary connection can be made quickly. Excessive heat permanently damages a semiconductor.

(2) Power transistors are mounted on a heat sink that is designed to dissipate heat away from them. The transistors must also be insulated from ground. This insulating is accomplished by means of anodizing the heat sink. Before installing the anodized heat sink, treat it with a film of Dow-Corning DC-4 Compound. This treatment helps in the transfer of heat. After the transistors are mounted, and before making any connections, check from the case of each transistor to ground with a multimeter to see that the insulation is effective. A frame-mounted transistor uses a mica washer for insulating and two extruded washers for mounting.

3. INTEGRATED CIRCUIT MAINTENANCE

Figure 801 is a list of the integrated circuits used in the test set identifying the manufacturer and the type. Figure 802 contains the integrated circuit logic diagrams and associated truth tables.

A. General

A knowledge of digital circuit fundamentals is necessary in testing logic circuits involving integrated circuits.

(1) A digital logic signal is either at a "one" (HI) or a "zero" (LO) level. A HI level for standard TTL circuitry is a level that is greater than +2 volts and a LO level less than +0.8 volts in the digital logic elements.

(2) A digital logic element should be thought of as a circuit element with its output level (being either HI or LO) programmed by levels and transitions present on its inputs. A list of programmed output levels corresponding to various combinations of input levels and transitions is known as a Truth Table.

(3) A digital I. C. logic element may be tested by verifying that it is performing per the Truth Table of that logic element.

Device Type Number	Manufacturer	Type
AH0014D	National Semiconductor Corp.	DPDT Analog Switch
AH0015D	National Semiconductor Corp.	Quadruple SPST Analog Switch
CO-238A-1	Vectron Laboratories Inc.	4-MHz Crystal Controlled Logic Clock
LM106H	National Semiconductor Corp.	Voltage Comparator
LM9100	Gulton Industries Inc.	Voltage Controlled Oscillator
SC5962-0068-1 (LM9103)	Sierra Research Corp. (Gulton Industries Inc.)	TTL-to-High Level Interface
MC1563R	Motorola Inc.	Negative Voltage Regulator
MC1569R	Motorola Inc.	Positive Voltage Regulator
NH0005	National Semiconductor Corp.	Operational Amplifier
S54H04A	Signetics Corp.	Hex Inverter
S5400A	Signetics Corp.	Quadruple, 2-input positive NAND gate
S5402A	Signetics Corp.	Quadruple, 2-input, positive NOR gate
S5404A	Signetics Corp.	Hex Inverter
S5406A	Texas Instrument Inc.	Hex Inverter Buffers/ Dividers with Open Collector High-Voltage Outputs
S54H08A	Signetics Corp.	Quadruple, 2-Input, Positive AND Gate

Figure 801. Integrated Circuit List (Sheet 1 of 3)

Device Type Number	Manufacturer	Type
S5410A	Signetics Corp.	Triple, 3-Input, Positive NAND Gate
SN5432J	Texas Instrument Inc.	Quadruple 2-Input Positive - OR Gate
S5474A	Signetics Corp.	Dual "D" type Flip-Flop
SN5475B	Signetics Corp.	Quadruple Bistable Latch
SN5485	Texas Instrument Corp.	4-Bit Magnitude Comparator
S5486A	Signetics Corp.	Quadruple, 2-Input Exclusive OR Gate
S5490A	Signetics Corp.	Counter, divide by 2, 5, or 10
S5492A	Signetics Corp.	Counter, divide by 2, 3, 6, or 12
S5493A	Signetics Corp.	Counter, divide by 2, 4, 8, or 16
S8242A	Signetics Corp.	Quadruple Exclusive - NOR Gate
SN54122J	Texas Instrument Corp.	Retriggerable Monostable Multivibrator with Clear
S54123B	Signetics Corp.	Dual Retriggerable, Monostable Multivibrator
S54157B	Signetics Corp.	Quadruple, 2-Input Data Selection Multiplexer
S54164A	Signetics Corp.	8-Bit Serial-In, Parallel-Out, Shift Register

Figure 801. Integrated Circuit List (Sheet 2 of 3)

Device Type Number	Manufacturer	Type
SN54174J	Texas Instrument Corp.	Hex D-Type Flip-Flop with Clear
S54193B	Signetics Corp.	Synchronous 4-Bit Up/ Down Counter with Preset Inputs
U6A7741312	Fairchild	Frequency-Compensated Operational Amplifier
U6A7749312	Fairchild	Dual Operational Amplifier
U6W7747312	Advanced Micro Devices	Dual Frequency Compensated Operational Amplifier
SC6250-0021-1 (U9101)	Sierra Research Corp. (Unique Mfg. Co.)	Indicator
899-3-R3.3K	Beckman Instruments Inc.	Resistor Array
899-3-R100	Beckman Instruments Inc.	Resistor Array
SC5962-0070 (HROM)	Sierra Research Corp. (Harris Semiconductor)	Special Programmed Integrated Circuit

Figure 801. Integrated Circuit List (Sheet 3 of 3)

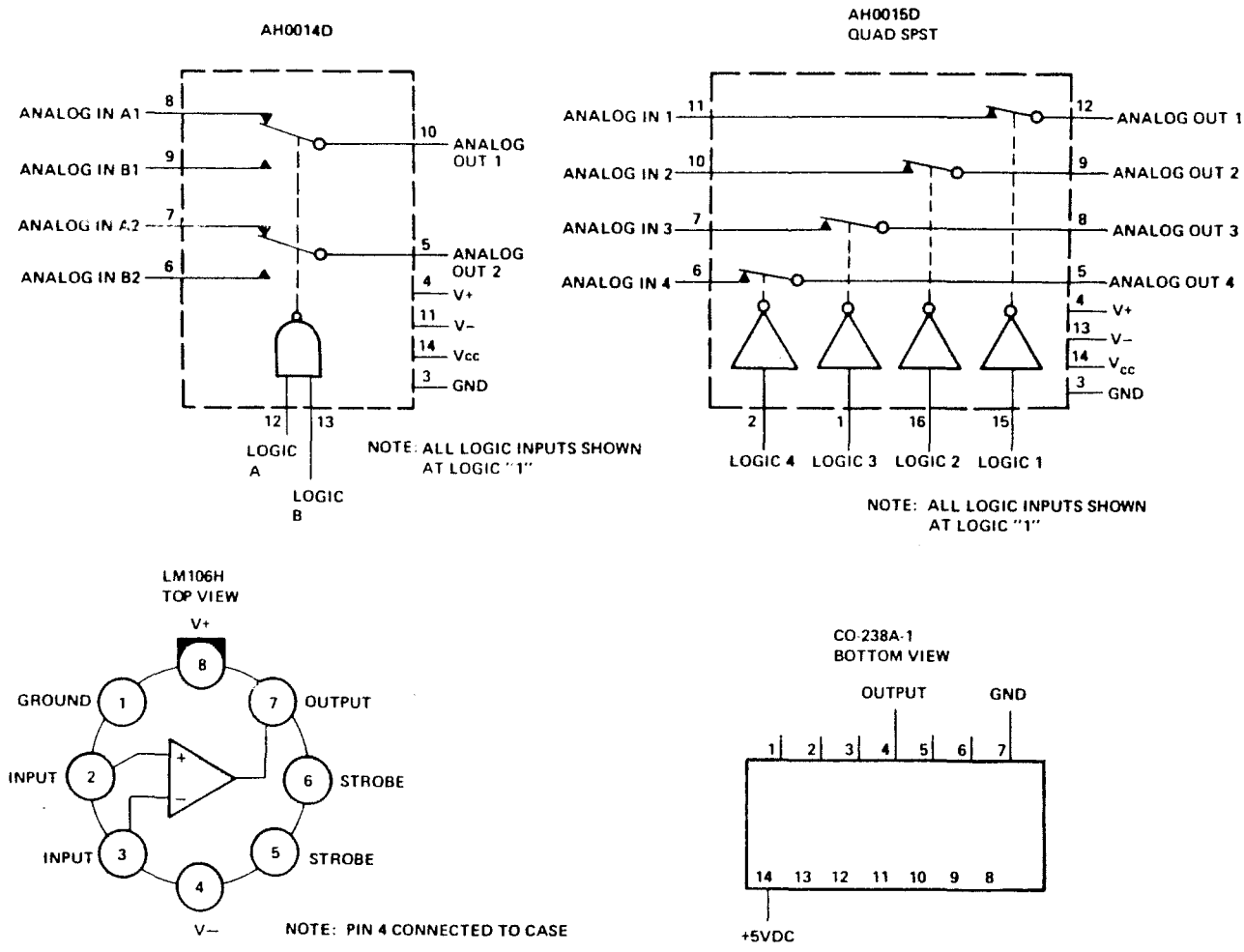
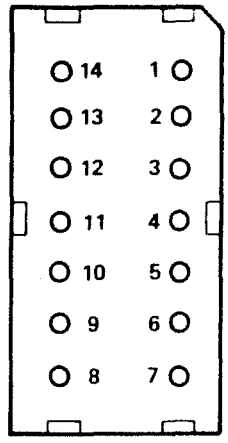


Figure 802. Integrated Circuits (Sheet 1 of 15)

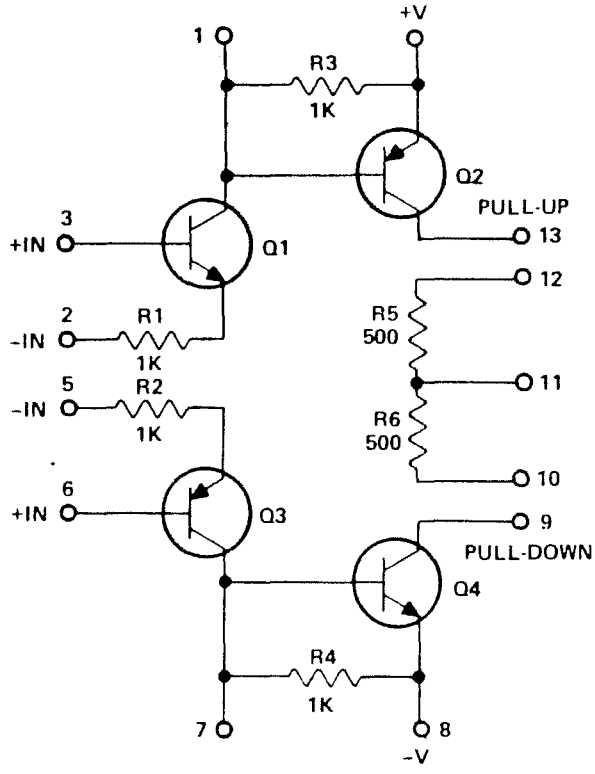
LM 9103
BASE CONNECTION



BOTTOM VIEW

SC5962-0068-1

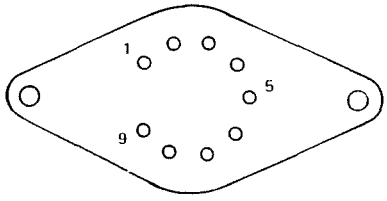
LM9103



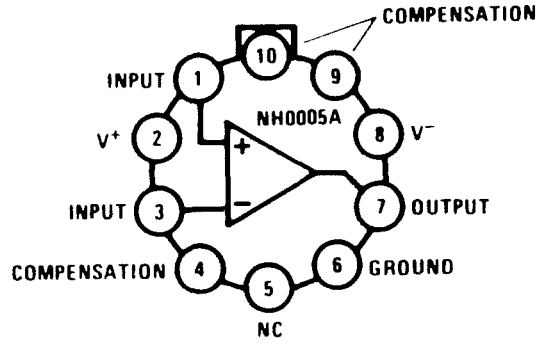
1814-017

Figure 802. Integrated Circuits (Sheet 2 of 15)

MC 1563R AND MC 1569R
PIN CONNECTION

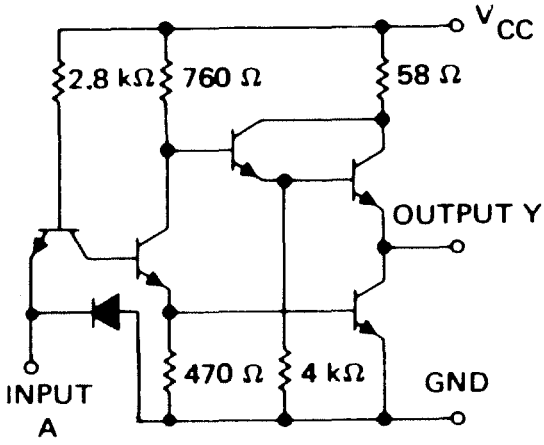


NH0005
TOP VIEW

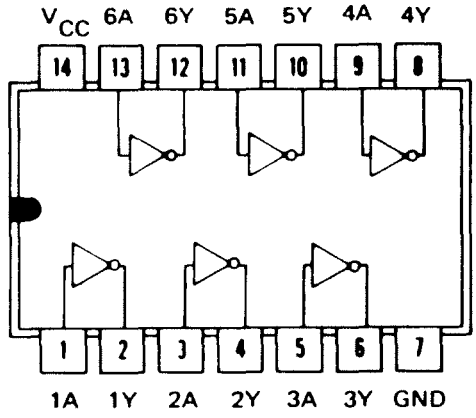


S54H04
$Y = \overline{A}$

SCHEMATIC (EACH INVERTER)

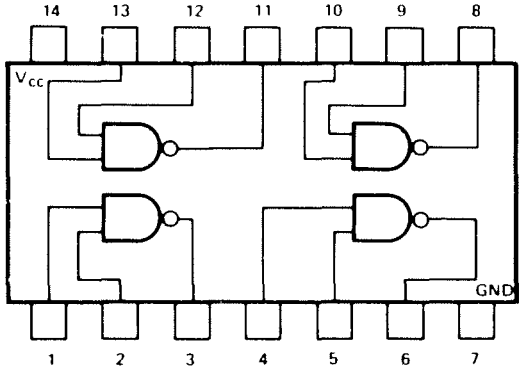


J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

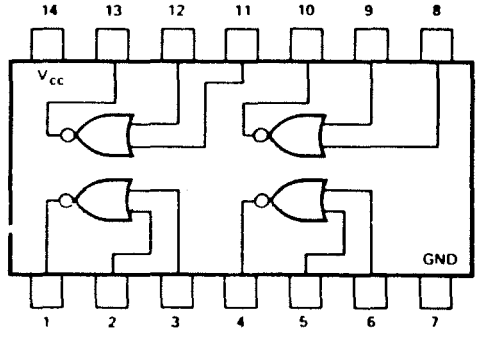


NOTE: COMPONENT VALUES SHOWN ARE NOMINAL

S5400A
POSITIVE LOGIC: $Y = \overline{AB}$



S5402A
POSITIVE LOGIC: $Y = \overline{A+B}$



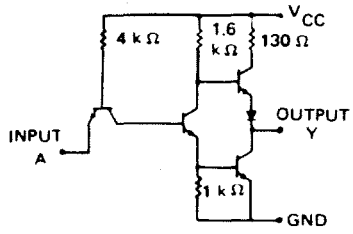
1552-013

Figure 802. Integrated Circuits (Sheet 3 of 15)

S5404A

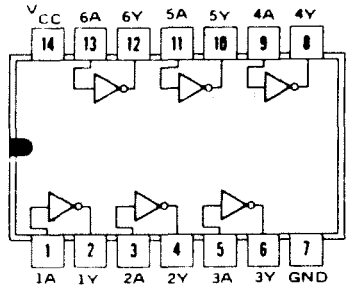
POSITIVE LOGIC $Y = \overline{A}$

SCHEMATIC (EACH INVERTER)



NOTE: COMPONENT VALUES SHOWN ARE NOMINAL

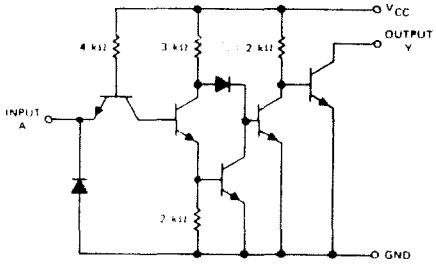
(TOP VIEW)



SN5406

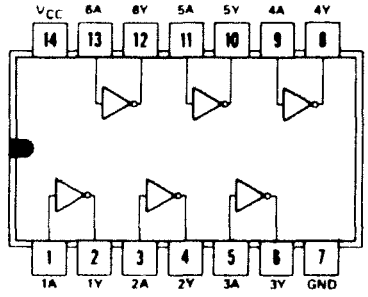
POSITIVE LOGIC $Y = \overline{A}$

SCHEMATIC (EACH INVERTER)



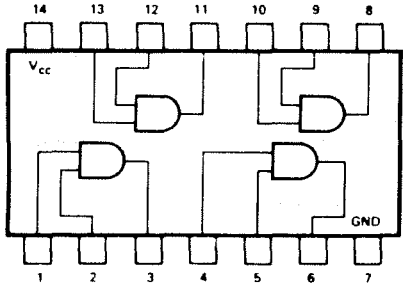
NOTE: COMPONENT VALUES SHOWN ARE NOMINAL

(TOP VIEW)



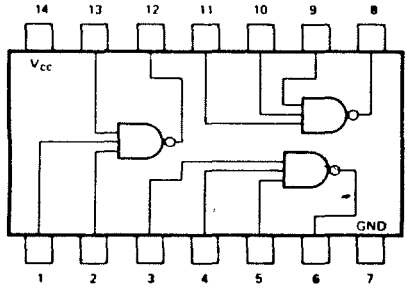
S54H08A

POSITIVE LOGIC $Y = AB$



S5410A

POSITIVE LOGIC $Y = \overline{ABC}$

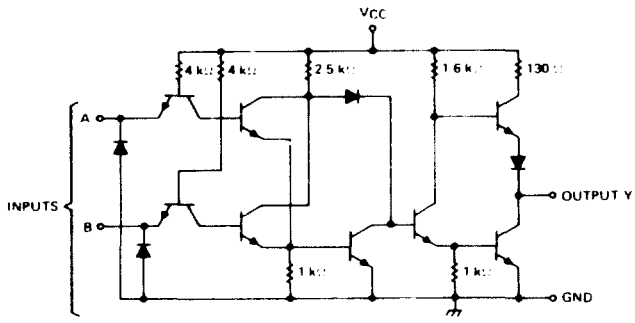


1552-014

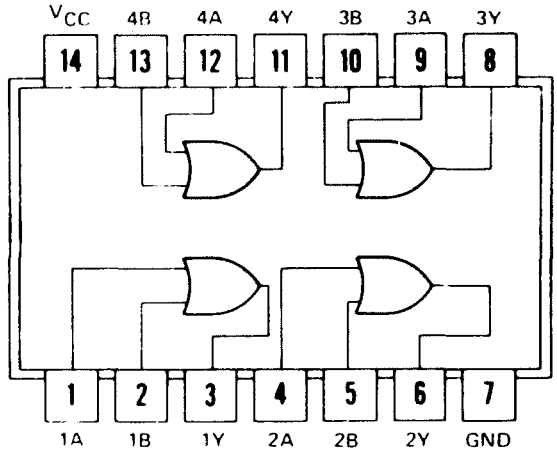
Figure 802. Integrated Circuits (Sheet 4 of 15)

SN5432J

SCHEMATIC (EACH GATE)



J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



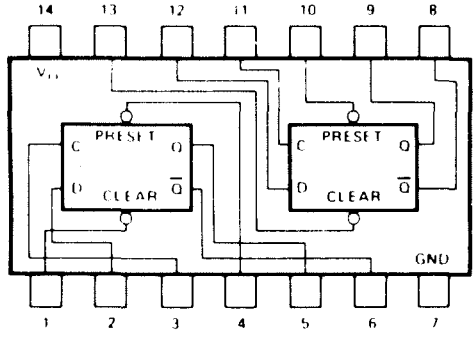
POSITIVE LOGIC: Y=A+B

S5474A

D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	1

1 Both outputs in 1 state
n is time prior to clock
n + 1 is time following clock



POSITIVE LOGIC - LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0. PRESET AND CLEAR
ARE INDEPENDENT OF CLOCK

1552-015

Figure 802. Integrated Circuits (Sheet 5 of 15)

SN5475B

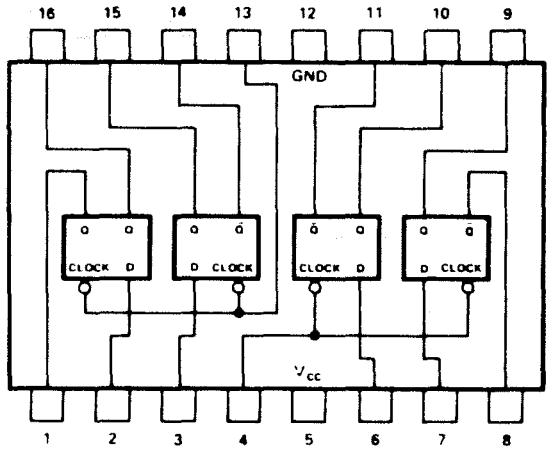
TRUTH TABLE

LOGIC

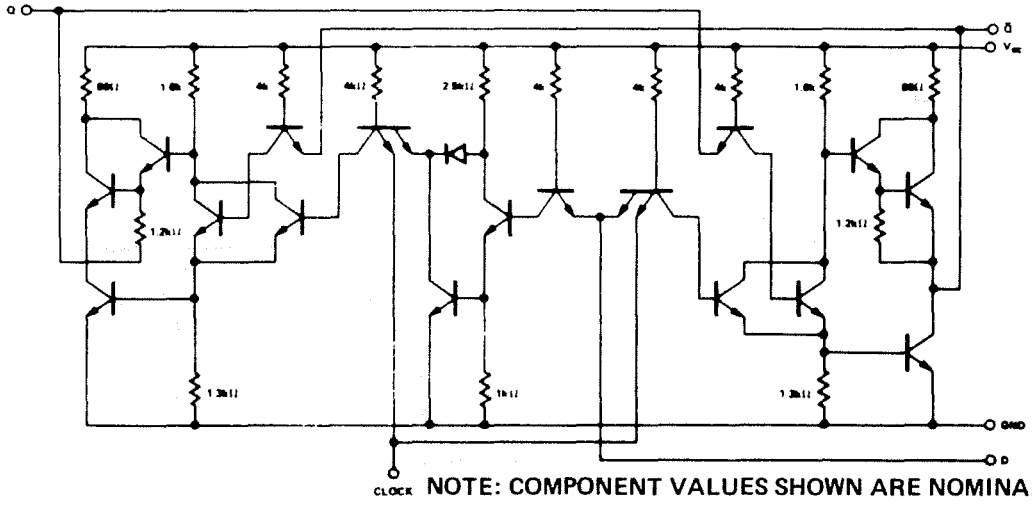
(Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

B PACKAGE



SCHEMATIC (EACH LATCH)



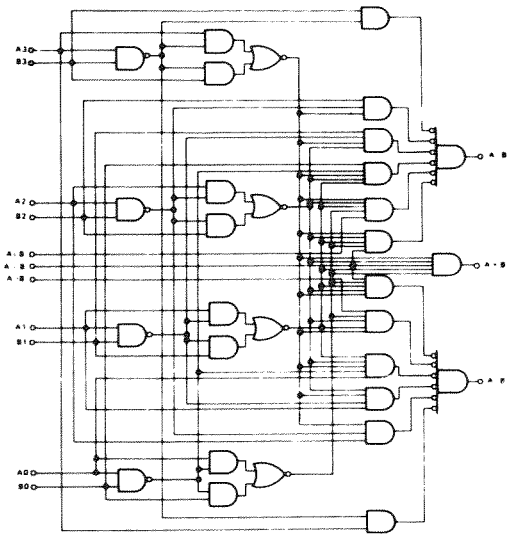
NOTE: COMPONENT VALUES SHOWN ARE NOMINAL

1552-016

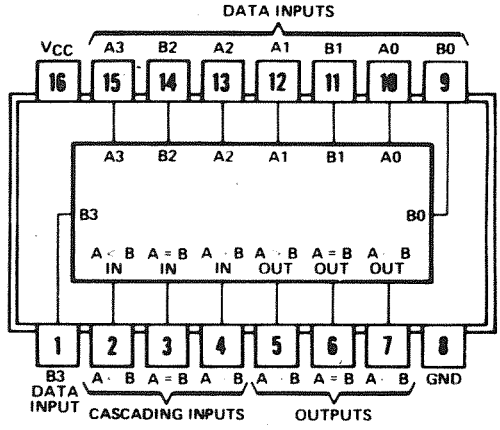
Figure 802. Integrated Circuits (Sheet 6 of 15)

SN5485

FUNCTIONAL BLOCK DIAGRAM



(TOP VIEW)



POSITIVE LOGIC: SEE TRUTH TABLE

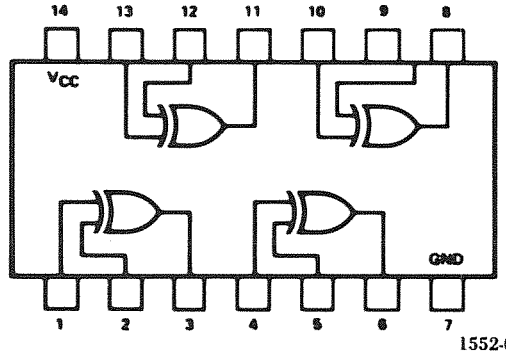
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

S5486A

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



1552-017

Figure 802. Integrated Circuits (Sheet 7 of 15)

S5490A

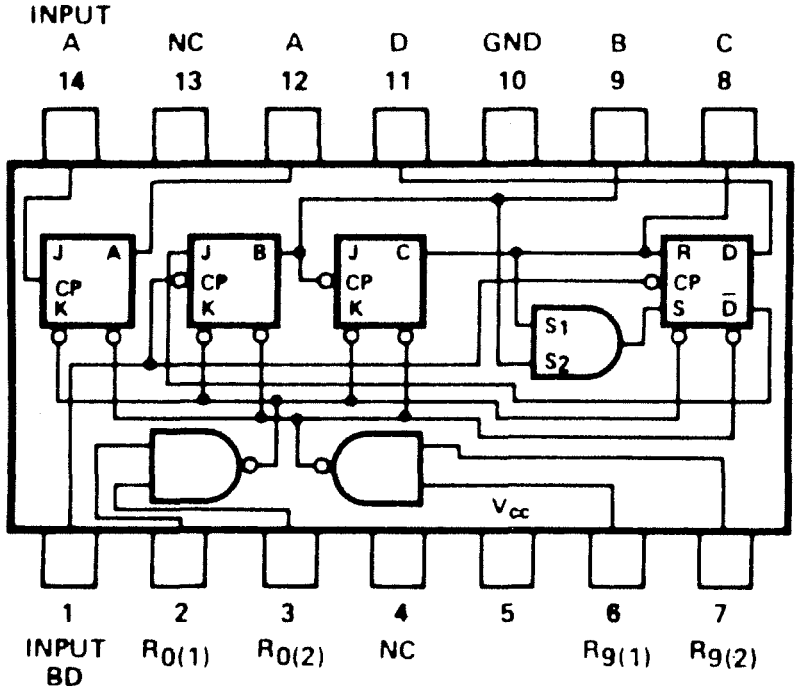
BCD COUNT SEQUENCE (See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

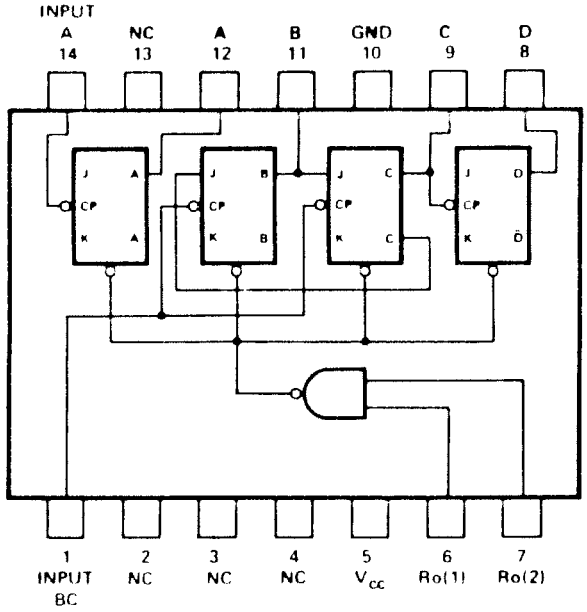
NOTES:
1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted



1552-018

Figure 802. Integrated Circuits (Sheet 8 of 15)

S5492A



COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

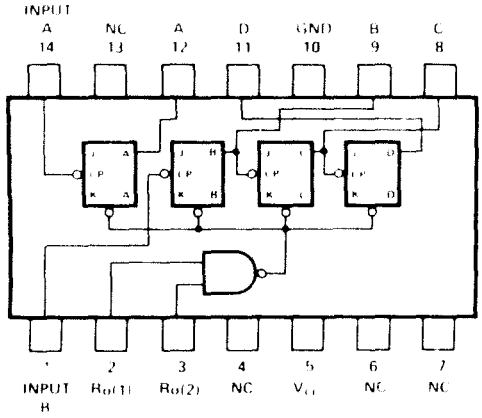
COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES:
1. OUTPUT A CONNECTED TO INPUT B.
2. TO RESET ALL OUTPUTS TO LOGICAL 0, BOTH $R_{0(1)}$ AND $R_{0(2)}$ INPUTS MUST BE AT LOGICAL 1.

1552-019

Figure 802. Integrated Circuits (Sheet 9 of 15)

S5493A



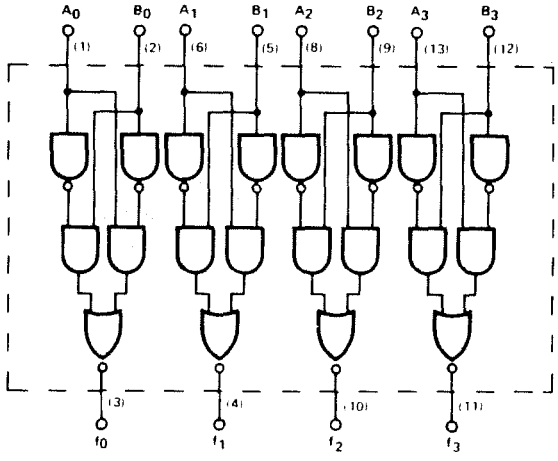
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

COUNT	OUTPUT			
	D	C	B	A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:

1. OUTPUT A CONNECTED TO INPUT B
2. TO RESET ALL OUTPUTS TO LOGICAL 0, BOTH $R_{0(1)}$ AND $R_{0(2)}$ INPUTS MUST BE AT LOGICAL 1.

S8242A



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

V_{CC} = (14)

GND = (7)

( ) = DENOTES PIN NUMBERS

1552-020

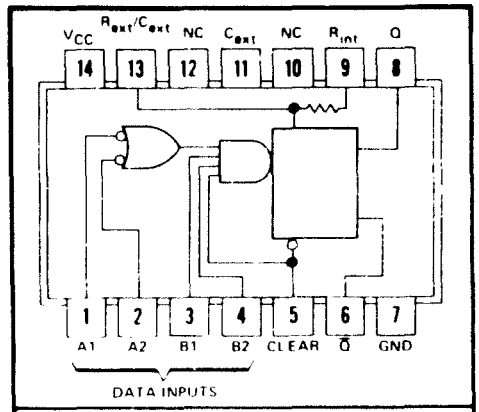
Figure 802. Integrated Circuits (Sheet 10 of 15)

SN54122J

TRUTH TABLE
(SEE NOTE A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

(SEE NOTES B THRU D)



positive logic:
Low input to clear resets Q to low level and inhibits data inputs

NOTES: A. H = HIGH LEVEL (STEADY STATE), L = LOW LEVEL (STEADY STATE), ↑ = TRANSITION FROM LOW TO HIGH LEVEL, ↓ = TRANSITION FROM HIGH TO LOW LEVEL, ⎍ = ONE HIGH-LEVEL PULSE, ⎏ = ONE LOW-LEVEL PULSE, X = IRRELEVANT (ANY INPUT, INCLUDING TRANSITIONS).

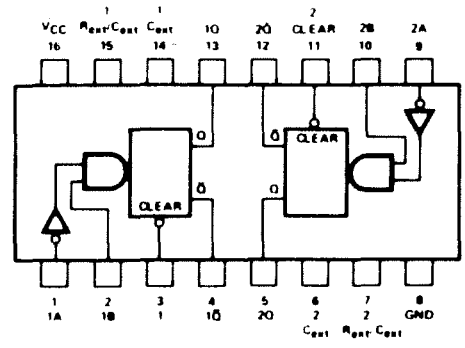
B. NC = NO INTERNAL CONNECTION.

C. TO USE THE INTERNAL TIMING RESISTOR OF SN54122/SN74122 (10 kΩ NOMINAL), CONNECT R_{INT} TO V_{CC}.

D. AN EXTERNAL TIMING CAPACITOR MAY BE CONNECTED BETWEEN C_{EXT} AND R_{EXT}/C_{EXT} (POSITIVE).

S54123B

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎏
↓	H	⎍	⎏



NOTES:
A. H = HIGH LEVEL (STEADY STATE), L = LOW LEVEL (STEADY STATE), = TRANSITION (FROM LOW TO HIGH LEVEL, = TRANSITION FROM HIGH TO LOW LEVEL, = ONE HIGH LEVEL PULSE, = ONE LOW-LEVEL PULSE, X = IRRELEVANT (ANY INPUT, INCLUDING TRANSITIONS).

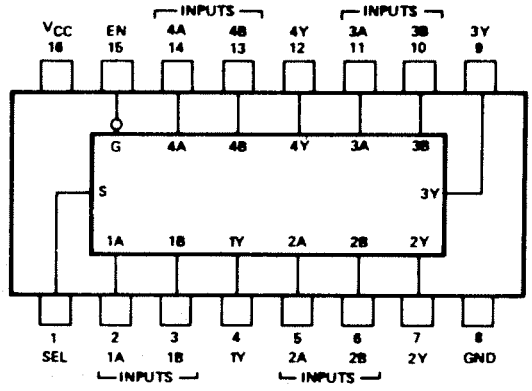
1552-021

Figure 802. Integrated Circuits (Sheet 11 of 15)

S54157B

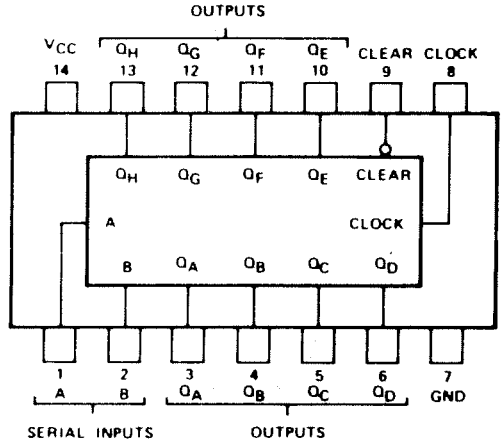
INPUTS			OUTPUT Y
ENABLE	SELECT	A B	
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT



S54164A

INPUTS ATt_n		OUTPUT ATt_n+1
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L



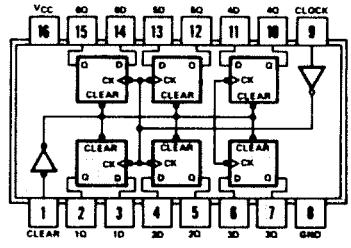
SN54174J

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED
SN54175 AND SN74175 ONLY.

(TOP VIEW)

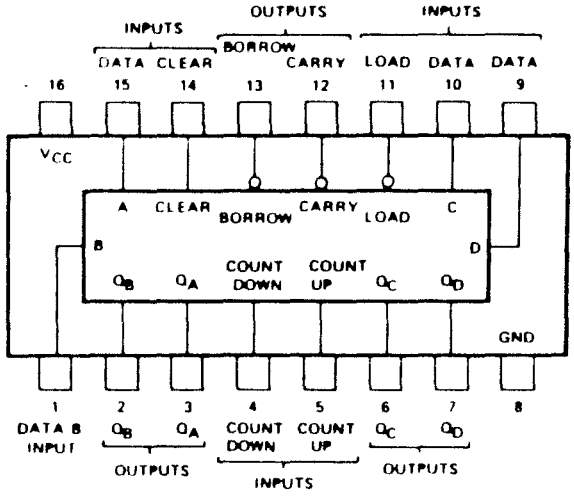


positive logic: see function table

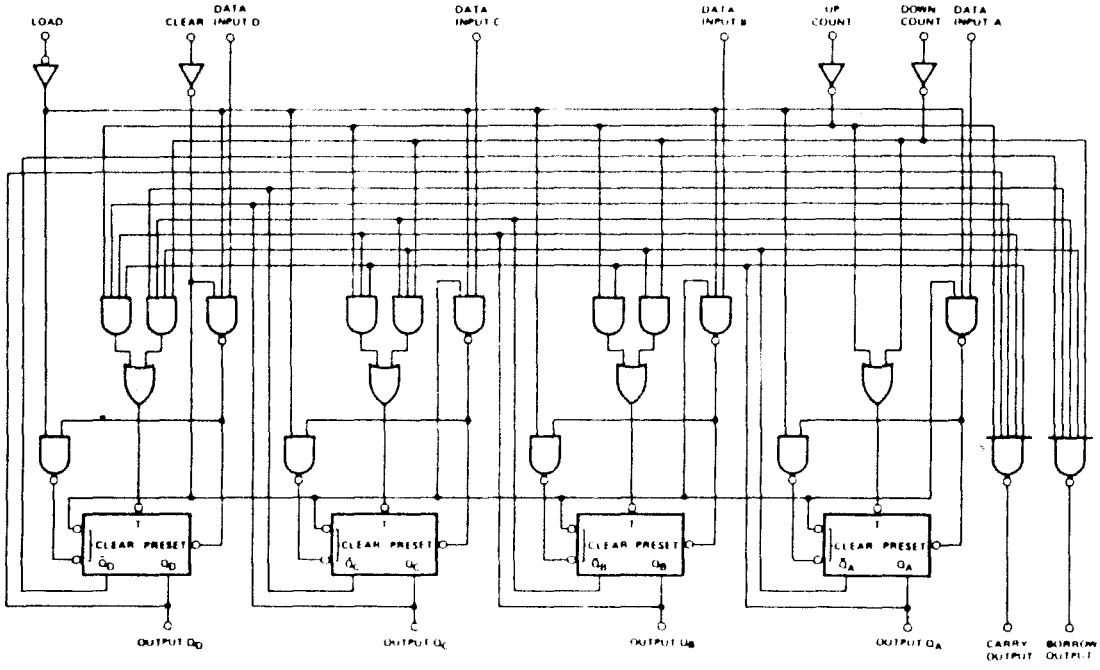
1552-022

Figure 802. Integrated Circuits (Sheet 12 of 15)

S54193B



LOGIC DIAGRAM



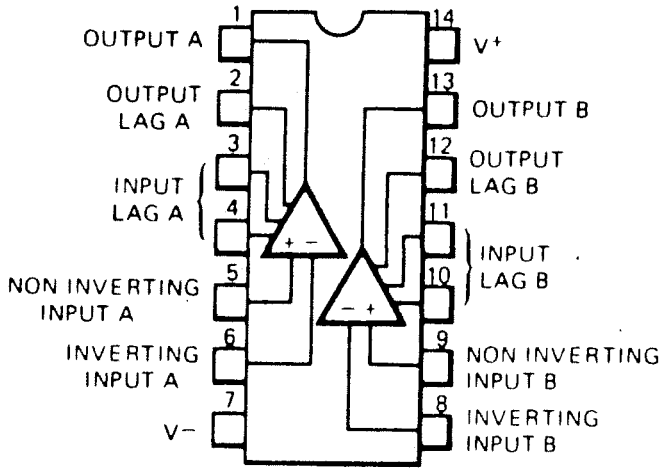
1552-023

Figure 802. Integrated Circuits (Sheet 13 of 15)

U6A7749312

14 LEAD DIP

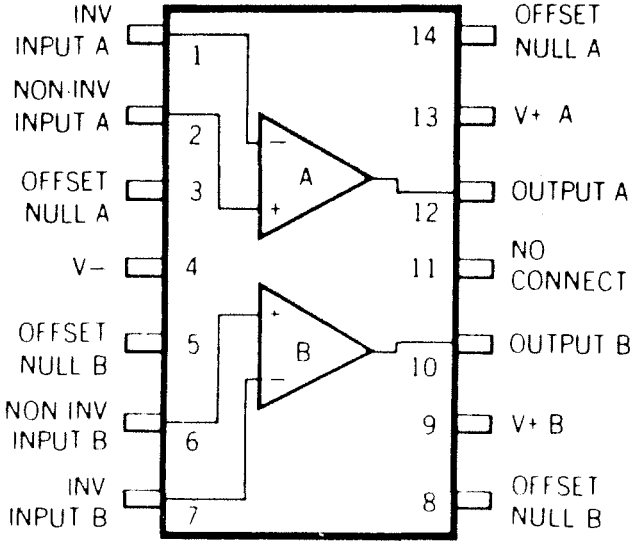
(TOP VIEW)

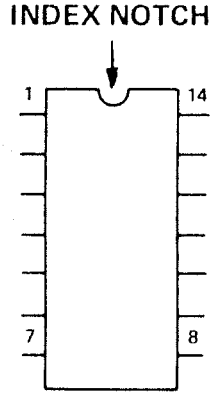


U6W7747312

14 LEAD DIP

(TOP VIEW)

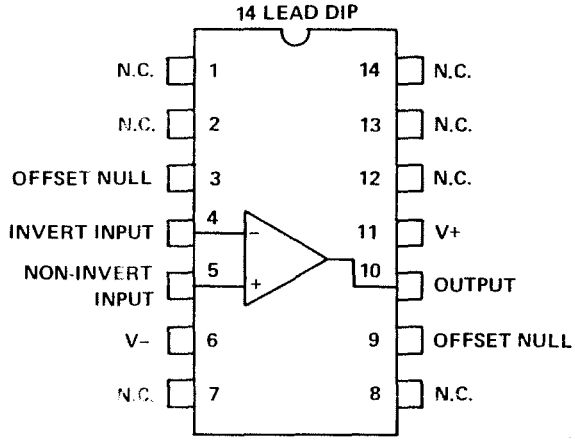




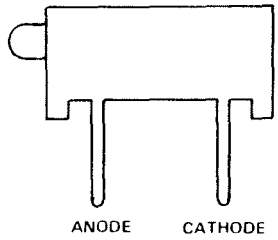
1552-024

Figure 802. Integrated Circuits (Sheet 14 of 15)

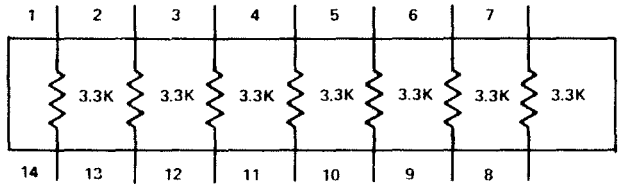
U6A7741312



SC6250-0021-1



899-3-R3.3K



899-3-R100

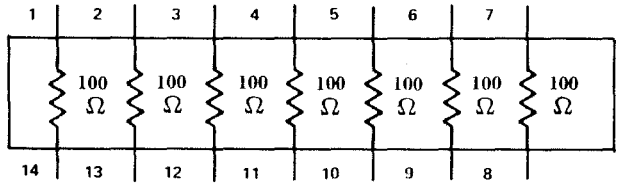


Figure 802. Integrated Circuits (Sheet 15 of 15)

(4) The logic elements known as "OR", "EXCLUSIVE OR", and "AND" are performed by gates. These devices have multiple inputs and a single output.

(5) The OR gate produces a HI output when one or more of the inputs are HI. With all inputs LO, the output is LO.

(6) The EXCLUSIVE OR gate produces a HI output when only one of the two inputs is HI.

(7) The AND gate produces a HI output only when all inputs are HI. When any input is LO the output is LO.

(8) A small circle (schematic-wise) at the output of a gate indicates "negation", which means that the sense of the output logic is reversed. An OR gate with negation is called a NOR gate and an AND gate with negation is called a NAND gate. A NOR gate produces a LO output when one or more of the inputs are HI and a NAND gate produces a LO output only when all inputs are HI.

(9) The flip-flop logic element is the basic data storage element of digital logic. It has two outputs that are always at opposite logic levels; that is, when one output is HI the other output is LO. The flip-flop will remain in a particular state until that state is changed by an input signal.

(10) Remember that the small circle on an input indicates that a LO state is recognized as the true condition. Also, a circle on a clock (or toggle) input indicates that a HI to LO transition causes the element to function.

(11) Two "D-Type" flip-flops (S5474A and SN54174) are used. The operation of these flip-flops is controlled by the signals at their inputs, and is best understood by a careful study of the Truth Tables shown in figure 802.

(12) Several different types of integrated counters are used for various purposes. The various counters and their count capability are as follows:

S5490A - Divide by 2, 5, or 10
S5492A - Divide by 2, 3, 6, or 12
S5493A - Divide by 2, 4, 8, or 16
S54193B - Divide by 2, 5, and 10

(13) These integrated circuits count the number of clock pulses that occur on their toggle inputs, and convert the count to weighted binary form on their output lines. When they have reached the maximum number for which they are used (such as 9, 11, or 15), the next clock pulse returns all counter outputs to zero, from which state it counts upward with subsequent clock pulses. When observing the "D" or 8-weighted output line, it is apparent that this output goes through one cycle each time the required number of input toggles have occurred, thus frequency dividing the input pulses by the required number.

(14) These counters also have the feature that they may be reset to zero at any time, by HI levels on both R_0 inputs. The S5490A also has the capability of being reset to 9 through its R_9 inputs in the same fashion.

(15) The S54164A is an 8-bit serial-in, parallel-out shift register. It is composed of 8 flip-flops, and is used to transfer data in an orderly manner.

(16) The output of each flip-flop in the register is either a HI or LO level, and at each clock pulse the output of each flip-flop is transferred to the input of the one to the right of it.

(17) The output is in parallel form at the output of each flip-flop (only the "true" output of each flip-flop is accessible). Data at the serial input may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the HI-to-LO transition of the clock input.

(18) The S54123B is a dual retriggerable monostable multivibrator. It is triggered to the unstable state by d-c triggering from either HI-to-LO sensing (A) or LO-to-HI sensing (B) inputs. The length of time of the unstable state (output pulse) is determined by the values of resistance and capacitance connected to the C ext and R ext/C ext terminals. The unstable state can be overriden by a LO direct clear input. The retriggerable capability permits the generation of output pulses of indefinitely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at any time, independently of the timing components R and C.

(19) The SN54122J is a single monostable multivibrator. Its operation is identical to that of the S54123B except that it has four inputs. The four inputs determine the output state. Figure 802 presents a Truth Table for the SN54122J.

(20) The S54157B is a quadruple 2-input data selector/multiplexer. This device is a logical implementation of a four-pole, two-position switch with the position of the switch being set by the logic levels supplied to the select inputs. The enable input is LO-active. These devices provide the ability, in one package, to select four bits of either data or control from one of two sources.

(21) The CO-238A-1 is a crystal-controlled logic clock, requiring no signal inputs. The output is a 4-MHz TTL format square-wave.

(22) The U9101 (SC6250-0021-1) is a LED indicator which is fully illuminated when a current of approximately 3 ma is passed through the device.

(23) The MC1563R is a negative voltage regulator. The unregulated voltage is applied to pin 4 and ground. The regulated output voltage appears between pins 6, 8 and ground. A capacitor from pin 3 to ground stabilizes the regulator and reduces output noise voltage. A capacitor connected between pins 5 and 7 also provide regulator stability. The output voltage is determined by the ratio of the resistance between pins 1 and 9 and the resistance between pins 1 and ground. A resistor connected between pins 4 and 5 determine the short circuit current at which the regulator will limit. A capacitor connected from output pins 6, 8 to ground insures low source impedance at high frequencies.

(24) The MC1569R is a positive voltage regulator. The unregulated input voltage is applied to pin 3. The output voltage is determined by the ratio of a resistor connected between pins 6, 9, and 8 and a resistor connected from pin 8 to ground. A capacitor from pin 7 to ground provides output voltage noise filtering. Short circuit current limiting is determined by a resistor and an external NPN transistor connected between pins 1, 4 and 5. A capacitor connected from the regulated output (pin 5) to ground provides low source impedance at high frequencies.

(25) The LM9103 contains circuits to provide TTL-to-high-level interface. Two independent sections provide active pull-up and pull-down capabilities.

(26) The LM106H is a high speed voltage comparator. The output of a voltage comparator provides a logic-level indication of the direction of inequality between the inputs; i.e., + input > - input produces HI output, + input < - input produces LO output. The LM106H also has two strobe inputs which prevent the output from being LO if either of them is LO.

(27) Several operational amplifiers are used. Operational amplifiers have the characteristics of high forward open loop gain and very low input current. The versatility of the operational amplifier results from many types of circuit configurations employing positive and/or negative feedback around the device. The characteristics in a given application are determined by the external feedback elements applied to the device. The operational amplifiers used in the test set are the NH0005, the U6W7747312 (747 type), the U6A7741312 (741 type), and the U6A7749312 (749 type). The NH0005 is a wide bandwidth operational amplifier and is used to amplify the receiver video signal. The U6W774712 is a dual-operational amplifier with internal frequency compensation for stable operation over any closed-loop gain.

(28) The 749 type is also a dual operational amplifier, but is not internally frequency-compensated. It features uncommitted-collector outputs and output disabling capability, and is used as a double-limit voltage comparator. The operational amplifiers have differential inputs and a single output.

(29) The 741 type is a frequency-compensated operational amplifier with a high common mode voltage range and absence of latch-up tendencies. This makes the 741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

(30) Operational amplifiers 747-type are used to perform the following circuit functions:

Voltage Follower
Active Filter
A-C Gain Controlled Amplifier

Integrator
Synchronous Detector
Astable Multivibrator
Precision Monostable Multivibrator
Low-Speed Voltage Comparator
Voltage-Controlled Oscillator
Power-Amplifier Driver
Time-Delay Circuit
Phase-Locked Loop Filter

(31) Two analog switches are used. This device is a TTL logic-controlled switch with a resistance characteristic between switch terminals of approximately 200 ohms in the "ON" state and 10 ohms in the "OFF" state. The analog switches are the AH0014D and AH0015D. The AH0014D is a double-pole, double-throw switch. The AH0015D is a quadruple single-pole, single-throw switch.

(32) The LM9100 is a voltage-controlled oscillator with a center frequency of 160 KHz and a control range of ±24 KHz.

(33) The SN5406A contains 6 inverter, buffer drivers. It features standard TTL inputs with inverted high voltage, high current, open collector outputs.

(34) The SN5475B is a quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock again is high.

(35) The SN5485 is a 4-bit magnitude comparator. It performs magnitude comparison of straight binary or straight BCD (8421) codes. Three fully coded decisions about two 4-Bit words are made and are externally available at three outputs.

(36) The SC5962-0070 is a special programmed read only memory integrated circuit U2001 used on the channel select A7505. Description of input-to-output signals of U2001 is given in the Description and Operation section, paragraphs 2 I (a) through 2 I (g) and figure 16.

B. Replacing Integrated Circuits

The following list identifies the multilayer cards of the test set.

Unit	Cards
Digital Bearing Unit	All cards except the Power Supply Regulator card 100 and the Digital Bearing Unit Monitor card 600.
Signal Analyzer Unit	Signal Processor Card 300
Panel Unit	LED Display card 100 and LED Logic card 200

CAUTION: TO AVOID DAMAGE TO THE MULTILAYER CARDS, FOLLOW THE PRECAUTIONS CONTAINED IN PARAGRAPH C WHILE SERVICING.

C. Precautions

Multilayer cards are actually four printed-circuit cards fused together into a single assembly that appears to be one card. In this "sandwich" all cards are insulated from one another except at those points where interconnection is desired. The two center cards contain printed wiring which carries the desired interconnections. This printed wiring has a low melting temperature, and therefore component removal or installation must be accomplished very carefully to avoid opening the internal connections. The following precautions must be observed:

1. Use a soldering tool of not more than 25 watts.

2. Do not press the tip of the soldering tool against the connection. The tool tip should lightly touch the joint to be heated.

3. Apply only enough heat to cause the solder to flow, then remove the heat.

4. Note the marking identification of the integrated circuit before removal and replace the new one with the same orientation as the one removed.

5. To remove in-line integrated circuits, cut each lead. Remove the integrated circuit and then unsolder one lead at a time and remove lead.

6. Use a vacuum-type solder remover to clean each hole before insertion of the new integrated circuit.

7. Insert the new integrated circuit and solder each connection separately observing caution when applying heat.

8. To remove integrated circuit in cans where the leads are under the integrated circuit, heat each lead separately and remove solder with vacuum solder remover. With solder removed, grasp lead with long nose pliers and move gently. If lead moves freely, assumed that the solder point is free on both sides of the card. Remove integrated circuit, remove any excess solder from holes, and insert new integrated circuit. Solder one lead at a time observing caution when applying heat.

9. In the event that the substitution of a new integrated circuit does not restore normal operation, it is possible that an internal connection has been opened in the repair process. Carefully check for necessary continuity. If there is an open internal connection, restore continuity with a carefully soldered wire on the surface of the card. Keep wire length as short as possible.

4. TEST SET OVERALL PERFORMANCE TEST

This paragraph contains the information necessary to determine the overall performance of the test set. In the event that the requirements of the DME are not met, refer to the Maintenance/Overhaul Manual for KDM 7000 Digital DME, including Service Bulletin No. KDM 7000-2 Special. If the requirements of the other major assemblies of the test set are not met, refer to the Troubleshooting Section. The adjustment procedures for the Digital Bearing Unit and Signal Analyzer Unit are contained in paragraphs 5 and 6 respectively.

A. Minimum Performance Standard Procedures

(1) The minimum performance standards of the test set are verified by first performing the Pre-Operational Procedure given in the Operating Procedures Section (paragraph 3 of Operating Procedures Section). When the Pre-Operational Procedures are performed as part of the minimum performance standards, a 50-ohm dummy load can be used instead of an antenna. If an abnormal indication is obtained during the Pre-Operational Procedures, note the faulty indication.

Perform the test setup as given in figure 803. Remove cover of Digital Bearing Unit and continue with additional procedures given in following paragraphs (2) and (3).

(2) Initial Conditions

(a) Unless otherwise indicated in the procedures, the input signals to the test set (generated by the modified TACAN Beacon Simulator DTS 101A or equivalent) are as follows:

Channel	1
R-F Signal Level	-50 dbm
Range Signal	000 NMI (nautical mile) stationary
Bearing Signal	000 degrees stationary
15 Hz Modulation	20 percent
135 Hz Modulation	20 percent
Antenna Speed	900 RPM
Squitter Rate	2700
MRG Size	Nominal
ARG Size	Nominal
Reply Efficiency	70 Percent

(b) Unless otherwise indicated in the procedures, set switches of Panel Unit to the following positions:

Switch	Position
TACAN	Either position
BEARING	NORMAL
OPERATE/CALIBRATE	OPERATE

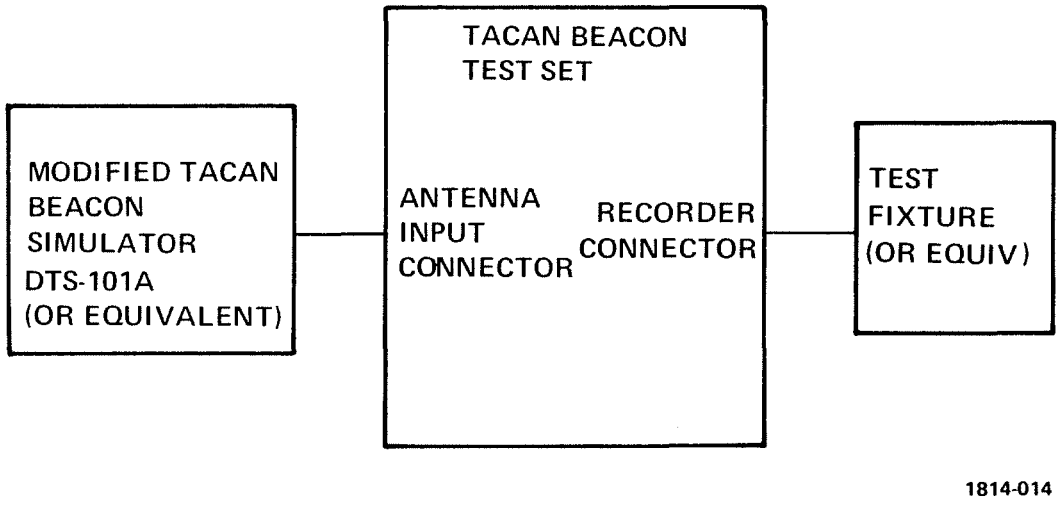


Figure 803. Test Set Up

Switch	Position
SQUITTER	TACAN
OBS CONTROL	MAN
COURSE SELECT DEGREES	000
POWER	OFF

(c) Set CHANNEL/MODE selector to 001X and set 30 DB to OUT position.

(3) Tests

Perform following steps (a) through (cc).

(a) On Panel Unit, set POWER switch to ON position.

(b) Observe that SELF TEST pushbutton/indicator is extinguished. If pushbutton/indicator is not extinguished, depress SELF TEST pushbutton/indicator to extinguish it.

(c) Observe that TRANSMIT pushbutton/indicator is illuminated. If pushbutton/indicator is not illuminated, depress TRANSMIT pushbutton/indicator to illuminate it.

(d) Set IDENTITY VOLUME control to two-thirds of maximum clockwise position.

DME TESTS

(e) Set simulator output r-f level to -90 dbm and range to 100 nautical miles.

NOTE: DME will begin transmitting after approximately 45 seconds and RANGE NAUTICAL MILES will indicate range lock-on by displaying 100.0 ± 0.2 nautical miles. Allow a 30-minute warmup period before continuing with step (f).

(f) Set simulator and test set to each of the following channels (2, 69, and 124) and, for each channel,

observe for test set lock-on by observing RANGE NAUTICAL MILES indicator for a 100.0 ± 0.2 nautical mile range, and a 180-degree bearing on BEARING DEGREES indicator.

(g) On simulator, observe that power output of DME is 500 watts minimum.

(h) Set simulator and test set to channel 69, wait for test set to lock-on and observe that power output of DME is 500 watts minimum.

(i) Repeat step (h) with simulator and test set set to channel 3.

DME RANGE ACCURACY AND TRACKING

(j) Set simulator output r-f level to -80 dbm. Set simulator to each of the following ranges and observe for indications on RANGE NAUTICAL MILES indicator of Panel Unit.

Simulator Range	RANGE NAUTICAL MILES Indication
3.0 NMI	003.0 ± 0.1 NMI
18.0 NMI	018.0 ± 0.2 NMI
108.0 NMI	108.0 ± 0.2 NMI
198.0 NMI	198.0 ± 0.2 NMI

(k) On test set, set TACAN AGC/DME AGC switch (located on left inside of test set) to DME AGC position. Observe that RANGE NAUTICAL MILES indication returns to 198.0 ± 0.2 NMI.

(l) Return TACAN AGC/DME AGC switch to TACAN AGC position.

(m) On simulator, set for a range rate increase of 2000 NMI per hour. Wait for test set to lock-on and observe that range indication on RANGE NAUTICAL MILES indicator tracks indicated range rate increase of simulator.

(n) On simulator, stop range rate increase and set for a range rate decrease of 2000 NMI per hour. Observe that DME unlocks, reacquires and range indication on RANGE NAUTICAL MILES indicator tracks indicated range rate decrease on simulator.

(o) On simulator, stop range rate decrease and set range for 100.0 NMI.

DME SELF TEST

(p) Depress SELF TEST pushbutton/indicator and observe that SELF TEST pushbutton/indicator illuminates.

(q) Observe that RANGE NAUTICAL MILES indicator displays dashes for one second, blanks for approximately one second, then displays 000.0 ± 0.1 nautical miles range. Audio tone should be heard. Observe that RANGE FAILURE indicator illuminates for approximately one second.

DBU TESTS - BEARING ACCURACY

(r) With SELF TEST pushbutton/indicator still illuminated, observe that BEARING DEGREES indication on Panel Unit is 000.0 ± 000.2 degrees. Record indication as plus or minus degrees from zero.

(s) Depress SELF TEST pushbutton/indicator and observe that SELF TEST pushbutton/indicator extinguishes.

(t) On simulator, set 15-Hz and 135-Hz modulation to 8 percent. Set simulator, in turn, to each of the following bearing and r-f power levels. Observe BEARING DEGREES indicator on Panel Unit for each setting. Add or subtract (if necessary and applicable) the calibration difference recorded in step (r). The result of this addition or subtraction should correspond to the Corrected Bearing Reading column that follows:

Simulated Bearing	Simulator R-F Level	Corrected Bearing Reading
20°	-85 dbm	200 ± 1.2° rms
110°	-85 dbm	290 ± 1.2° rms
200°	-85 dbm	20 ± 1.2° rms
290°	-85 dbm	110 ± 1.2° rms
20°	-20 dbm	200 ± 0.4° rms
110°	-20 dbm	290 ± 0.4° rms
200°	-20 dbm	20 ± 0.4° rms
290°	-20 dbm	110 ± 0.4° rms
20°	-79 dbm	200 ± 0.4° rms
110°	-79 dbm	290 ± 0.4° rms
200°	-79 dbm	20 ± 0.4° rms
290°	-79 dbm	110 ± 0.4° rms

(u) On simulator, set r-f level to -85 dbm. Set simulator output for a bearing slew rate of 3 degrees per second. Observe that indication on BEARING DEGREES indicator of Panel Unit changes in a linear fashion and that when the output of the simulator is 0 degrees, the BEARING DEGREES indication is approximately 180.0 degrees.

(v) Repeat steps (t) and (u) with 15-Hz modulation and 135-Hz modulation set to 27 percent.

(w) Set simulator to provide a beacon signal with only 15-Hz information present at 25-percent modulation. On Panel Unit, set BEARING switch to 15 Hz ONLY position. On Panel Unit, set OPERATE/CALIBRATE switch to CALIBRATE position. Observe that BEARING DEGREES indication is 010.0 ± 001.0 degrees. Record indication as plus or minus degrees from ten.

(x) Set OPERATE/CALIBRATE switch to OPERATE position.

(y) On simulator, set output for each of the following bearings and r-f power levels. Observe BEARING DEGREES indicator on Panel Unit for each setting. Add or subtract the calibration difference recorded in step (w). The result of this addition or subtraction should correspond to the Corrected Bearing Reading column that follows:

Simulated Bearing	Simulator R-F Level	Corrected Bearing Reading
20°	-85 dbm	200 ± 5.2° rms
110°	-85 dbm	290 ± 5.2° rms
200°	-85 dbm	20 ± 5.2° rms
290°	-85 dbm	110 ± 5.2° rms
20°	-20 dbm	200 ± 1.2° rms
110°	-20 dbm	290 ± 1.2° rms
200°	-20 dbm	20 ± 1.2° rms
290°	-20 dbm	110 ± 1.2° rms
20°	-80 dbm	200 ± 1.2° rms
110°	-80 dbm	290 ± 1.2° rms
200°	-80 dbm	20 ± 1.2° rms
290°	-80 dbm	110 ± 1.2° rms

(z) On simulator, set r-f power level to -85 dbm. Set simulator output for a bearing slew rate of 3 degrees per second. Observe that indication on BEARING DEGREES indicator of Panel Unit changes in a linear fashion and when the output of the simulator is 0 degrees, the BEARING DEGREES indication is approximately 180.0 degrees.

DBU ACQUISITION TIME

(aa) Set simulator as indicated on Initial Condition paragraph 3.A.(2)(a). Set BEARING switch on Panel Unit to NORMAL position.

(ab) Set CHANNEL/MODE selector to channel 011X, allow Digital Bearing Unit to go into search condition (dashes on BEARING DEGREES indicator of Panel Unit), and then return CHANNEL/MODE selector to channel 001X. Observe that Digital Bearing Unit locks on and provides a bearing indication on BEARING DEGREES indicator within 5 seconds of return of the CHANNEL/MODE selector to channel 001X.

DBU TRACKING RATE (NORMAL)

(ac) On simulator, set modulation level of 15 Hz and 135 Hz at 8 percent. Set simulator output for a bearing slew rate of 3 degrees per second. Observe that Digital Bearing Unit maintains lock-on by observing that BEARING DEGREES indication follows bearing output of simulator (approximately) except that it is 180-degrees out-of-phase.

(ad) Repeat step (ac) with 15-Hz and 135-Hz modulation output of simulator at 27 percent.

DBU TRACKING RATE (15-Hz ONLY)

(ae) Set simulator to provide a beacon signal with only 15-Hz information present. Set modulation level to 25 percent. On Panel Unit, set BEARING switch to 15 Hz ONLY position.

(af) Allow Digital Bearing Unit to lock on to simulator signal, then set simulator for a bearing slew rate of 3 degrees per second. Observe that Digital Bearing Unit maintains lock-on as evidenced by indication on BEARING DEGREES indicator of Panel Unit.

DBU MEMORY TIME

(ag) Set simulator output as indicated in Initial Conditions paragraph 3.A.(2)(a).

(ah) On Panel Unit, set BEARING switch to NORMAL position.

(ai) Allow Digital Bearing Unit to lock on to simulator and, after at least 10 seconds, increase simulator r-f output attenuation to -120 db or greater. Observe that BEARING DEGREES continues to display approximately 180 degrees for 6 ± 1 second and then unlocks (BEARING DEGREES indicator displays dashes).

15-Hz PERCENT MODULATION

(aj) Set simulator to provide 15-Hz modulation only and r-f attenuation to -50 db.

(ak) On test set, set PERCENT switch to 15 HZ MOD position. Determine that test fixture (or equivalent) is connected to RECORDER connector on test set (see figures 803 and 804). Connect digital voltmeter between TP1 (15 HZ LEVEL) and TP9 (GND) on test fixture.

(al) Set simulator, in turn, to each of the following percent modulation and observe for indications on digital voltmeter and PERCENT meter.

Percent Modulation	Digital Voltmeter Indication	PERCENT Meter Indication
0%	0 to + 0.5 Vdc	0 to 2%
10%	2.5 ± 0.5 Vdc	10 ± 2%
20%	5.0 Vdc*	20%*
30%	7.5 ± 0.5 Vdc	30 ± 2%
39%	9.75 ± 0.5 Vdc	39 ± 2%

* Test set adjusted for this indication

135-Hz PERCENT MODULATION

(am) Set simulator to provide 135-Hz modulation only.

(an) On test set, set PERCENT switch to 135 HZ MOD position. Connect digital voltmeter between TP2 (135 HZ LEVEL) and TP9 (GND) on test fixture. Set simulator, in turn, to each of the following percent modulations and observe indications on digital voltmeter and PERCENT meter.

Percent Modulation	Digital Voltmeter Indication	PERCENT Meter Indication
0%	0 to 0.5 Vdc	0 to 2%
10%	2.5 ± 0.5 Vdc	10 ± 2%
20%	5.0 Vdc*	20%*
30%	7.5 ± 0.5 Vdc	30 ± 2%
39%	9.75 ± 0.5 Vdc	39 ± 2%

* Test Set Adjusted for this indication

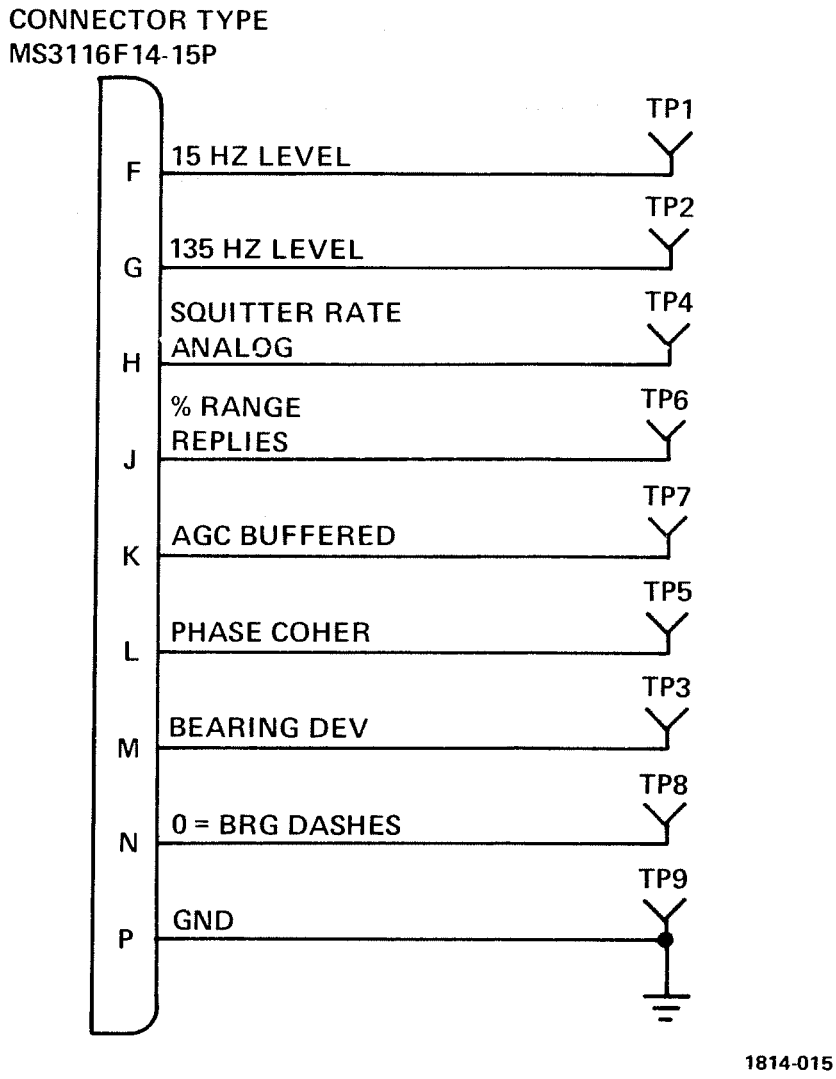


Figure 804. Test Fixture Wiring Diagram

DBU MONITOR CARD AND BEARING FAILURE INDICATOR CHECK

(ao) Sequentially ground each of the following Digital Bearing Unit test points. After grounding each test point, observe that associated LED indicator on the Digital Bearing Unit Monitor card illuminates and the BEARING FAILURE indicator on the Panel Unit illuminates. When ground is removed, associated LED and BEARING FAILURE indicator extinguishes.

Test Point	LED Indicator
TP409	REF CTR
TP210	MEM CTR
TP504	PLS DEC
TP306	VID PCR
TP104	PWR REG

SAU BEARING DEVIATION

(ap) Set simulator as indicated in Initial Conditions paragraph 3.A.(2)(a). Connect a 1000-ohm precision resistor between test points TP3 (BEARING DEV) and TP9 (GND) on test fixture. Connect digital voltmeter across this resistor.

(aq) Set simulator to produce a 000.0 indication on BEARING DEGREES indicator of Panel Unit.

(ar) On Panel Unit, set COURSE SELECT DEGREES control, in turn, to each of the following settings. At each setting, observe digital voltmeter and COURSE DEVIATION DEGREES meter indication.

COURSE SELECT Setting	Digital Voltmeter Indication	COURSE DEVIATION DEGREES Meter Indication
000	0 ± 3.5 mv	0 ± 0.2 degrees
005	+75 ± 3.5 mv	+5 ± 0.2 degrees
010	+150 ± 3.5 mv	+10 ± 0.2 degrees
355	-75 ± 3.5 mv	-5 ± 0.2 degrees
350	-150 ± 3.5 mv	-10 ± 0.2 degrees

(as) Observe that FROM indicator on Panel Unit is illuminated.

(at) Set COURSE SELECT DEGREES control on Panel Unit to 180 degrees. Observe that TO indicator on Panel Unit is illuminated.

(au) Disconnect 1000-ohm resistor and digital voltmeter from test fixture.

(av) On Panel Unit, set OBS CONTROL to AUTO position.

(aw) Set simulator to produce a bearing slew rate of 1 degree per second. Observe signal bearing on simulator versus COURSE DEVIATION DEGREES meter indication for normal conditions as follows:

Bearing	COURSE DEVIATION DEGREES Meter Indication
0°	Centered (0 degrees)
0° to 5°	Needle moves to left at bearing slew rate, then suddenly moves to +5 degrees.
5° to 10°	Needle moves from right (+5 degrees) towards center at bearing slew rate. Indicates center at 10° bearing.
10° to 15°	Needle moves from center to left at bearing slew rate, then suddenly moves to +5 degrees.

(ax) Observe that FROM indicator on Panel Unit is illuminated.

SAU ANTENNA SPEED

(ay) Set simulator to provide following antenna speeds. For each speed, observe status of ANT. SPEED ± 1.8 RPM UNDER/OVER LEDS on Panel Unit and indication on ANTENNA SPEED RPM meter.

Antenna Speed Switch Position	UNDER LED	OVER LED	ANTENNA SPEED RPM Meter Indication
OVER	Extinguished	Illuminated	Greater than 901.8 rpm
UNDER	Illuminated	Extinguished	Less than 898.2 rpm
NOMINAL	Extinguished	Extinguished	Between 898.2 and 901.8 rpm

SAU SQUITTER RATE

(az) Connect digital voltmeter between test points TP4 (SQUITTER RATE ANALOG) and TP9 (GND) on test fixture. On test set, set PERCENT switch to SQUITTER position.

(ba) On Panel Unit, set BEARING switch to NORMAL position and SQUITTER switch to TACAN position. On simulator, set squitter rate to each of the following rates while observing SQUITTER RATE ±5% UNDER/OVER LEDS, PERCENT meter indication, and digital voltmeter indication.

Squitter Rate	UNDER LED	OVER LED	Digital Voltmeter Indication	PERCENT Meter Indication
2500	Illuminated	Extinguished	——	——
2900	Extinguished	Illuminated	——	——
2700	Extinguished	Extinguished	——	——

(bb) On Panel Unit, set SQUITTER switch to DME position. On simulator, set squitter rate to each of the following rates while observing SQUITTER RATE ±5% UNDER/OVER LEDS, PERCENT meter indication, and digital voltmeter indication.

Squitter Rate	UNDER LED	OVER LED	Digital Voltmeter Indication	PERCENT Meter Indication
600	Illuminated	Extinguished	——	——
2900	Extinguished	Illuminated	——	——
2700	Extinguished	Extinguished	——	——

PHASE COHERENCEY CHECK

(bc) Set simulator such that 15-Hz phase indicates following listed values and, for each setting, observe PHASE COHER ±5° UNDER/OVER LEDS on Panel Unit and PHASE COHERENCY DEGREES meter.

15-Hz Phase	UNDER LED	OVER LED	PHASE COHERENCY DEGREES Meter Indication
+6°	Extinguished	Illuminated	+6 degrees
-6°	Illuminated	Extinguished	-6 degrees
+4°	Extinguished	Extinguished	+4 degrees
-4°	Extinguished	Extinguished	-4 degrees

(bd) Connect a 1000-ohm precision resistor between test point TP5 (PHASE COHER) and TP9 (GND) on test fixture. Connect a VOM across 1000-ohm resistor. Set simulator such that 15-Hz phase indicates following listed values and, for each setting, observe phase difference d-c analog voltage on VOM and indication on PHASE COHERENCY DEGREES meter.

15-Hz Phase	VOM Indication	PHASE COHERENCY DEGREES Meter Indication
15	+7.5 ± 0.5 Vdc	+15 degrees
10	+5.0 ± 0.5 Vdc	+10 degrees
0	0.0 ± 0.5 Vdc	0 degrees
-10	-5.0 ± 0.5 Vdc	-10 degrees
-15	-7.5 ± 0.5 Vdc	-15 degrees

MRG SIZE

(be) On simulator, set MRG switch to positions as follows and, for each position, note status of MRG SIZE UNDER/OVER LEDS on Panel Unit.

MRG Size Switch Position	UNDER LED	OVER LED
MRG Over	Extinguished	Illuminated
MRG Under	Illuminated	Extinguished
MRG Nominal	Extinguished	Extinguished

ARG SIZE

(bf) On simulator, set ARG switch to positions as follows and, for each position, note status of ARG SIZE UNDER/ OVER LEDS on Panel Unit.

ARG Size Switch Position	UNDER LED	OVER LED
ARG Over	Extinguished	Illuminated
ARG Under	Illuminated	Extinguished
ARG Nominal	Extinguished	Extinguished

ARG COUNT

(bg) On simulator, set ARG size control to delete one ARG per cycle and observe that ARG COUNT UNDER indicator illuminates.

(bh) Set ARG size control to normal.

PERCENT RANGE REPLIES

(bi) Connect digital voltmeter between test points TP6 (% RANGE REPLIES) and TP9 (GND). On test set, set PERCENT switch to RANGE REPLIES position. On simulator, set Efficiency Reply control in turn to each of the following percent replies. Observe for nominal voltage on digital voltmeter and for indication on PERCENT meter.

Percent Reply	Mean D-C Voltage Indication on Digital Voltmeter	PERCENT Meter Indication (Approx)
40%	4 Vdc	40%
50%	5 Vdc	50%
60%	6 Vdc	60%
80%	8 Vdc	80%

OSCILLOSCOPE SYNC OUTPUTS

(bj) Determine that vertical and horizontal inputs to oscilloscope are connected to SYNC connector on test set.

(bk) On test set, set SYNC switch to MRG position and observe waveform on oscilloscope. See waveform A, figure 805.

(bl) On test set, set SYNC switch to ARG position and observe waveform on oscilloscope. See waveform B, figure 805.

(bm) On test set, set SYNC switch to RANGE INTERROGATE position and observe waveform on oscilloscope. See waveform C, figure 805.

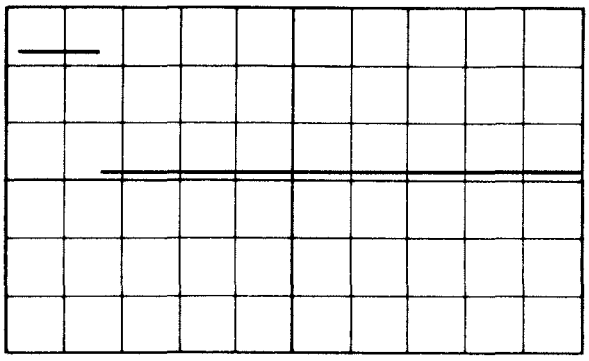
(bn) On test set, set SYNC switch to RANGE REPLY position and observe waveform on oscilloscope. See waveform D, figure 805.

AGC OUTPUT

(bo) Connect 1000-ohm precision resistor between test point TP7 (AGC BUFFERED) and TP9 (GND). Connect digital voltmeter across 1000-ohm resistor.

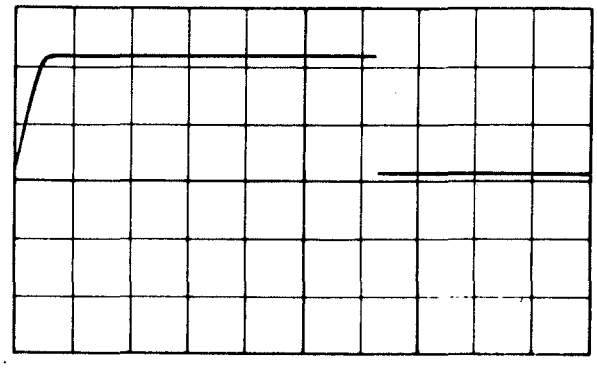
(bp) Set simulator R-F output attenuation to -120 db or greater and observe that AGC BUFFERED voltage is 7 volts or greater.

A



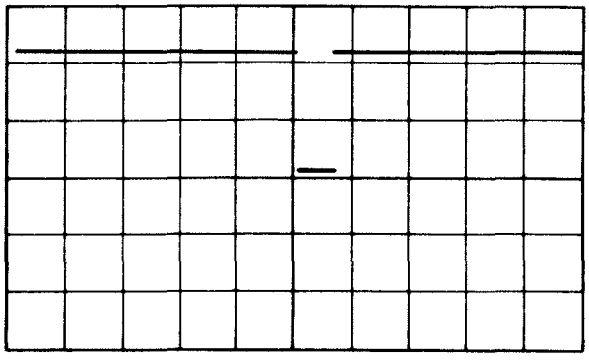
MRG SCOPE SYNC .5MS/CM
INT SYNC 2V/CM
SLOPE +

C



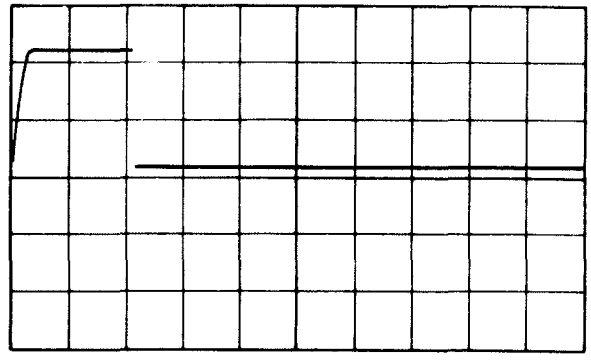
RANGE INTRG SCOPE SYNC 5μS/CM
INT SYNC 2V/CM
SLOPE +

B



ARG SCOPE SYNC 10MS/CM
INT SYNC 2V/CM
SLOPE +

D



RANGE REPLY SCOPE SYNC 5μS/CM
INT SYNC 2V/CM
SLOPE +

1552-152

Figure 805. Oscilloscope Sync Waveforms

Y-MODE OPERATION

(bq) Set CHANNEL/MODE selector to 001Y and set 30 DB to OUT position.

(br) Set simulator controls as indicated in paragraph 4A.(2)(a).

(bs) Set simulator for an r-f level of -80 dbm on channel 001, Y mode, 100-mile range.

(bt) Observe for test set lock-on by observing RANGE NAUTICAL MILES indicator for a 100.0 ± 0.2 nautical mile range, and a 180-degree bearing on BEARING DEGREES indicator.

ATTENUATOR CHECK

(bu) Observe indication on AGC VOLTS meter and record indication.

(bv) On simulator, set r-f level to -50 dbm.

(bw) On test set, set 30 DB to 30 DB position. Wait for test set to lock-on and observe that AGC VOLTS meter indication is approximately the same as recorded in step bu.

ADDITIONAL OUTPUTS

(bx) Set simulator for X-mode operation on channel 001, 0-degree bearing.

(by) Set test set CHANNEL/MODE selector to 001X.

(bz) Connect oscilloscope vertical input to SUPPR connector on test set.

(ca) Wait for test set to lock-on and observe waveform on oscilloscope. See waveform A, figure 806.

(cb) Connect oscilloscope vertical input to TRANSMIT PULSE connector on test set and observe waveform on oscilloscope. See waveform B, figure 806.

(cc) Connect oscilloscope vertical input to VIDEO connector on test set and observe waveform on oscilloscope. See waveform C, figure 806.

5. DIGITAL BEARING UNIT ADJUSTMENT PROCEDURES

Controls are provided for adjusting the outputs of the +12 V and -12 V d-c power supplies, the 15-Hz filter, 135-Hz filter, 15-Hz level, and 135-Hz level. Perform test hookup as illustrated on figure 803. On Panel Unit, set POWER switch to ON position. Allow Digital Bearing Unit to warm up for 30 minutes before performing adjustments. Identification of the Digital Bearing Unit controls is as follows:

Variable Resistor	Adjustment For
R103	+12 V d-c output
R108	-12 V d-c output
R304	15-Hz filter
R310	135-Hz filter
R314	15-Hz level
R316	135-Hz level

A. Power Supply Adjustment Procedure

Perform following steps (1) through (4).

(1) Connect digital voltmeter between TP103 and chassis ground.

(2) Adjust R103 for an indication of +12.000 ± 0.002 V dc.

(3) Connect digital voltmeter between TP104 and chassis ground.

(4) Adjust R108 for an indication of -12.000 ± 0.002 V dc.

B. 15-Hz Filter and 135-Hz Filter Adjustment Procedures

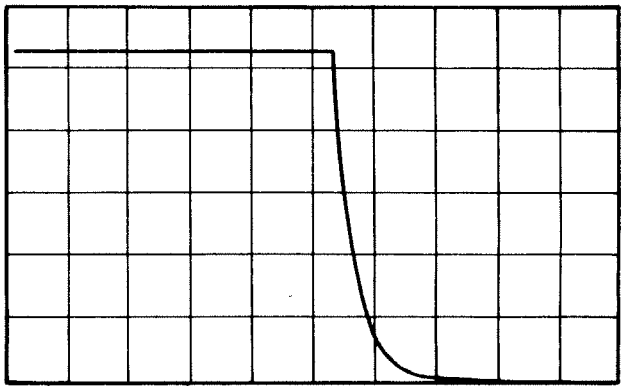
Perform following steps (1) through (4).

(1) On Panel Unit, set switches as follows:

OPERATE/CALIBRATE - CALIBRATE

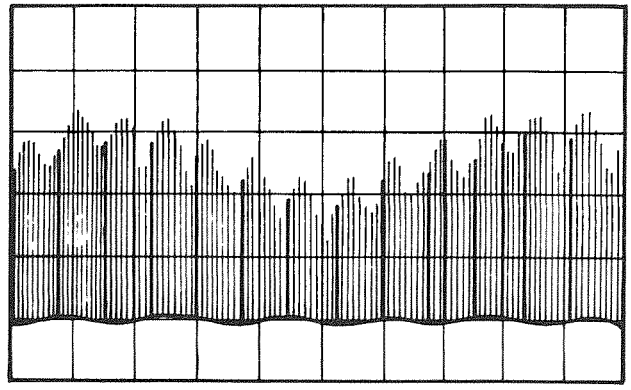
BEARING - 15 Hz ONLY

A



SUPPR — 5 μSEC/CM
INT SYNC — 5 V/CM
SLOPE + — X MODE

C



VIDEO — 10 MS/CM
EXT SYNC — 2 V/CM
SLOPE + — 0° BEARING

NOTE

SYNCHRONIZE OSCILLOSCOPE ON MRG FROM SIMULATOR

B

TRANSMIT PULSE — 5 μSEC/CM
EXT SYNC — 5 V/CM
SLOPE + — X MODE

NOTE

SYNCHRONIZE OSCILLOSCOPE ON SUPPR PULSE (WAVEFORM A)

1814-013

Figure 806. Test Set Additional Outputs

(2) Adjust R304 until BEARING DEGREES indicator on Panel Unit indicates 010.0 ± 000.2 degrees.

(3) Set BEARING switch to NORMAL position.

(4) Adjust R310 until BEARING DEGREES indicator on Panel Unit indicates 000.0 ± 000.2 degrees.

C. 15-Hz Level and 135-Hz Level Adjustment Procedures

Perform following steps (1) through (8).

(1) On Panel Unit, set OPERATE/CALIBRATE switch to OPERATE position. Determine SELF TEST pushbutton/indicator is extinguished (test set in operate mode).

(2) Determine that simulator is energized and that 15-Hz output is set for 20-percent modulation and that 135-Hz output is set for 0-percent modulation (no output).

(3) Set CHANNEL/MODE selector to simulator output and determine that Digital Bearing Unit is locked-on.

(4) Connect digital voltmeter between test points TP1 (15-Hz LEVEL) and TP9 (GND) on test fixture.

(5) Adjust R314 until digital voltmeter indicates 5.0 ± 0.1 V dc.

(6) Set simulator for 135-Hz output at 20-percent modulation.

(7) Connect digital voltmeter between test points TP2 (135-Hz LEVEL) and TP9 (GND) on test fixture.

(8) Adjust R316 until digital voltmeter indicates 5.0 ± 0.1 V dc.

6. SIGNAL ANALYZER UNIT ADJUSTMENT PROCEDURES

Controls are provided for adjusting the outputs of the +15 V and -15 V d-c power supplies, the phase coherency circuit, the bearing deviation circuit, the percent of range reply circuit, AGC circuit, and the squitter rate circuit. Perform test hookup as illustrated on figure 803. On Panel Unit, set POWER switch to ON position. Allow Signal Analyzer Unit to warm up for 30 minutes before performing adjustments. Identification of Signal Analyzer Unit controls is as follows:

Variable Resistor	Adjustment For
R103	+15 V d-c output
R108	-15 V d-c output
R305	Phase Coherency
R308	Phase Coherency
R306	Bearing Deviation
R307	Bearing Deviation
R309	Percent Range Reply
R310	AGC
R201	Squitter Rate

A. Power Supply Adjustment Procedure

Perform following steps (1) through (4).

(1) Connect digital voltmeter between TP103 and chassis ground.

(2) Adjust R103 for an indication of +15.000 ± 0.002 V dc.

(3) Connect digital voltmeter between TP104 and chassis ground.

(4) Adjust R108 for an indication of -15.00 ± 0.002 V dc.

B. Phase Coherency Adjustment Procedure

Perform following steps (1) through (6).

(1) Adjust simulator for a +10-degree 15-Hz phase output. Connect digital voltmeter to TP309 and record voltage indication.

(2) Adjust simulator for a -10-degree 15-Hz phase output. Record voltage indication at TP309.

(3) Add absolute value of voltage indications obtained in steps (1) and (2).

(4) Repeat steps (1) through (3) and adjust R308 until absolute value obtained is 10.0 ± 0.5 V dc.

(5) Adjust simulator for a 0-degree 15-Hz phase output.

(6) Adjust R305 until digital voltmeter indicates 0.0 ± 0.5 V dc.

C. Bearing Deviation Adjustment Procedure

Perform following steps (1) through (6).

(1) Adjust simulator until BEARING DEGREES indication on Panel Unit is 005.0 degrees.

(2) Connect digital voltmeter between TP302 and chassis ground, and record voltage.

(3) Adjust simulator until BEARING DEGREES indication on Panel Unit is 355.0 degrees.

(4) Record voltage indication on digital voltmeter.

(5) Add absolute value of voltage indication recorded in steps (2) and (4).

(6) Repeat steps (1) through (5) and adjust R307 until absolute value is 10.0 ± 0.2 V dc.

(7) Adjust simulator until BEARING DEGREES indication on Panel Unit is 000.0 degrees.

(8) Adjust R306 until digital voltmeter indicates 0.0 ± 0.2 V dc.

D. Percent of Range Reply Adjustment Procedure

Perform following steps (1) through (3).

(1) Adjust simulator for a 70 percent reply efficiency.

(2) Connect digital voltmeter between test points TP6 (% RANGE REPLIES) and TP9 (GND) on test fixture.

(3) Adjust R309 until digital voltmeter indicates 7 V dc (nominally).

NOTE: Voltage will vary with time as a function of the simulator.

E. AGC Adjustment Procedure

Perform following steps (1) through (4).

(1) Connect digital voltmeter between TP306 and chassis ground.

(2) Connect ammeter in series with 50-ohm resistor between test points TP7 (AGC BUFFERED) and TP9 (GND) on test fixture.

(3) Adjust simulator r-f level output until digital voltmeter connected at TP306 indicates 7.0 V dc.

(4) Adjust R310 for a 4-milliampere indication on ammeter.

F. Squitter Rate Adjustment Procedure

Perform following steps (1) through (3).

(1) Connect digital voltmeter between TP201 and chassis ground.

(2) Adjust simulator squitter rate output for 2700 pulse pairs per second.

(3) Adjust R201 for a 10.0 ± 0.2 V d-c indication on digital voltmeter.

7. METER CALIBRATION CHECK

The calibration check for the meters of the TACAN Beacon Test Set is contained in paragraphs A through E. If the check reveals that a meter does not fall within the applicable tolerances, refer to meter calibration correction information contained in paragraph 8.

A. Antenna Speed Meter

Following steps (1) through (10) contain the calibration check for the ANTENNA SPEED meter.

(1) Remove Signal Analyzer Unit and Digital Bearing Unit from their mounting racks.

(2) Determine that power supply (Power Designs Inc. Model 4010 or equivalent) output is set to 0 V dc. Connect positive output of power supply to standoff terminal that is mounted on

top of positive meter terminal (precision 10,000-ohm resistor is connected to this standoff terminal).

(3) Connect negative output of supply to negative meter terminal (black wire connects to this terminal).

(4) Increase power supply voltage output slowly until ANTENNA SPEED meter indicates exactly full scale (meter deflection is to the right of center).

(5) Connect digital voltmeter (Fluke Model 8100A or equivalent) across precision 10,000-ohm resistor (R7506) connected between standoff terminal and lug mounted under standoff terminal.

(6) Observe that digital voltmeter indications is 5.000 ± 0.002 V dc.

(7) Reduce power supply output to 0 V dc and reverse supply lead connections such that standoff terminal is now negative and negative meter terminal is now positive.

(8) Increase power supply output slowly until ANTENNA SPEED meter indicates exactly full scale (meter deflection is to left of center).

(9) With digital voltmeter connected as indicated in step (5), observe that indication is 5.000 ± 0.002 V dc.

(10) Reduce power supply output to 0 V dc and remove power supply and digital voltmeter leads from Test Set.

B. AGC VOLTS Meter

Following steps (1) through (6) contain the calibration check for the AGC VOLTS meter.

(1) Remove Signal Analyzer Unit and Digital Bearing Unit from their mounting racks.

(2) Determine that power supply (Power Designs Inc. Model 4010 or equivalent) output is set to 0 V dc. Connect positive output of power supply to positive terminal of meter (white/black/grey wire).

(3) Connect negative output of power supply to negative meter terminal (black wire).

(4) Increase power supply output voltage slowly until AGC VOLTS meter indicates exactly full scale (meter deflection is to the right of zero).

(5) Connect digital voltmeter (Fluke Model 8100A or equivalent) across power supply output and observe a reading of 10.000 ± 0.004 V dc.

(6) Reduce power supply output to 0 V dc and remove power supply and digital voltmeter leads from Test Set.

C. COURSE DEVIATION DEGREES Meter

Following steps (1) through (10) contain the calibration check for the COURSE DEVIATION DEGREES meter.

(1) Remove Signal Analyzer Unit from its mounting rack.

(2) Determine that power supply (Power Designs Inc. Model 4010 or equivalent) output is set to 0 V dc. Connect positive output of power supply to standoff terminal that is mounted on top of the positive meter terminal (precision 20,000-ohm resistor is connected to this standoff terminal).

(3) Connect negative output of supply to negative meter terminal (black wire connects to this terminal).

(4) Increase power supply voltage output slowly until COURSE DEVIATION DEGREES meter indicates exactly full scale (meter deflection is to the right of center).

(5) Connect digital voltmeter (Fluke Model 8100A or equivalent) across precision 20,000-ohm resistor (R7508) connected between standoff terminal and lug mounted under standoff.

(6) Observe for a digital voltmeter indication of 10.000 ± 0.003 V dc.

(7) Reduce power supply output to 0 V dc and reverse supply lead connections such that standoff terminal is now negative and negative meter terminal is now positive.

(8) Increase power supply output slowly until COURSE DEVIATION DEGREES meter indicates exactly full scale (meter deflection is to the left of center).

(9) With digital voltmeter connected as indicated in step (5), observe that indication is 10.000 ± 0.003 V dc.

(10) Reduce power supply output to 0 V dc and remove power supply and digital voltmeter leads from Test Set.

D. PHASE COHERENCY DEGREES Meter

Following steps (1) through (10) contain the calibration check for the PHASE COHERENCY DEGREES meter.

(1) Remove Signal Analyzer Unit from its mounting rack.

(2) Determine that power supply (Power Designs Inc. Model 4010 or equivalent) output is set to 0 V dc. Connect positive output of power supply to standoff terminal that is mounted on top of the positive meter terminal (a precision 20,000-ohm resistor is connected to this standoff terminal).

(3) Connect negative output of supply to negative meter terminal (black wire connects to this terminal).

(4) Increase power supply voltage output slowly until PHASE COHERENCY DEGREES meter indicates exactly full scale (meter deflection is to the right of center).

(5) Connect digital voltmeter (Fluke Model 8100A or equivalent) across precision 20,000-ohm resistor (R7509) connected between standoff terminal and lug mounted under standoff.

(6) Observe for a digital voltmeter indication of 10.000 ± 0.003 V dc.

(7) Reduce power supply output to 0 V dc and reverse supply lead connections such that standoff terminal is now negative and negative meter terminal is now positive.

(8) Increase power supply output slowly until PHASE COHERENCY DEGREES meter indicates exactly full scale (meter deflection is to left of center).

(9) With digital voltmeter connected as indicated in step (5), observe that indication is 10.000 ± 0.003 V dc.

(10) Reduce power supply output to 0 V dc and remove power supply and digital voltmeter leads from Test Set.

E. PERCENT Meter

Following steps (1) through (13) contain the calibration check for the PERCENT meter.

(1) Remove Signal Analyzer Unit and Digital Bearing Unit from their mounting racks.

(2) Determine that power supply (Power Designs Inc. Model 4010 or equivalent) output is set to 0 V dc. Connect positive output of power supply to terminal 1 of the rear deck of PERCENT switch S7502 (white/brown wire).

(3) Connect negative output of supply to negative meter terminal (black wire).

(4) Set PERCENT switch S7502 in 15 Hz MOD position.

(5) Increase power supply output voltage slowly until PERCENT meter indicates exactly full scale (meter deflection is to the right).

(6) Connect digital voltmeter (Fluke Model 8100A or equivalent) across precision 12,400-ohm resistor (R7502) connected between front and rear decks of switch S7502.

(7) Observe that digital voltmeter indication is 12.400 ± 0.400 V dc.

(8) Reduce power supply output to 0 V dc and connect positive terminal of the supply to terminal 4 of the rear deck of PERCENT switch S7502 (white/violet wire).

(9) Set PERCENT switch S7502 to RANGE REPLIES position.

(10) Increase power supply output voltage slowly until PERCENT meter indicates exactly full scale (meter deflection is to the right).

(11) Connect digital voltmeter across precision 10,000-ohm resistor (R7503) connected between front and rear decks of PERCENT switch S7502.

(12) Observe that digital voltmeter indication is 10.000 ± 0.200 V dc.

(13) Reduce power supply output to 0 V dc and remove power supply and digital voltmeter leads from Test Set.

8. METER CALIBRATION CORRECTION INFORMATION

A. AGC Volts Meter

If the calibration check indicates that the AGC VOLTS meter is out of calibration, replace the meter.

B. PERCENT, COURSE DEVIATION DEGREES, PHASE COHERENCY DEGREES, and ANTENNA SPEED RPM Meters

If the calibration check indicates that one of these meters is out of calibration, first check the associated meter calibration resistor (for signs of damage) as follows:

PERCENT Meter M7503 - R7502, R7503

COURSE DEVIATION DEGREES Meter M7504 - R7508

PHASE COHERENCY DEGREES Meter M7505 - R7509

ANTENNA SPEED RPM Meter M7501 - R7506

Resistors with values other than those initially provided with the Test Set may be substituted to correct meter calibration; however, these resistor values must be within ±15 percent of the original value. If this fails to provide indications within calibration tolerances, then the meter must be replaced.

CONTENTS
TROUBLESHOOTING

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2.	Fault Indicator Analysis	902
3.	Troubleshooting Sequence Charts	903
4.	Troubleshooting Flow Charts	903
5.	Waveform Data	903
6.	Test Set Troubleshooting	903
7.	Digital Bearing Unit Troubleshooting	909
8.	Signal Analyzer Unit Troubleshooting	932
9.	Console Display and Control Panel Unit Troubleshooting	945

TROUBLESHOOTING

1. GENERAL

A. This section is intended for use as a guide to assist in isolating trouble in the TACAN Beacon Test Set. A thorough understanding of the theory of operation is necessary for isolating possible malfunctions. This section contains the troubleshooting sequence charts, troubleshooting flow charts, and test point tabulation data (figures 901 through 911). Schematic, logic, and wiring diagrams are grouped together at the end of this section. The figure number for the schematic, logic, and wiring diagrams is as follows:

Title	Figure No.
TACAN Beacon Test Set Interconnecting Wiring Diagram	912
TACAN Beacon Test Set Rear Panel Schematic Diagram	913
Digital Bearing Unit Interconnecting Wiring Diagram	914
DBU Power Supply Regulator A100 Schematic Diagram	915
Memory Counter A200 Logic Diagram	916
Digital Video Signal Processor A300 Schematic Diagram	917
Reference Counter A400 Logic Diagram	918
Pulse Group Decoder A500 Logic Diagram	919
Digital Bearing Unit Monitor A600 (7124-4305-1) Logic Diagram	920
Digital Bearing Unit Monitor A600 (7124-4305-2) Logic Diagram	921
Signal Analyzer Unit Interconnecting Wiring Diagram	922
SAU Power Supply Regulator A100 Schematic Diagram	923
Limit Detector A200 (7124-1110-1) Schematic Diagram	924
Limit Detector A200 (7124-1110-2) Schematic Diagram	925
Signal Processor A300 Logic Diagram	926
Console Display and Control Panel Unit Interconnecting Wiring Diagram	927

Title	Figure No.
LED Display Logic Diagram	928
Course Select Schematic Diagram	929
Channel Select Logic Diagram	930
Power Cable Assembly (7124-2529) Diagram	931

B. Maintenance data for the integrated circuits (logic diagrams, truth tables, etc.) are given in the Test and Alignment section. Troubleshooting data for the DME is given in the Maintenance/Overhaul Manual for KDM 7000 Digital DME. Maintenance data for the Static Inverter Model PC-15B is given in the instruction manual for this Static Inverter (included as Appendix A and bound at the back of this manual).

2. FAULT INDICATOR ANALYSIS

A. In addition to the fault indicators on the DME, the RANGE FAILURE indicator on the Console Display and Control Panel Unit (Panel Unit) indicates when there is a failure in the DME. If the RANGE FAILURE indicator is illuminated, troubleshoot the DME as indicated in the Maintenance/Overhaul Manual for KDM 7000 Digital DME. If this fails to correct the problem, troubleshoot the Panel Unit RANGE FAILURE indicator circuit.

B. The Panel Unit contains a BEARING FAILURE fault indicator to identify the status of the Digital Bearing Unit. If the BEARING FAILURE indicator is illuminated, observe the light emitting diodes (LED's) on the Digital Bearing Unit Monitor card 600. When the BEARING FAILURE indicator of the Panel Unit is illuminated, one of the LED indicators of card 600 is illuminated. When a card 600 LED is illuminated, troubleshooting should be directed to the applicable card in the Digital Bearing Unit as follows:

LED Indicator Illuminated	Suspected Faulty Card
PWR REG	Power Supply Regulator card 100
VID PCR	Video Signal Processor card 300
PLS DEC	Pulse Group Decoder card 500
REF CTR	Reference Counter card 400
MEM CTR	Memory Counter card 200

C. Three circuit breakers are mounted on the rear panel of the test set. Depending upon the primary power source to which the test set is connected, one or more of these circuit breakers may prevent operation of the test set. Check circuit breakers CB7501, CB7502, and CB7503 as applicable.

3. TROUBLESHOOTING SEQUENCE CHARTS

The troubleshooting sequence charts consists of a logical sequence of sumptoms and possible causes of each section of the major components of the test set. In addition, an overall test set troubleshooting sequence chart is provided to assist in isolating a problem to a major assembly of the test set. The troubleshooting sequence charts are figures 901, 903, 906, and 909.

4. TROUBLESHOOTING FLOW CHARTS

The troubleshooting flow charts are arranged in approximately the same order as the associated sequence chart. Each test contained within a decision block results in either a "yes" or "no" decision. If the test is passed ("yes"), the flow is routed to the next decision block. If the test is failed ("no"), the flow is routed to other decision or "check" blocks to further isolate the cause or failure. The arrangement of both troubleshooting charts and the possible causes presented assumes that the previous steps of the test were passed. The troubleshooting flow charts are figures 902, 904, 907, and 910.

5. WAVEFORM DATA

Waveform data for the Digital Bearing Unit, Signal Analyzer Unit, and Panel Unit is given on figures 905, 908, and 911 respectively.

6. TEST SET TROUBLESHOOTING

The information presented in the test set sequence chart (figure 901) and associated troubleshooting flow chart (figure 902) do not include all possible causes of a test set failure, but are presented as a guide line to be used in locating the approximate major assembly of the test set that has failed. The test setup required for troubleshooting is identified on figure 803. The tests identified in figures 901 and 902 closely parallel the tests procedures given in the Test and Alignment section. If it is suspected that the CHANNEL/MODE selector is malfunctioning, refer to paragraph 2 I of Description and Operation section for information required for troubleshooting.

Test	Symptom	Possible Cause
DME Receiver Sensitivity	Test set fails to lock-on (RANGE NAUTICAL MILES indicator does not indicate 100.0 ± 0.2 nautical miles and BEARING DEGREES indicator does not indicate a 180-degree bearing) on channels 2, 69, or 124.	Faulty DME Faulty TACAN AGC output of Digital Bearing Unit
	Test set fails to lock-on on one channel but does lock-on on other channels.	Faulty DME Faulty CHANNEL/MODE selector
DME Power Output	DME power output is less than 500 watts.	Faulty DME
Faulty Y Mode Operation	Test set fails to lock-on in Y-mode operation (operates in X-mode).	Faulty CHANNEL/MODE selector Faulty Pulse Group Decoder card in Digital Bearing Unit Faulty DME
DME Range Accuracy and Tracking	Improper range indication and range tracking.	Faulty DME Faulty range indicating circuit in Panel Unit
Test Audio Output and Volume	Audio output absent from speaker.	Faulty DME Faulty VOLUME control Faulty speaker
Digital Bearing Unit Bearing Accuracy	Improper bearing information displayed.	Faulty Digital Bearing Unit Faulty bearing display circuit in Panel Unit Faulty DME
Digital Bearing Unit Acquisition Time	Test set fails to lock-on within specified time.	Faulty Digital Bearing Unit

Figure 901. TACAN Beacon Test Set Troubleshooting Sequence Chart (Sheet 1 of 4)

Test	Symptom	Possible Cause
Digital Bearing Unit Tracking Rate (Normal)	Test set tracking rate is abnormal.	Faulty Digital Bearing Unit
Digital Bearing Unit Tracking Rate (15-Hz Only)	Test set tracking rate is abnormal.	Faulty Digital Bearing Unit Faulty BEARING switch circuit in Panel Unit
Digital Bearing Unit Memory	Digital Bearing Unit memory time is improper.	Faulty Digital Bearing Unit
Modulation Check	Test set fails 15-Hz and/or 135-Hz modulation check.	Faulty Digital Bearing Unit Faulty PERCENT switch or PERCENT meter circuit
Fault Indicator Checks	BEARING FAILURE indicator on Panel Unit fails to illuminate when at least 1 LED on Digital Bearing Unit Monitor card is illuminated.	Faulty BEARING FAILURE indicator circuit in Panel unit
	LED indicator(s) on Digital Bearing Unit Monitor card fail to illuminate when failure is simulated.	Faulty Digital Bearing Unit Monitor card
Signal Analyzer Unit Bearing Deviation	Test set fails bearing deviation tests.	Faulty Digital Bearing Unit Faulty Signal Analyzer Unit Faulty COURSE SELECT DEGREES control on Panel Unit Faulty COURSE DEVIATION DEGREES meter circuit
TO/FROM Indicators	TO/FROM indicators on Panel Unit fail to illuminate at proper time.	Faulty Digital Bearing Unit

Figure 901. TACAN Beacon Test Set Troubleshooting Sequence Chart (Sheet 2 of 4)

Test	Symptom	Possible Cause
Antenna Speed	ANT. SPEED ± 1.8 RPM UNDER/OVER indicators on Panel Unit fail to illuminate at proper time (ANTENNA SPEED meter indicates proper speed).	Faulty Signal Analyzer Unit Faulty LED indicator circuits on Panel Unit
	ANTENNA SPEED meter and UNDER/OVER indicators fail to indicate proper antenna speed/condition.	Faulty Digital Bearing Unit
Squitter Rate	SQUITTER RATE ± 5% UNDER/OVER indicators on Panel Unit fail to illuminate at proper time (TACAN).	Faulty Signal Analyzer Unit Faulty Digital Bearing Unit Faulty LED indicator circuits on Panel Unit
	PERCENT meter indication improper for squitter rate test.	Faulty PERCENT switch circuit/PERCENT meter circuit
	SQUITTER RATE ± 5% UNDER indicator on Panel Unit fails to illuminate at proper time (DME).	Faulty Signal Analyzer Unit Faulty SQUITTER switch on Panel Unit
Phase Coherency	PHASE COHER ± 5° UNDER/OVER indicators on Panel Unit fail to illuminate at proper time.	Faulty Signal Analyzer Unit Faulty LED indicator circuits in Panel Unit
	PHASE COHERENCY DEGREES meter indication improper.	Faulty PHASE COHERENCY DEGREES meter circuit
MRG Size	MRG SIZE UNDER/OVER indicators on Panel Unit fail to illuminate at proper time.	Faulty Signal Analyzer Unit Faulty LED indicator circuits in Panel Unit Faulty Digital Bearing Unit

Figure 901. TACAN Beacon Test Set Troubleshooting Sequence Chart (Sheet 3 of 4)

Test	Symptom	Possible Cause
ARG Size	ARG SIZE UNDER/OVER indicators on Panel Unit fail to illuminate at proper time.	Faulty Signal Analyzer Unit Faulty LED indicator circuits in Panel Unit Faulty Digital Bearing Unit
ARG Count	ARG COUNTER UNDER indicator fails to illuminate at proper time.	Faulty Signal Analyzer Unit Faulty LED indicator circuit in Panel Unit
Percent Range Reply	Indications for percent range reply check are improper.	Faulty Signal Analyzer Unit Faulty PERCENT switch/ meter circuit Faulty DME
Oscilloscope Sync Outputs	MRG oscilloscope sync output incorrect.	Faulty Signal Analyzer Unit Faulty SYNC switch Faulty Digital Bearing Unit
	ARG oscilloscope sync output incorrect.	Faulty Signal Analyzer Unit Faulty SYNC switch Faulty Digital Bearing Unit
	Range interrogate oscilloscope sync output incorrect.	Faulty Signal Analyzer Unit Faulty SYNC switch Faulty DME
	Range reply oscilloscope sync output incorrect	Faulty Signal Analyzer Unit Faulty SYNC switch
AGC Output	AGC BUFFERED voltage is not within acceptable limits with simulator output set to -110 dbm.	Faulty Signal Analyzer Unit Faulty Digital Bearing Unit

Figure 901. TACAN Beacon Test Set Troubleshooting Sequence Chart (Sheet 4 of 4)

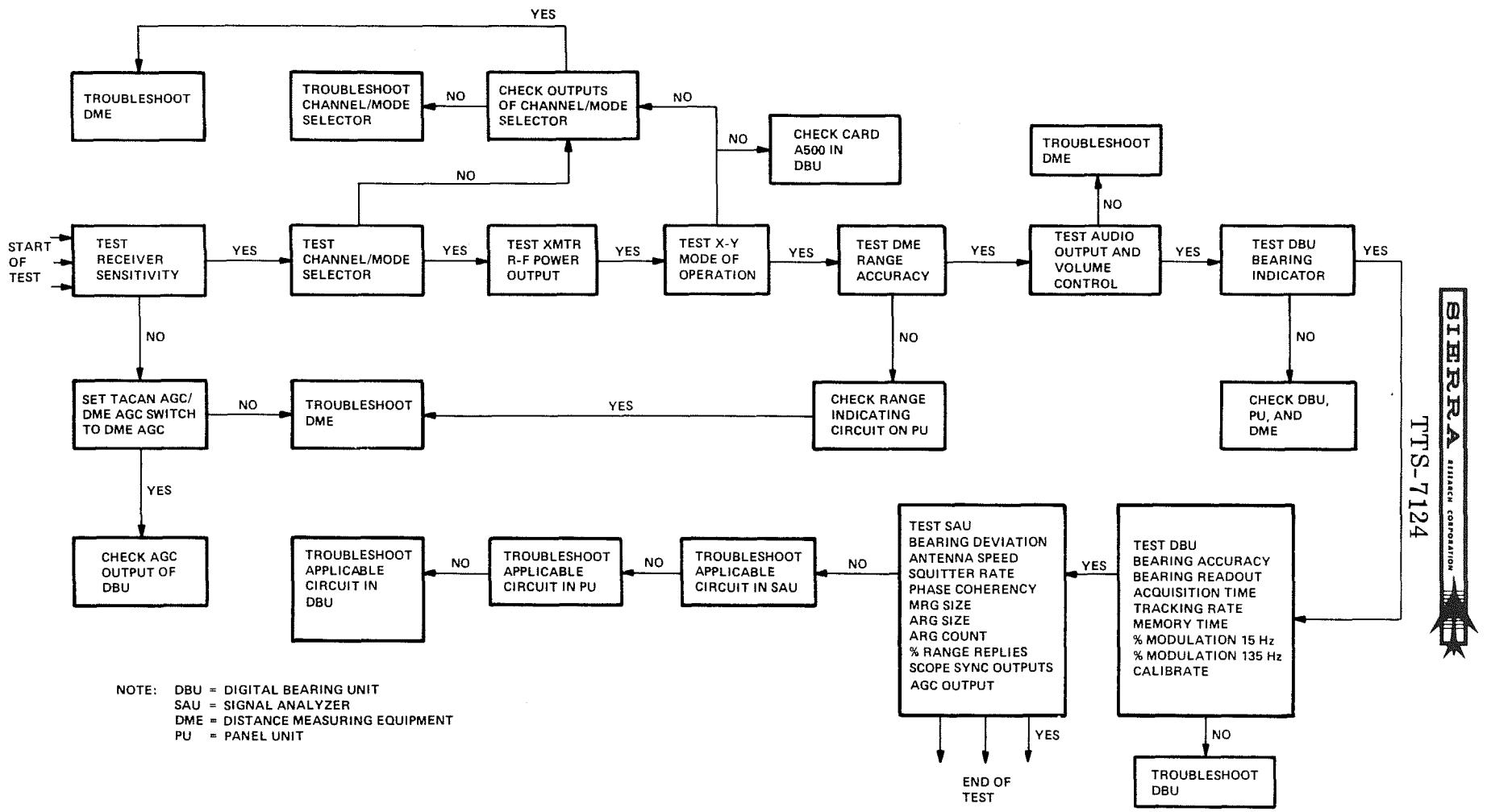


Figure 902. TACAN Beacon Test Set Troubleshooting Flow Diagram

7. DIGITAL BEARING UNIT TROUBLESHOOTING

Examine the type of failures identified as a possible cause which illuminated the BEARING FAILURE LED indicator on the Panel Unit (refer to paragraph 2B). Then refer to the Digital Bearing Unit troubleshooting sequence chart figure 903 to identify the typical failure to an individual circuit or subassembly of the Digital Bearing Unit. When the problem has been isolated to a subassembly (card), refer to the applicable card theory in the Description and Operation section. Figure 904 is the Digital Bearing Unit troubleshooting flow chart. Figure 905 identifies test point data for the cards of the Digital Bearing Unit. The test hookup required to check the Digital Bearing Unit is given on figure 803. Refer to paragraph 1 for a listing of the schematic, logic, and wiring diagrams of the Digital Bearing Unit.

Section	Symptom		Possible Cause
Power Supply (figures 914 and 915)	15V, 400 Hz:	Out of tolerance (±1 Vac)	A-c input to Digital Bearing Unit not at 115 ±11.5 Vac, 400 ±20 Hz.
			T7201 shorted
	:	Missing	T7201 open
	9V, 400 Hz:	Out of tolerance (±1 Vac) Designated 5V on figure 914	T7201 shorted
			CR7201 shorted
			C7201 shorted
	24V, 400 Hz:	Out of tolerance (±2.4 Vac) or missing	T7201
			CR401, C403, U401
	+20Vdc:	Out of tolerance (±2 Vdc) or missing	CR101, CR102, U101, C104
	-20Vdc:	Out of tolerance (±2 Vdc) or missing	CR104, CR105, U102, C105
	+12Vdc:	Out of tolerance (±0.12 Vdc)	R103 not adjusted properly
			U101, Q101, associated resistors
	:	Missing	+20V missing, faulty U101, Q101
	-12Vdc:	Out of tolerance (±0.12 Vdc)	R108 not adjusted properly
			U102, associated resistors
	:	Missing	-20V missing, faulty U102
	+5.7Vdc:	Out of tolerance (±0.3 Vdc) or missing	+12Vdc missing
			R104, VR101, CR103

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart(Sheet 1 of 12)

Section	Symptom		Possible Cause
Power Supply (Cont)	+5Vdc:	Out of tolerance (±0.3 Vdc) or missing	CR7201, C7201, Q7201 +5.7Vdc incorrect
Video Processor (see figures 914 and 917)	LIMITED VIDEO:	Missing at TP306 (check signal at TP305)	U314, U315, or associated components defective U301A or U301B defective R355, R343
Pulse Group Decoder (figures 914 and 919)	PULSE PAIRS:	Missing at TP506	Clock missing at TP504 (defective U522, U523A, U523B) Defective shift register (U505A, U505B, U506, U507, U508, U509) Defective counter (U519A, U519B, U518, U516B) Defective gates (U504C, U513A, U514A, U517D, U517A, U517C, U512A, U520A, U513C, U512C, U504D) X Mode failure - No signal at TP503, check U512D, U501B Y Mode failure - No signal at TP503, check U501D, U502A, U503
	DUMP PULSE:	Missing at TP510	U520D, U517C, U516A, U517B
	PEAK DETECTOR INHIBIT:	Missing at TP509	Same possible causes as for missing PULSE PAIRS

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 2 of 12)

Section	Symptom		Possible Cause
Pulse Group Decoder (Cont)	MRGEV Pulse:	Missing at TP508 (for X- or Y-mode)	Defective counter (U511, U515B) U521A, U520C, U504A
	:	Missing at TP508 (for X-mode only)	U503, U501D, U502A (Check signal at TP501) ZERO ±2° GATE output of reference counter not occurring
	:	Missing at TP508 (for Y-mode only)	U503, U502C - check at TP501
	PGD MONITOR:	Missing at P501-4	Defective shift register (U505A, U505B, U506, U507, U508, U509) Defective clock at TP504 (U522, U523A, U523B)
	MRGCK:	Missing at P501-13	U504A
	ARGCK:	Missing at P501-14	U504B
	ARGEV:	Missing at TP507	Counter U510, U515A, U521B, U514D, U520B ±2° GATE missing U504B
	:	Missing, X-mode only	U501C, U502B - check at TP502
	:	Missing, Y-mode only	U502D, U501A - check at TP502

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart(Sheet 3 of 12)

Section	Symptom	Possible Cause
Pulse Group Decoder (Cont)	MRGP Pulse: Missing at TP508	U514C, U513B
Amplitude Modulation Processor (figures 914 and 917)	15Hz: Missing at TP302 (135 Hz is present) or improper amplitude	15-Hz filter not adjusted properly (R304) Filter U301A or associated components defective
	15S: Missing at TP308 (15 Hz is present)	0 = BEARING DASHES at TP304 is a logical 0 U303
	15 Hz: Missing at TP302 (135 Hz is also missing)	CR304, CR303, U310A, U309C, U310B, U307, U309D, U308B, C315, C316, U309A, C320 (Check signal at TP303.)
	135 Hz: Missing at TP301 (15 Hz is present) or improper amplitude	135-Hz filter not adjusted properly (R310) Filter U301B or associated components defective
	135S: Missing at TP307 (135 Hz is present)	U304 or associated components defective
	FILTER MONITOR: Missing or improper at P301-2 (15 Hz and 135 Hz normal)	R307 or R308
	15S BUFFERED: Missing at P301-12 (15S present at TP308)	U316A, U316B

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart(Sheet 4 of 12)

Section	Symptom		Possible Cause
Amplitude Modulation Processor (Cont)	15 Hz LEVEL:	Missing or at an improper amplitude at TP309 (15 Hz at TP302 normal)	Variable resistor R314 out of adjustment U313A, U313B
	135 Hz LEVEL:	Missing or at an improper amplitude at TP310 (135 Hz at TP301 normal)	Variable resistor R316 U306A, U306B
PULSE PAIRS BUFFER Amplifier (figures 914 and 917)	BUFFERED PULSE PAIRS:	Missing at P301-16	U316C, U316D
4-MHz Oscillator and Divide-By-Circuit (figures 914 and 919)	4 MHz:	Missing or improper at P501-12	U514, U522
	2 MHz:	Missing or improper at P501-11	U523A
Reference Counter (figures 914 and 918)	ZERO ±2° GATE:	Missing or improper at TP408	Reference counter clock not present at TP405 Defective counter (U407, U412, U413, U414, U415) U404A, U410B, U406A, U405A, U405B, U410A, U406B, U404A 4-degree pulse not present at TP407 ANT. SPEED signal incorrect at TP401

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 5 of 12)

Section	Symptom		Possible Cause
Reference Counter (Cont)	Reference Counter Clock:	Missing at TP405	Defective VCO U401 (Check at TP404.) U409A, U409B, U408D, U408A
	4° Wide Pulse:	Missing at TP407	Defective counter (U416, U411A). Check at TP410. U405C, U406D
	ANT. SPEED:	D-c level improper at TP401	U403, U402 (Check at TP402.)
	±2° GATE:	Missing at TP403	U404B
	0.2° CLOCK:	Missing at P401-31 (reference counter operation normal)	Broken trace
	0.2° CLOCK*:	Missing at P401-6 (reference counter operation normal)	U422E, U408C, U422B
	SELF TEST SIGNAL:	Missing or incorrect at TP406	R407, R408
Reference Counter Buffer Storage Register (figures 914 and 918)	Bearing Degrees Information:	Improper indication displayed on Panel Unit BEARING DEGREES LED indicator (ZERO ±2° GATE signal normal)	READ pulse output of memory counter improper. Buffer/Storage Register defective (U418, U420, and U411B) U410D

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart(Sheet 6 of 12)

Section	Symptom		Possible Cause
Comparator Circuit (figures 914 and 918)	EQ PULSE:	Missing or improper at TP409 (reference counter operating properly)	U417A-U417D, U419A-U419D, U421A-U421D
Memory Counter (figures 914 and 916)	READ PULSE:	Missing or improper at TP210	No clock to memory counter at TP209
			Defective memory counter (U216, U217, U218, U219)
			U213A, U223D, U211B, U210D, U207B
			Check signal at TP205
	Memory Counter Clock:	Missing at TP209	U214A, U208A, U209D
		Improper at TP209	Defective clock control circuit (U220B, U220A, U210B, U215B, U205A, U205B, U201A, U201B, U201D, U201C, U203, U202, U207F, U207A, U204A, U204B, U206A, U206B, U209D, U208A, U214C, U214D). Check signals at TP207, TP201, TP202, TP203, and TP206.
	0 = ±20° GATE:	Missing or improper at TP208	U207E, U208C, U215D, U213B, U223C, U212B, U211A, U210A. Check signals at TP204 and TP205.

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 7 of 12)

Section	Symptom	Possible Cause
Automatic Bearing Select Circuit (figure 916)	D10 and D20 digital bearing deviation outputs are not logical 1's (at P201-9 and P201-7 respectively) when the OBS CONTROL on the Panel Unit is set to MAN and the COURSE SELECT DEGREES thumbwheel switches are set between +25 to +90 degrees of the systems simulated heading, or between +205 and +270 degrees of the systems simulated heading.	U222, U223A, U223B U221, U210C, U212A, U214B
	D1A, D2B, D4C, D8D, D10, and D20 digital bearing deviation outputs are not logical 0's (at P201-14, P201-11, P201-10, P201-9, and P201-7 respectively) when the OBS CONTROL on the Panel Unit is set to MAN and the COURSE SELECT DEGREES thumbwheel switches are set between +90 and +165 degrees of the systems simulated heading, or between +270 and +345 degrees of the systems simulated heading.	U222, U221, U215C, U214B, U212A
	D. 2B, D. 4C, and D. 8D digital bearing deviation outputs (at P201-18, P201-20, and P201-16 respectively) do not represent the binary numbers 0 through 4 (D. 2B least significant digit) as the systems simulated heading is changed from 0-degree deviation from the selected course to 0. 8-degree deviation. Each binary number is equal to 0. 2-degree deviation.	U221

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 8 of 12)

Section	Symptom	Possible Cause
Automatic Bearing Select Circuit (Cont)	D1A, D2B, D4C, and D8D digital bearing deviation outputs (at P201-14, P201-11, P201-10, P201-12) do not represent the binary numbers 0 through 9 (D1A least significant digit) as the systems simulated heading is changed from 0-degree deviation from the selected course to 10-degree deviation. Each binary number represents 1 degree deviation with binary 5 equivalent to 0-degree deviation, binary 6 = 1-degree deviation, binary 7 = 2-degrees deviation, binary 0 = 3 degrees deviation, binary 9 = 4-degrees deviation, binary 8 = 5-degrees deviation, binary 1 = 6-degrees, binary 2 = 7-degrees deviation, binary 3 = 8-degrees deviation, and 4 = 9-degrees deviation.	U222
	With OBS control on Panel Unit in AUTO position, D10 and D20 digital deviation outputs (at P201-9 and P201-7) are not a logical 1 and not a logical 0 respectively when the systems simulated heading is ±5 degrees of 0 degrees. These signals should both be logical 0's if the heading is between 345.2 and 355.0 degrees, a logical 0 and logical 1 respectively if the heading is between 5.2 and 15.0 degrees, and both logical 1's if the heading is between 15.2 and 25 degrees.	U222, U223A, U223B

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 9 of 12)

Section	Symptom		Possible Cause
Automatic Bearing Select Circuit (Cont)	1 = TO Signal (at P201-22)	: Is not a logical 0 when OBS CONTROL on Panel Unit is in AUTO position.	U208B, U207C
		: Is not a logical 1 when OBS CONTROL on Panel Unit is in MAN position and the systems simulated heading is $0^{+90.0}_{-89.8}$ degrees of the selected heading as determined by the COURSE SELECT DEGREES thumbwheel switches on the Panel Unit.	
		: Is not a logical 0 when OBS CONTROL on Panel Unit is in MAN position and the systems simulated heading is $180^{+90.0}_{-89.8}$ degrees of the selected heading as determined by the COURSE SELECT DEGREES thumbwheel switches on Panel Unit.	U208B, U207C

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 10 of 12)

Section	Symptom	Possible Cause
Bearing Dashes Control Circuit (figures 914 and 917)	0=BEARING: DASHES (TP304): Does not change to a logical 0 when a channel change is made.	U308A, Q303
	: Does not change to a logical 1 when system is operated with beacon simulator.	U305A, U308A, Q302, Q303
Monitor Circuit (figures 914 and 920 or 921)	PWR REG LED: Fails to illuminate if +12, -12, or +5 Vdc fails or is out of tolerance.	U605, U609A, U609B, CR609, CR610 or associated components (Q602 on 7124-4305-2 card only)
	VID PCR LED: Fails to illuminate if LIMITED VIDEO is present however FILTER MONITOR signal is improper.	U608A, U608B, U604 or associated components. R619, C611
	: Fails to illuminate LIMITED VIDEO is not present however FILTER MONITOR signal is normal.	U607A, U608A, U608B, U604
	PLS DEC LED: Fails to illuminate if LIMITED VIDEO is present however PGD MONITOR signal is improper.	U607A, U607B, U603 or associated components.
	REF CTR LED: Fails to illuminate if EQ pulse fails to occur.	U606A, U601 or associated components

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 11 of 12)

Section	Symptom	Possible Cause
Monitor Circuit (Cont)	MEM CTR LED : Fails to illuminate if READ pulse fails to occur.	U606B, U602 or associated components
	DIGITAL BEARING FAILURE : (at P601-5) Fails to become a logical 0 if PWR REG LED is illuminated.	Q601, CR607, or associated components
	: Fails to become a logical 0 if VID PCR LED is illuminated.	Q601, CR605, or associated components
	: Fails to become a logical 0 if PLS DEC LED is illuminated.	Q601, CR604 or associated components
	: Fails to become a logical 0 if REF CTR LED is illuminated.	Q601, CR602 or associated components
	: Fails to become a logical 0 if MEM CTR LED is illuminated.	Q601, CR601 or associated components
Video Processor (figures 914 and 917)	DIGITAL TACAN AGC signal improper	U311B, U311A, CR306, or associated components.

Figure 903. Digital Bearing Unit Troubleshooting Sequence Chart (Sheet 12 of 12)

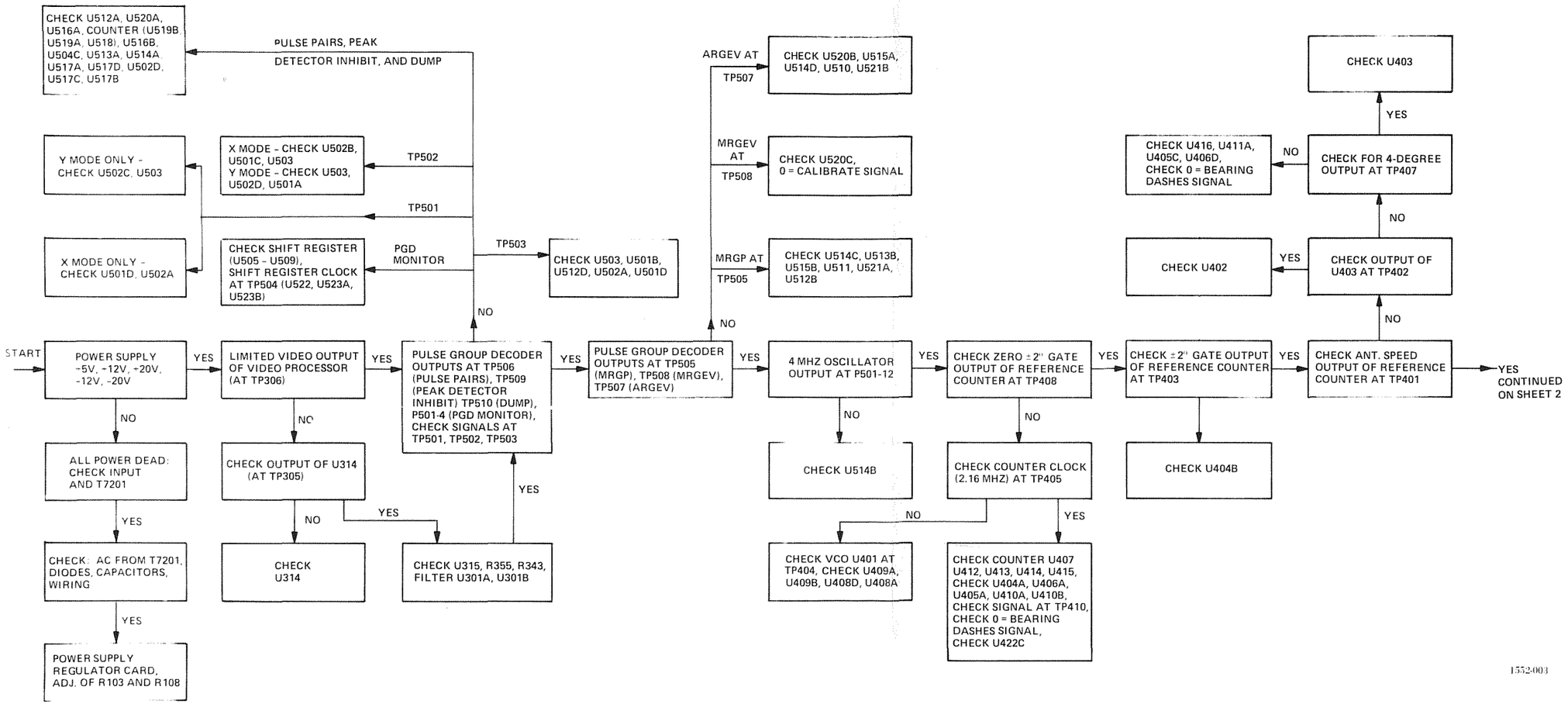


Figure 904. Digital Bearing Unit Troubleshooting Flow Chart (Sheet 1 of 3)

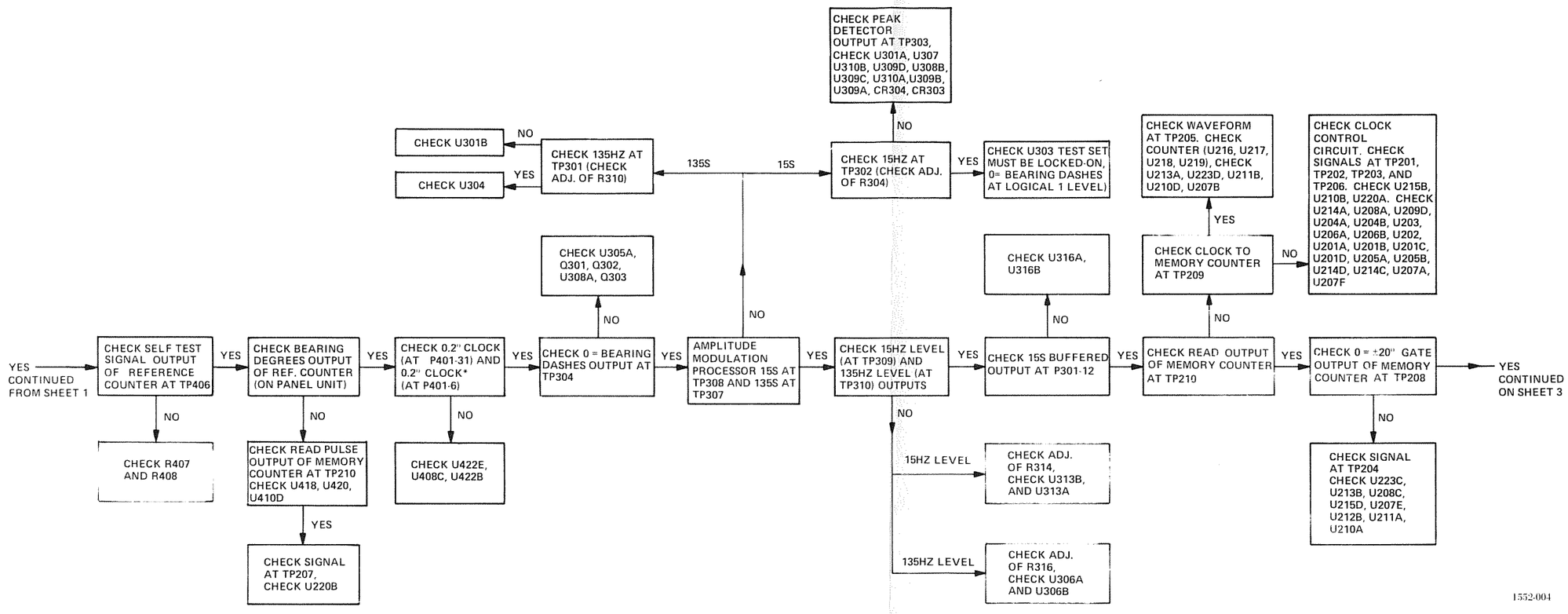


Figure 904. Digital Bearing Unit Troubleshooting Flow Chart (Sheet 2 of 3)

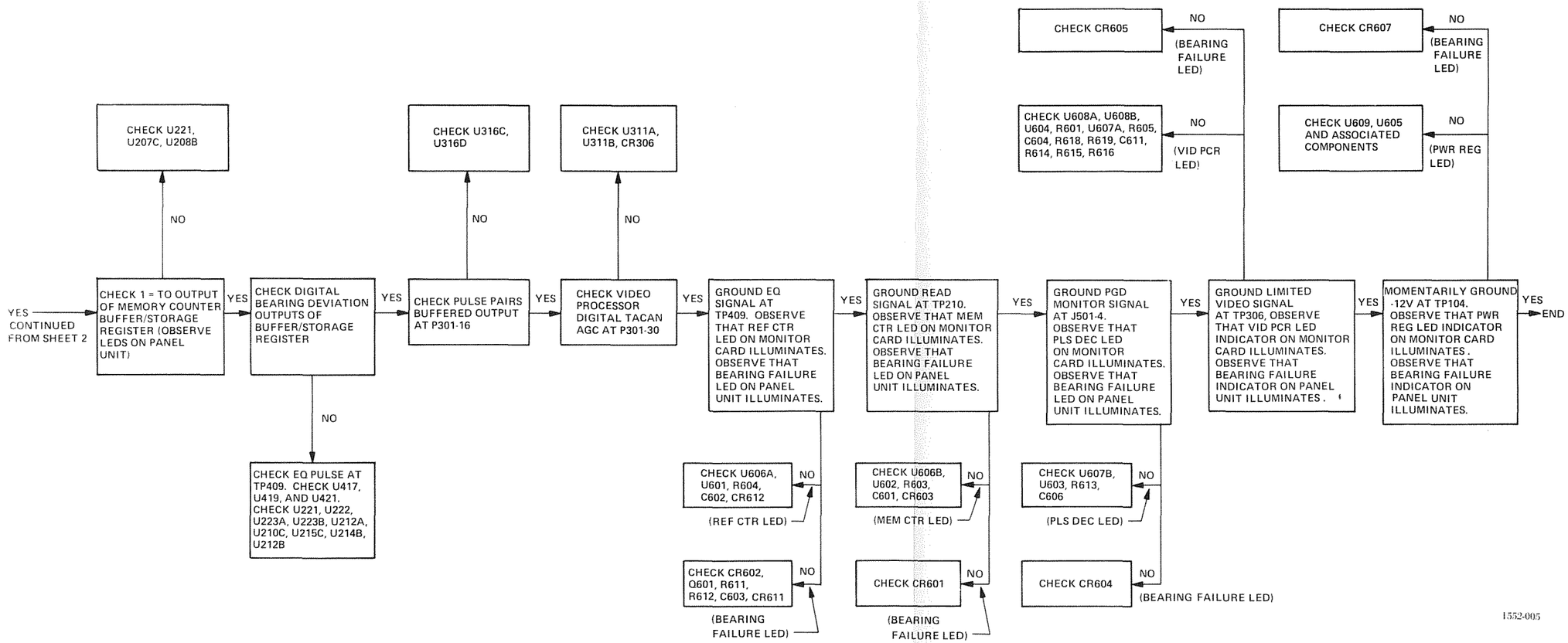


Figure 904. Digital Bearing Unit Troubleshooting Flow Chart (Sheet 3 of 3)

TP101	+19.5 VDC 0.6V P-P RIPPLE	TP104	-12.00 VDC RIPPLE LESS THAN 2MV P-P
TP102	+5.5 VDC	TP105	-19.5 VDC 0.6V P-P RIPPLE
TP103	+12.00 VDC RIPPLE LESS THAN 2MV P-P		

NOTE

UNLESS OTHERWISE INDICATED, THE FOLLOWING DTS-101A SIMULATOR CONDITIONS ARE APPLICABLE FOR ALL REMAINING TROUBLESHOOTING DATA IN THIS FIGURE.

1. SQUITTER RATE = 2700 PULSE PAIRS PER SECOND
2. BEARING = 000.0 DEGREES
3. CHANNEL 1
4. 15 HZ MODULATION = 0.2
5. 135 HZ MODULATION = 0.2
6. 15 HZ PHASE = 0
7. PULSE SPACING = 12 μSEC
8. R-F LEVEL = -50 DBM
9. X MODE
10. ID TONE
11. SCOPE SYNC ON MRB

UNLESS OTHERWISE INDICATED, THE FOLLOWING TEST SET CONDITIONS ARE APPLICABLE FOR ALL REMAINING TROUBLESHOOTING DATA IN THIS FIGURE.

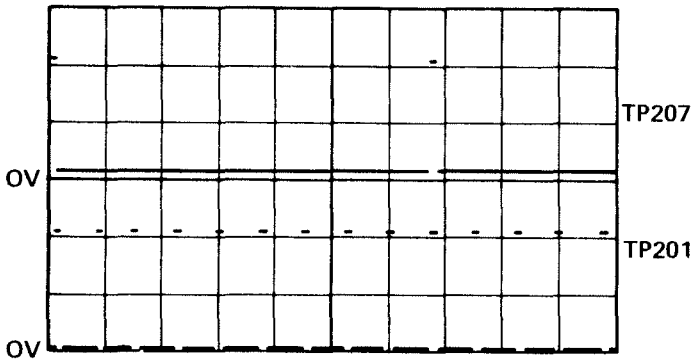
1. CHANNEL/MODE= 001X
2. TRANSMIT PUSHBUTTON/INDICATOR = EXTINGUISHED (STANDBY MODE)
3. SELF TEST PUSHBUTTON/INDICATOR = EXTINGUISHED

UNLESS OTHERWISE INDICATED, THE FOLLOWING PANEL UNIT CONDITIONS ARE APPLICABLE.

1. BEARING = NORMAL
2. SQUITTER = TACAN
3. OPERATE MODE
4. OBS CONTROL = MANUAL
5. COURSE SELECT DEGREES = 000

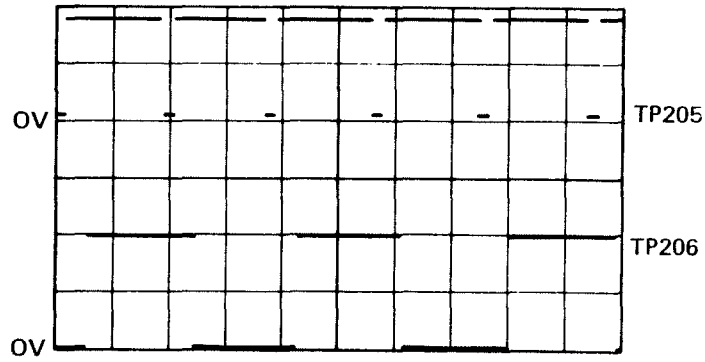
SCOPE DEFLECTION INPUTS ARE D-C COUPLED.

Figure 905. Digital Bearing Unit Test Point Data (Sheet 1 of 7)



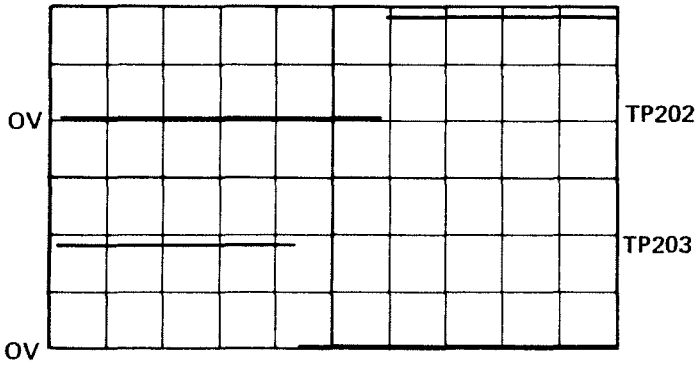
TP201
TP207
(TP201 APPEARS AS TOP TRACE IN 15 HZ - ONLY MODE)

10MS/CM
2V/CM



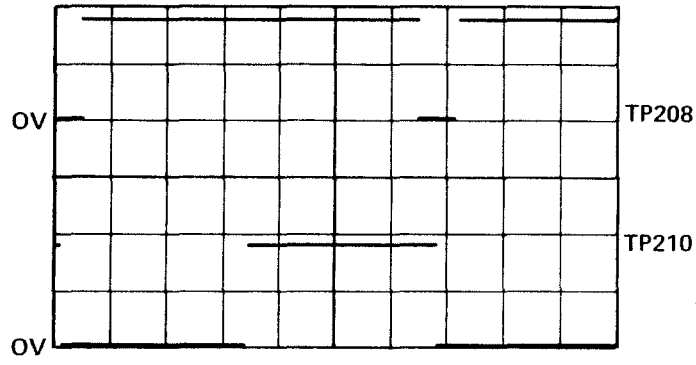
TP205
TP206

2MS/CM
2V/CM



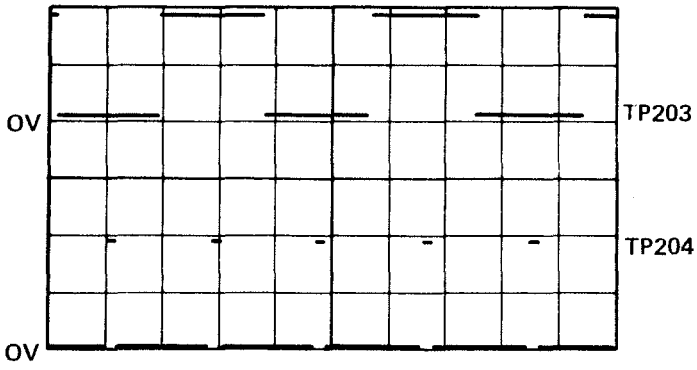
TP202
TP203

50 μS/CM
2V/CM



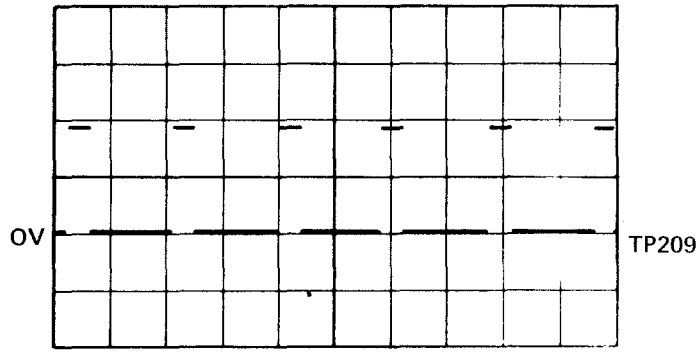
TP208 (0 = ±20° GATE)
TP210 (READ)

10MS/CM
2V/CM



TP203
TP204

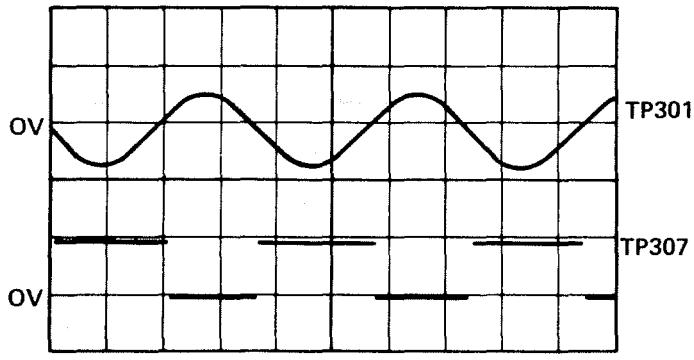
2MS/CM
2V/CM



TP209

20 μS/CM
2V/CM

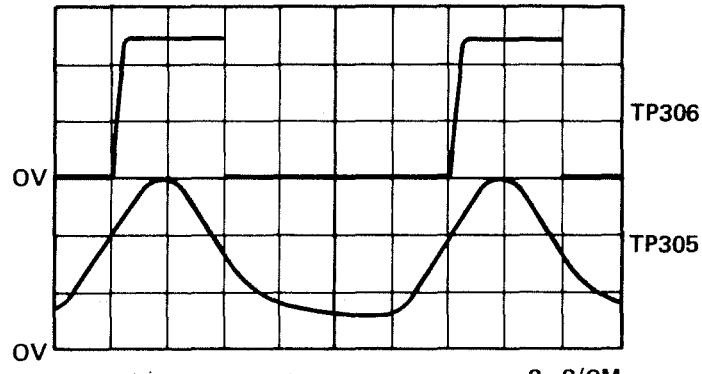
Figure 905. Digital Bearing Unit Test Point Data (Sheet 2 of 7)



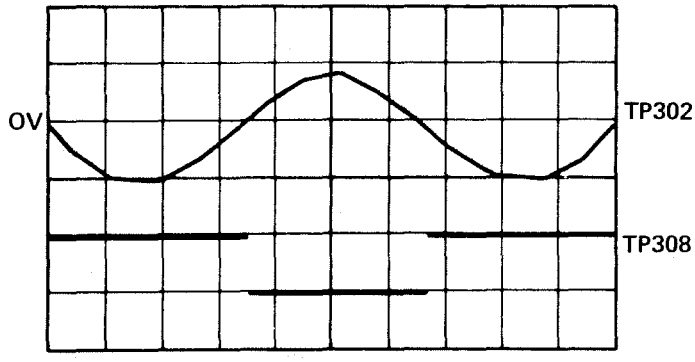
TP301 (135 HZ FILTER) 2MS/CM
TP307 (135 S) 5V/CM

TP304 (0 = BEARING DASHES) –

+0.2V WITH BEACON SIMULATOR TURNED OFF. LOGICAL 1 WITH SIMULATOR ON AND TEST SET LOCKED ON.



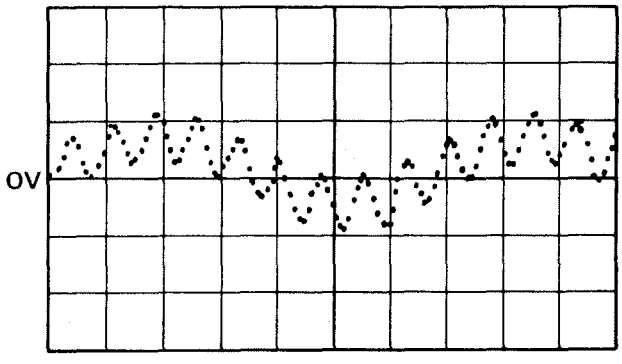
TP305 (AMPL VIDEO) 2 μS/CM
-5V TO GND 2V/CM
TP306 (LIMITED VIDEO)
BASE LINE AT GND



TP302 (15 HZ FILTER) 10MS/CM
TP308 (15S) 5V/CM

TP309 (15 HZ LEVEL) -

+2.5 ± 0.5V DC FOR 10% MODULATION
+5.0 ± 0.5V DC FOR 20% MODULATION
+7.5 ± 0.5V DC FOR 30% MODULATION

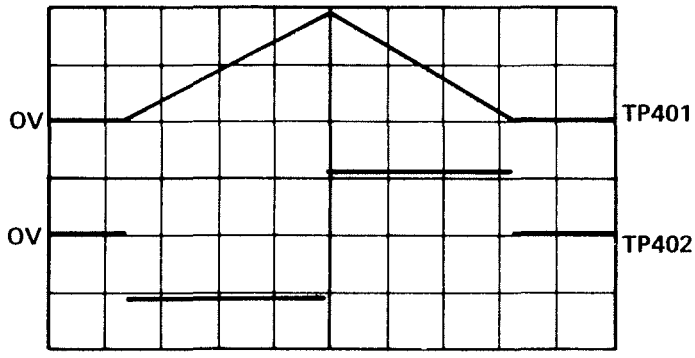


TP303 10MS/CM
2V/CM

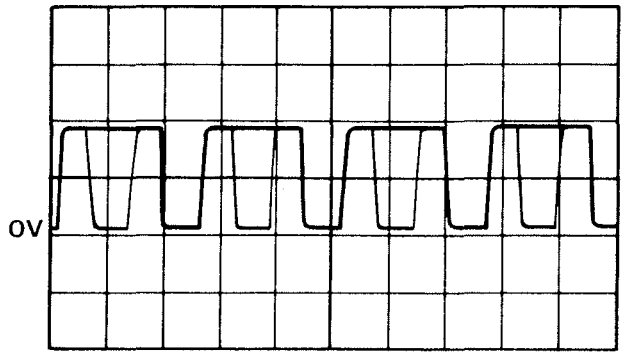
TP310 (135 HZ LEVEL) -

+2.5 ± 0.5V DC FOR 10% MODULATION
+5.0 ± 0.5V DC FOR 20% MODULATION
+7.5 ± 0.5V DC FOR 30% MODULATION

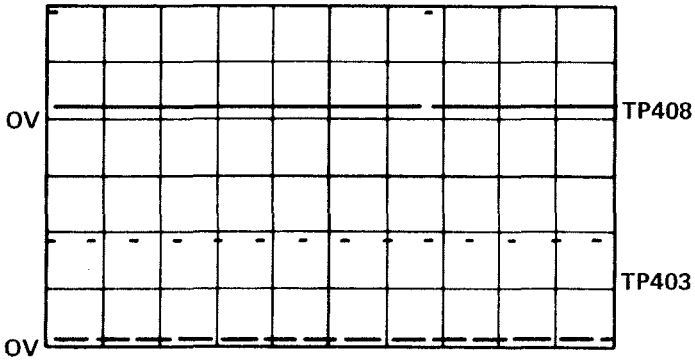
Figure 905. Digital Bearing Unit Test Point Data (Sheet 3 of 7)



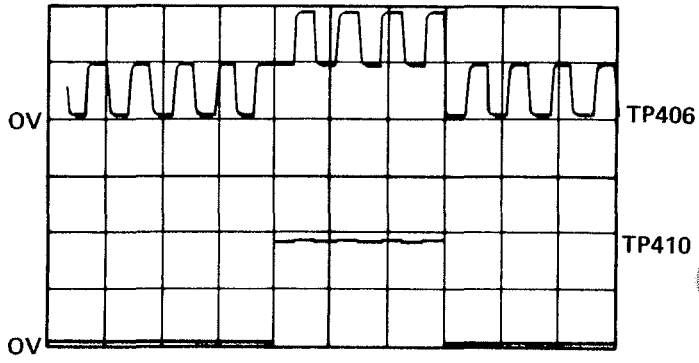
TP401 (ANT. SPEED) 2V/CM
TP402 10V/CM
.1 MS/CM



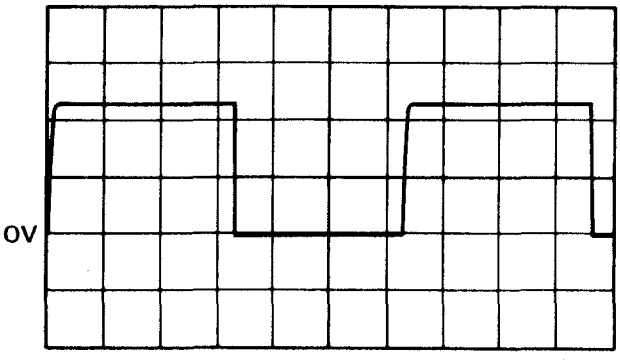
TP405 .2 μS/CM
SYNC – INT + 2V/CM



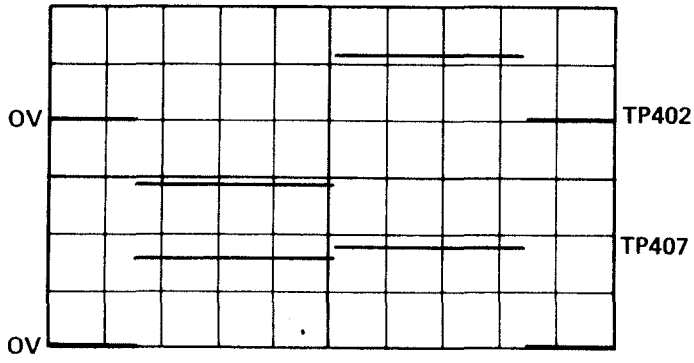
TP403 (±2° GATE) 10MS/CM
TP408 (ZERO ±2° GATE) 2V/CM



TP406 (SELF TEST SIGNAL) 10MS/CM
TP410 (200) 2V/CM

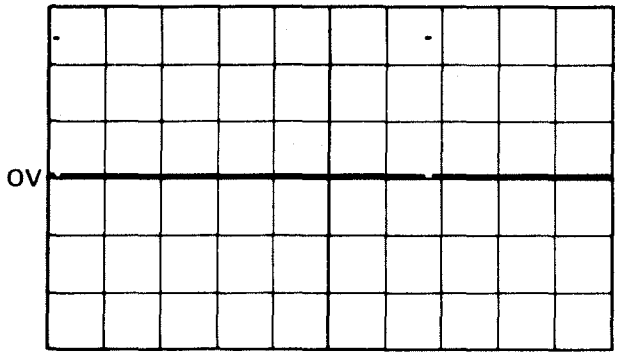


TP404 1 μS/CM
SYNC – INT + 2V/CM

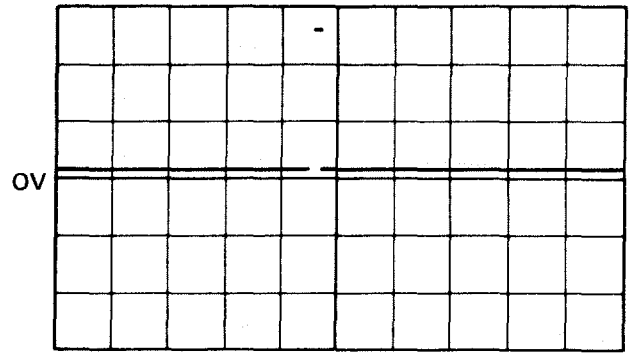


TP402 10V/CM
TP407 2V/CM
.1 MS/CM

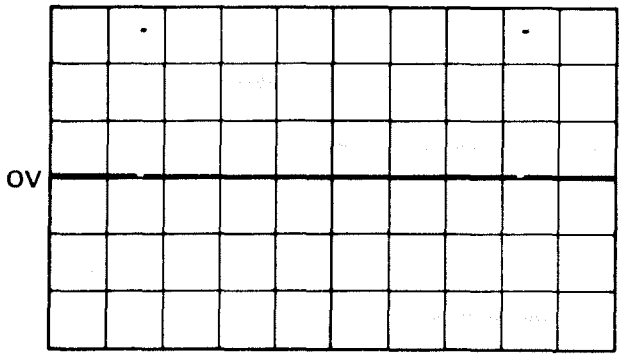
Figure 905. Digital Bearing Unit Test Point Data (Sheet 4 of 7)



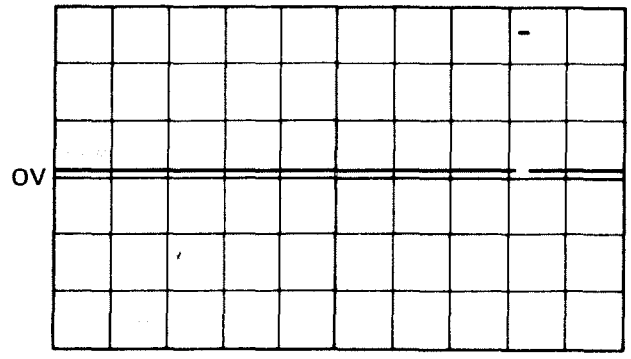
TP409 (EQ) 10MS/CM
PANEL UNIT COURSE SELECT - 000 2V/CM



TP409 (EQ) 50μS/CM
PANEL UNIT COURSE SELECT - 000 2V/CM

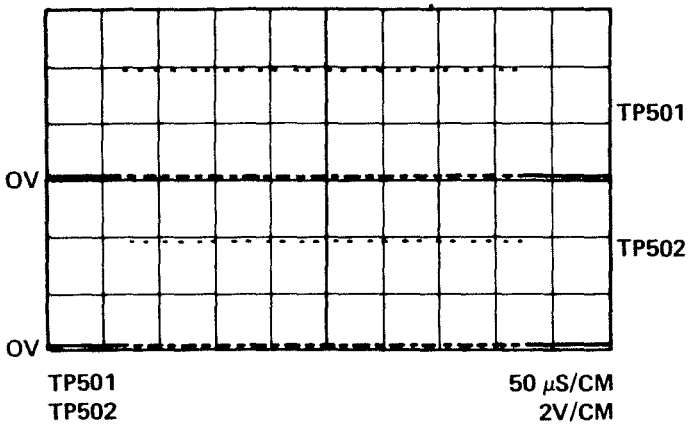


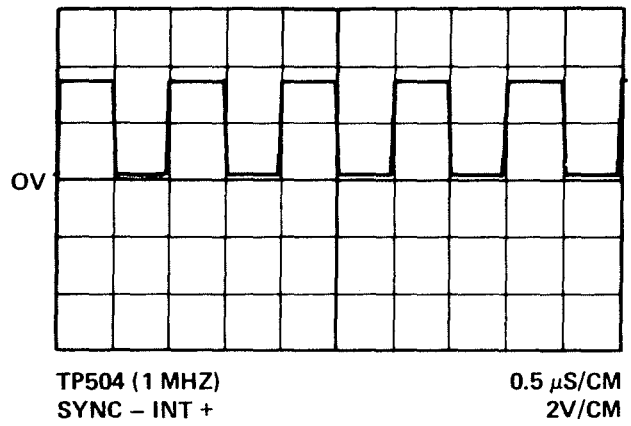
TP409 (EQ) 10MS/CM
PANEL UNIT COURSE SELECT - 090 2V/CM



TP409 (EQ) 50μS/CM
PANEL UNIT COURSE SELECT - 001 2V/CM

Figure 905. Digital Bearing Unit Test Point Data (Sheet 5 of 7)





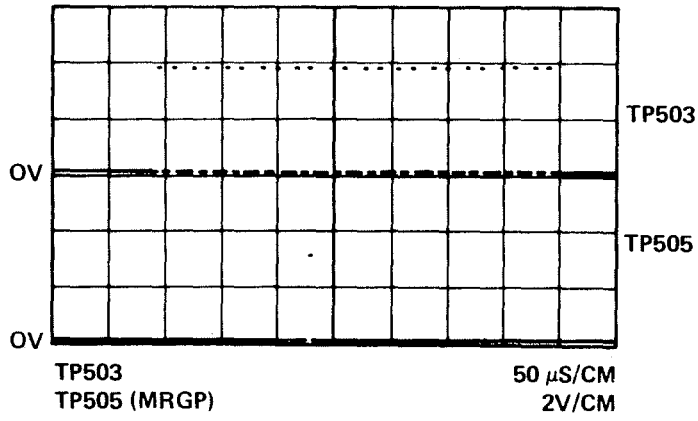
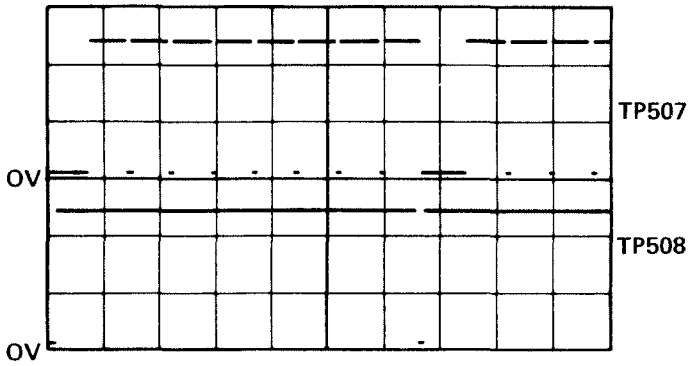
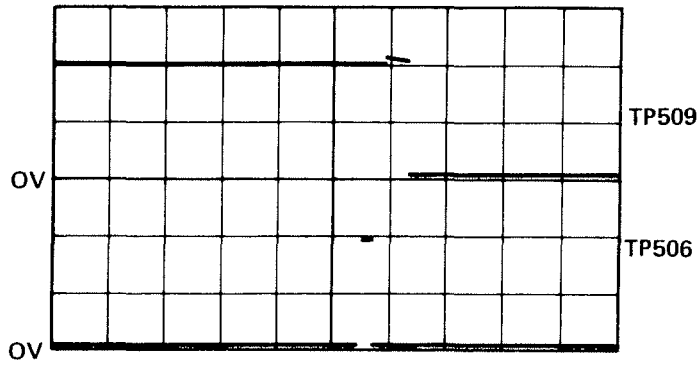


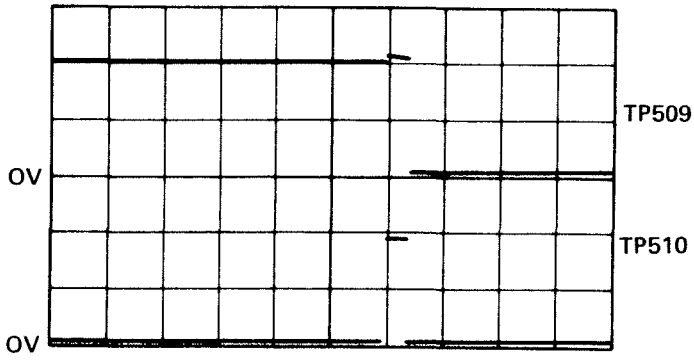
Figure 905. Digital Bearing Unit Test Point Data (Sheet 6 of 7)



TP507 (ARGEV) 10MS/CM
TP508 (MRGEV) 2V/CM



TP509 (PEAK DETECTOR INHIBIT) 5 μS/CM
TP506 (PULSE PAIRS) 2V/CM
SIMULATOR MRB AND ARB DISABLED
SYNC INT + ON TP509



TP509 (PEAK DETECTOR INHIBIT) 5 μS/CM
TP510 (DUMP) 2V/CM
SIMULATOR MRB AND ARB DISABLED
SYNC INT + ON TP509

Figure 905. Digital Bearing Unit Test Point Data (Sheet 7 of 7)

8. SIGNAL ANALYZER UNIT TROUBLESHOOTING

Refer to the Signal Analyzer Unit troubleshooting sequence chart figure 906 to identify the typical failure to an individual circuit or subassembly. Since the Signal Analyzer Unit consists of a number of independent circuits (except for the power supply common to all circuits) and since any problem can easily be isolated to one of these circuits, it may not be necessary to perform all the steps of the troubleshooting sequence chart figure 906 but rather only the section (function) pertinent to the fault suspected. When the problem has been isolated to a subassembly (or section), refer to the applicable theory given in the Description and Operation section. Figure 907 is the Signal Analyzer Unit troubleshooting flow chart. Figure 908 identifies test point data for the cards of the Signal Analyzer Unit. The test hookup required to check the Signal Analyzer Unit is given on figure 803. Refer to paragraph 1 for a listing of the schematic, logic, and wiring diagrams of the Signal Analyzer Unit.

Section	Symptom		Possible Cause
Power Supply (figures 922 and 923)	15 V, 400 Hz:	Out of tolerance (17.7 ±2.0 Vac rms) - Measured to center tap of T7301	A-c input to Signal Analyzer Unit not at 115 ±11.5 Vac, 400 ±20 Hz. T7301 shorted
	:	Missing	T301 open CR101, CR102, CR104, or CR105 shorted
	5V, 400 Hz:	Out of tolerance (9.1 ±1.0 Vc rms)	T7301 shorted CR7301 shorted C7301 shorted
	+20 V dc:	Out of tolerance (23.5 ±4.0 V dc) at TP101	CR101, CR102, U101, C104
	-20 V dc:	Out of tolerance (-23.5 ±4.0 V dc) at TP105	CR104, CR105, U102
	+15 V dc:	Out of tolerance (15 ±0.01 V dc) at TP103	R103 not adjust properly U101, Q101, associated resistors
	:	Missing	+20 V missing, faulty U101, Q101, C104
	-15 V dc:	Out of tolerance (-15 ±0.01 V dc) at TP104	R108 not adjust properly U102, associated resistors
	:	Missing	-20 V missing, faulty U102, C104
	+5.7 V dc:	Out of tolerance (5.7 ±0.3 V dc) at TP102	+15 V dc missing R104, VR101, CR103
	+5 V dc:	Out of tolerance (5 ±0.3 V dc) or missing	CR7301, C7301, Q7301

Figure 906. Signal Analyzer Unit Troubleshooting Sequence Chart (Sheet 1 of 5)

Section	Symptom	Possible Cause
Antenna Speed Circuit (figures 922 and 924 or 925)	ANT. SPEED ±1.8 RPM OVER indicator on Panel Unit fails to illuminate when simulated antenna speed exceeds 902 rpm.	Q201, U207A or associated resistors
	ANT. SPEED ±1.8 RPM UNDER indicator on Panel Unit fails to illuminate when simulated antenna speed is below 898 rpm.	Q206, U207B or associated resistors
Squitter Rate Circuit (figures 922 and 924 or 925)	SQUITTER RATE ±5% OVER indicator on Panel Unit fails to illuminate when squitter rate exceeds 2900 pulse pairs per second.	R201 not properly adjusted Q203, U203A, U209B, Q214, Q215, U214D, U213A, U213B, U214B, U214A or associated resistors U312B, U312C (figure 926)
	SQUITTER RATE ±5% UNDER indicator on Panel Unit fails to illuminate when squitter rate drops below 2500 pulse pairs per second (TACAN mode). (Squitter rate over function operates properly.)	R201 not properly adjusted Q208, U203B, Q209 or associated resistors
	SQUITTER RATE ±5% UNDER indicator on Panel Unit fails to illuminate when squitter rate drops below 600 pulse pairs per second (DME mode). (Squitter rate over function operates properly.)	R201 not properly adjusted Q209, Q208, U203B, or associated resistors.

Figure 906. Signal Analyzer Unit Troubleshooting Sequence Chart (Sheet 2 of 5)

Section	Symptom	Possible Cause
Squitter Rate Circuit (Cont)	Squitter rate analog voltage to recorder incorrect (at TP201).	R201 not properly adjusted U209B, Q214, Q215, U214A, U213A, U213B, U214D, U214B U312B, U312C (figure 926)
MRG Size Circuit (figures 922, 924 or 925, 926)	MRG SIZE OVER indicator on Panel Unit fails to illuminate when MRG is oversize.	Q211, U210A, U215, U214C, U216 U311D, U310D, U315B, U315A, U316A, U316B, U316F, U314C
	MRG SIZE UNDER indicator on Panel Unit fails to illuminate when MRG is undersize. (MRG size over function operates properly.)	Q204, U210B, U215, U214C
ARG Size Circuit (figures 922, 924 or 925, 926)	ARG SIZE OVER indicator on Panel Unit fails to illuminate when ARG is oversize. (MRG size over and under function operates properly.)	Q212, U211A, U217, U218 U311C, U310C, U314B
	ARG SIZE UNDER indicator on Panel Unit fails to illuminate when ARG is undersize. (MRG size over and under function operates properly.) ARG SIZE OVER function operates properly.	Q205, U211B, U217
Phase Coherency Check Circuit (figures 922, 924 or 925, 926)	PHASE COHER ±5° OVER indicator on the Panel Unit fails to illuminate when the phase coherency is six degrees over.	Q207, U208A R308 and R305 not properly adjusted U308B, U308A, U302, U303, U305, U306, U311F, U312A, U307A

Figure 906. Signal Analyzer Unit Troubleshooting Sequence Chart (Sheet 3 of 5)

Section	Symptom	Possible Cause
Phase Coherency Check Circuit (Cont)		U307B, U312D, U312B, U312C, U314D, U301, U304
	PHASE COHER ±5° UNDER indicator on the Panel Unit fails to illuminate when the phase coherency is six degrees under. (Phase coherency over function operates properly.)	Q202, U208B
ARG Count Under Circuit (figures 922, 924 or 925)	ARG COUNT UNDER indicator on the Panel Unit fails to illuminate when the ARG count is less than eight.	Q210, U204B, U209A, Q213, Q216
Bearing Deviation Circuit (figures 922, 926)	BEARING DEVIATION analog voltage to recorder at TP308 is incorrect.	Variable resistors R307 or R306 not properly adjusted.
		U313B, Q304, Q303, U313A, U301F, U301A, U301B, U317E, U317F, U317C, U317D, U310B, U311A, U317A, U311B, U310A, U317B
Percent Range Reply Circuit (figures 922, 926)	Percent range reply analog voltage to recorder is incorrect.	Variable resistor R309 not properly adjusted.
		U309A, Q301, Q302
AGC Buffer Circuit (figures 922, 926)	AGC BUFFERED analog voltage to recorder is incorrect.	Variable resistor R310 not properly adjusted
		U309B
MRG Scope Sync Circuit (figures 922, 926)	MRG SCOPE SYNC signal is incorrect.	U316F, U316E

Figure 906. Signal Analyzer Unit Troubleshooting Sequence Chart (Sheet 4 of 5)

Section	Symptom	Possible Cause
ARG Scope Sync Circuit (figures 922, 926)	ARG SCOPE SYNC signal is incorrect.	U315A, U316A, U316B, U316F
Range Interrogate Scope Sync Circuit (figures 922, 926)	RANGE INTERROGATE SCOPE SYNC signal fails to appear.	U316D
Range Reply Scope Sync Circuit (figures 922, 926)	RANGE REPLY SCOPE SYNC signal fails to appear.	U316C

Figure 906. Signal Analyzer Unit Troubleshooting Sequence Chart (Sheet 5 of 5)

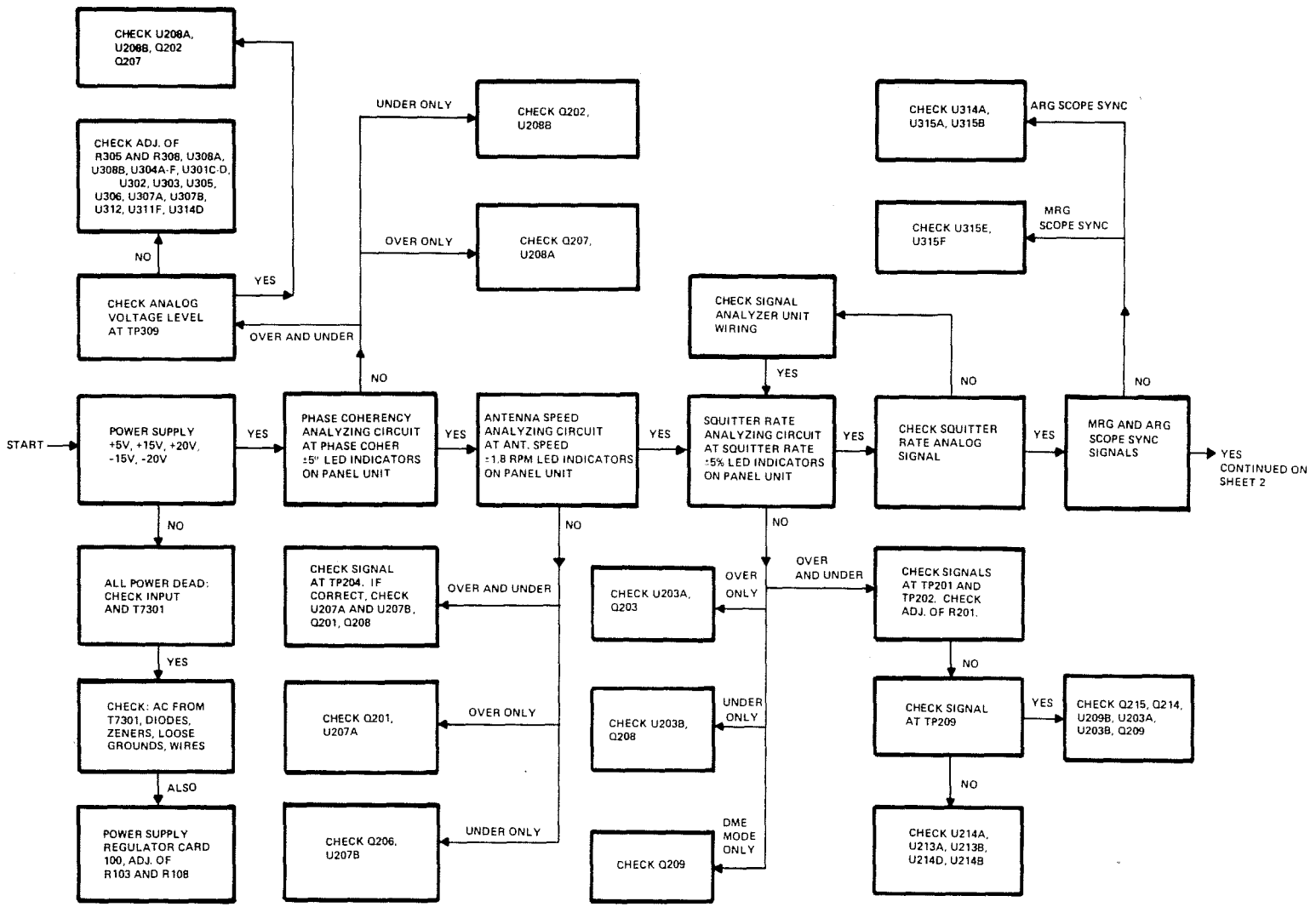


Figure 907. Signal Analyzer Unit Troubleshooting Flow Chart (Sheet 1 of 2)

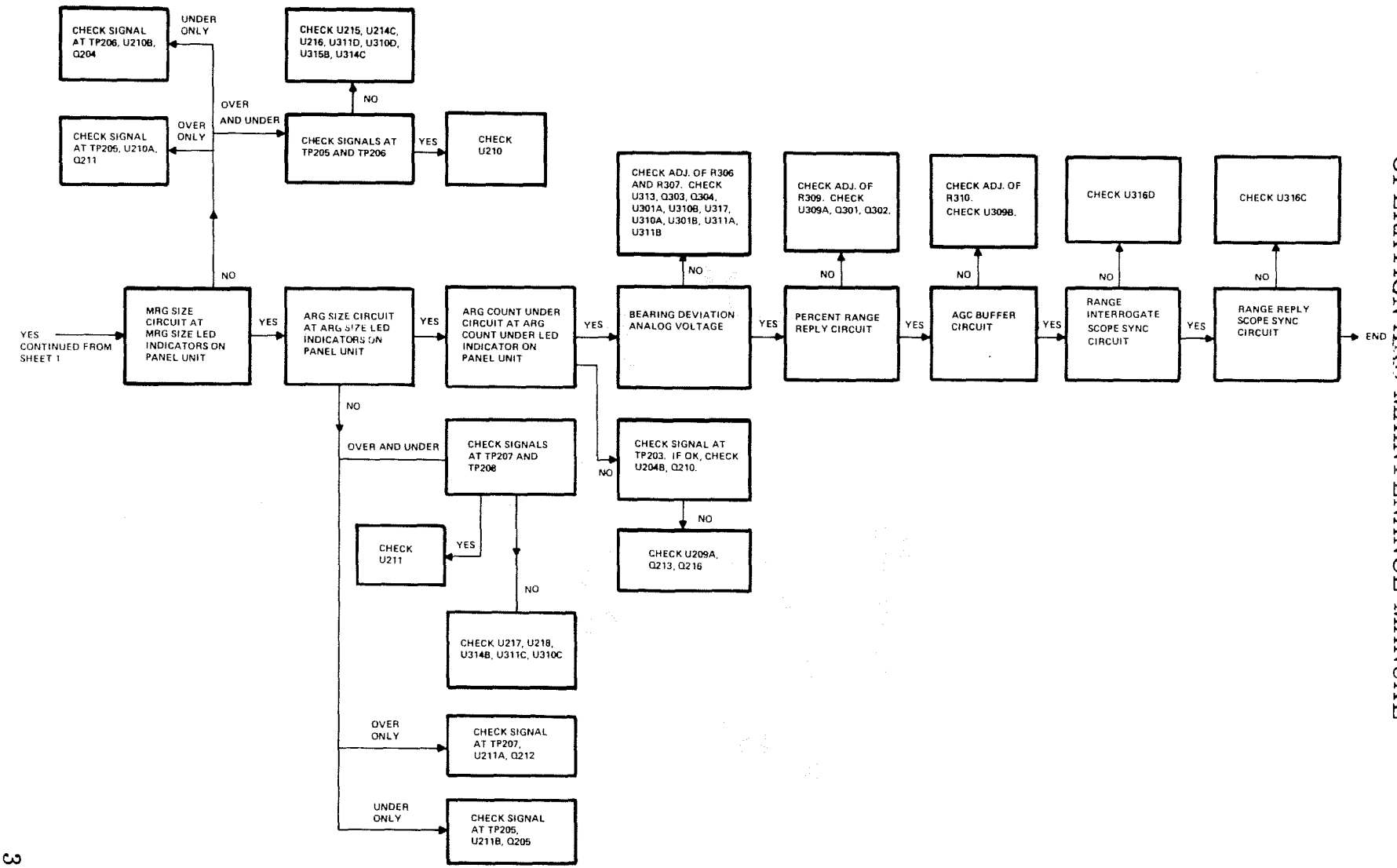


Figure 907. Signal Analyzer Unit Troubleshooting Flow Chart (Sheet 2 of 2)

TP101	+22.5 ± 3.0 VDC 0.6V P-P RIPPLE	TP104	-15.00 RIPPLE LESS THAN 2MV P-P
TP102	+5.7 ± 0.3 VDC	TP105	-22.5V ± 3.0 VDC 0.6V P-P RIPPLE
TP103	+15.00 VDC RIPPLE LESS THAN 2MV P-P		

NOTE

UNLESS OTHERWISE INDICATED, THE FOLLOWING DTS-101A SIMULATOR CONDITIONS ARE APPLICABLE FOR ALL REMAINING TROUBLESHOOTING DATA IN THIS FIGURE.

1. SQUITTER RATE = 2700 PULSE PAIRS PER SECOND
2. BEARING = 000.0 DEGREES
3. CHANNEL 1
4. 15 HZ MODULATION = 0.2
5. 135 HZ MODULATION = 0.2
6. 15 HZ PHASE = 0
7. PULSE SPACING = 12 μSEC
8. R-F LEVEL = -50 DBM
9. X-MODE
10. NORMAL
11. 1-8 ABOVE ARE IDENTICAL TO PRESET

UNLESS OTHERWISE INDICATED, THE FOLLOWING TEST SET CONDITIONS ARE APPLICABLE FOR ALL REMAINING TROUBLESHOOTING DATA IN THIS FIGURE.

1. CHANNEL/MODE= 001X
2. TRANSMIT PUSHBUTTON/INDICATOR = EXTINGUISHED (STANDBY MODE)
3. SELF TEST PUSHBUTTON/INDICATOR = EXTINGUISHED

UNLESS OTHERWISE INDICATED, THE FOLLOWING PANEL UNIT CONDITIONS ARE APPLICABLE.

1. BEARING = NORMAL
2. SQUITTER = TACAN
3. OPERATE/CALIBRATE = OPERATE
4. OBS CONTROL = MANUAL
5. COURSE SELECT DEGREES = 000

SCOPE DEFLECTION INPUTS ARE D-C COUPLED.

Figure 908. Signal Analyzer Unit Test Point Data (Sheet 1 of 5)

TP201 –

SQUITTER RATE 2700 – +10.0 ± 0.2 VDC
SQUITTER RATE 2900 – +10.7 ± 0.2 VDC
SQUITTER RATE 2500 – + 9.4 ± 0.2 VDC

TP202 - (1)

SQUITTER SWITCH TO TACAN - +3.8V, +9.5V
SQUITTER SWITCH TO DME - +1.04V, +2.6V

TP203 –

ARG NOMINAL – +4.7V ± 0.2V
ARG COUNT UNDER – +4.2V ± 0.2V

TP204 - (1)

ANTENNA SPEED NOMINAL - 0.0V ± 0.5VDC, 0.0V ± 1.25VDC
ANTENNA SPEED HIGH - +0.8V ± 0.1VDC, +2.0 ± 0.25VDC
ANTENNA SPEED UNDER - -0.8 ± 0.1VDC, -2.0 ± 0.25VDC

NOTES

TEST POINT DATA FOR TP205 THROUGH TP209 IS AFFECTED BY VALUE OF +5V OUTPUT. VALUES GIVEN FOR THESE TEST POINTS ARE TYPICAL AND LIMITS ESTABLISHED MAY BE EXCEEDED IN SOME INSTANCES WITHOUT INDICATING FAULTY OPERATION.

(1) FIRST VOLTAGE IS FOR 7124-1110-1 CARD
SECOND VOLTAGE IS FOR 7124-1110-2 CARD

TP205 –

MRG NOMINAL – +0.5 ± 0.5VDC
MRG OVER – +4.7 ± 0.3VDC

TP206 –

MRG NOMINAL – +0.6 ± 0.6VDC
MRG UNDER – +4.7 ± 0.3VDC

TP207 –

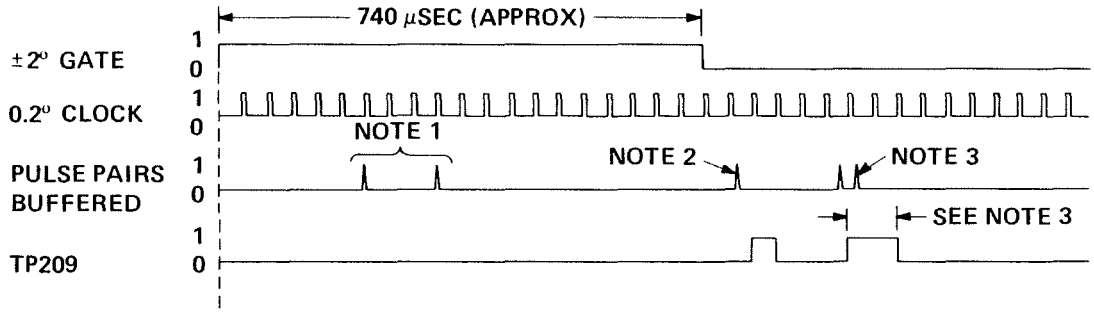
ARG NOMINAL – +0.3 ± 0.3VDC
ARG OVER – +4.7 ± 0.3VDC

TP208 –

ARG NOMINAL – +0.6 ± 0.6VDC
ARG UNDER – +4.7 ± 0.3VDC

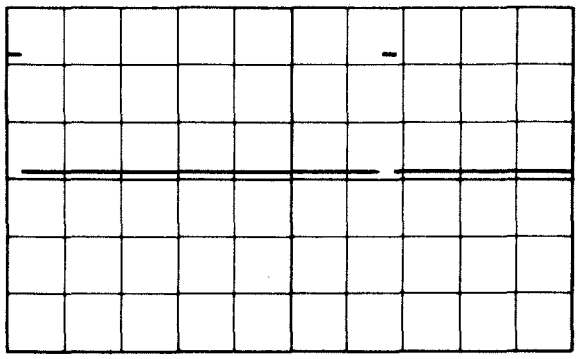
Figure 908. Signal Analyzer Unit Test Point Data (Sheet 2 of 5)

TP209 – DATA

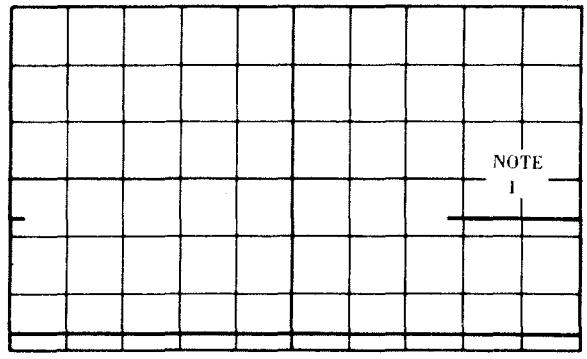


NOTES:
1. NO OUTPUT AT TP209 WHEN PULSE PAIRS BUFFERED OCCUR WITHIN ±2° GATE.
2. FOR EVERY PULSE PAIRS BUFFERED PULSE, PULSE AT TP209 IS 37.5 μSEC WIDE.
3. IF SPACING BETWEEN PULSE PAIRS BUFFERED PULSES IS LESS THAN 37.5 μSEC WIDE, OUTPUT AT TP209 IS GREATER THAN 37.5 μSEC (IN MULTIPLES OF 37.5 μSEC).

Figure 908. Signal Analyzer Unit Test Point Data (Sheet 3 of 5)



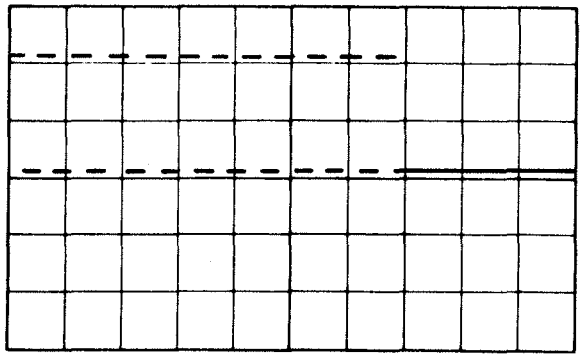
TP301 10MS/CM
SYNC – INT 2V/CM
SLOPE +



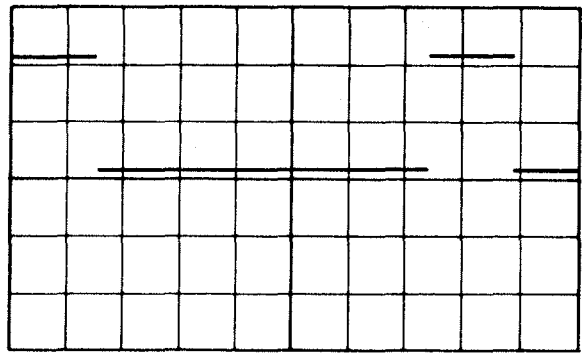
TP303 500 μSEC/CM
SYNC ON POSITIVE-GOING 2V/CM
TRANSITION OF 15S SIGNAL

NOTE 1

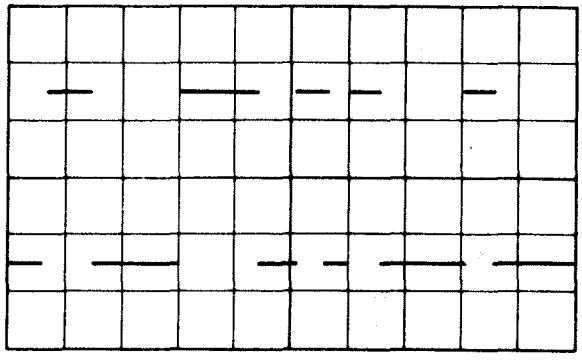
THIS AREA OF WAVEFORM CONSISTS OF PULSES AS SHOWN IN WAVEFORM BELOW.



TP304 1MS/CM
SYNC – INT 2V/CM
SLOPE +
15 HZ PHASE = +20 DEGREES



TP303 5 μSEC/CM
SYNC - INT 2V/CM
SLOPE +



TP305 0.2 SEC/CM
SYNC – INT 5V/CM
SLOPE +
(TYPICAL WAVEFORM)

Figure 908. Signal Analyzer Unit Test Point Data (Sheet 4 of 5)

TP302 AND TP308 –

ADJUST SIMULATOR FOR INDICATED BEARING DEGREES READOUT ON PANEL UNIT. SET COURSE SELECT TO 000. CHECK FOR VOLTAGES AT TP302 AND TP308.

BEARING DEGREES	BEARING DEVIATION	TP302	TP308 (NO LOAD)	TP308 PRECISION 1000-OHM LOAD)
000.0	0°	0 ± 0.2V	0 ± 0.2V	0 ± 3MV
000.2	0.2°	-0.2 ± 0.2V	-0.2 ± 0.2V	-3 ± 3MV
000.6	0.6°	-0.6 ± 0.2V	-0.6 ± 0.2V	-9 ± 3MV
001.4	1.4°	-1.4 ± 0.2V	-1.4 ± 0.2V	-21 ± 3MV
002.4	2.4°	-2.4 ± 0.2V	-2.4 ± 0.2V	-36 ± 3MV
003.4	3.4°	-3.4 ± 0.2V	-3.4 ± 0.2V	-51 ± 3MV
358.4	1.6°	+1.6 ± 0.2V	+1.6 ± 0.2V	+24 ± 3MV
006.4	6.4°	-6.3 ± 0.2V	-6.3 ± 0.2V	-96 ± 3MV
SET COURSE SELECT TO 180				
006.4	6.4°	-6.3 ± 0.2V	+6.3 ± 0.2V	+96 ± 3MV
ON PANEL UNIT, SET OBS CONTROL TO AUTO				
006.4	6.4°	+3.6 ± 0.2V	+3.6 ± 0.2V	+54 ± 3MV

TP306 — TACAN AGC

R-F LEVEL	
-50 DB	+3.7V NOMINAL
-20 DB	-2.7V NOMINAL
-80 DB	+6.6V NOMINAL

TP309 —

15 HZ PHASE 0° — 0 ± 0.5VDC
15 HZ PHASE +10° — +5 ± 0.5VDC
15 HZ PHASE -10° — -5 ± 0.5VDC

Figure 908. Signal Analyzer Unit Test Point Data (Sheet 5 of 5)

9. CONSOLE DISPLAY AND CONTROL PANEL UNIT TROUBLESHOOTING

Refer to the Console Display and Control Panel Unit (Panel Unit) troubleshooting sequence chart figure 909 to relate the typical malfunction or failure to an individual circuit or subassembly. Since the Panel Unit consists of a number of independent or semi-independent circuits and since any problem can easily be isolated to one of these circuits, it may not be necessary to analyze the complete troubleshooting chart but rather only the section (or function) pertinent to the specific fault. When the problem has been isolated to a subassembly (or section), refer to the applicable theory given in the Description and Operation section. Figure 910 is the Panel Unit troubleshooting flow chart. Figure 911 identifies the test point data for the Panel Unit. The test hookup required to check the Panel Unit is given on figure 803. Refer to paragraph 1 for a listing of schematic, logic, and wiring diagrams of the Panel Unit.

Section	Symptom		Possible Cause
Power Supply (figure 927)	15 V, 400 Hz:	Out of tolerance (15 ±2 Vac rms)	A-c input to Panel Unit not at 115 ±11.5 Vac, 400 ±20 Hz.
			T7401 shorted, CR7402, C7402
	:	Missing	T7401 open
	5 V, 400 Hz:	Out of tolerance (9 ±1 Vac rms)	T7401 shorted, CR7401, Q7401
	+5 Vdc:	Out of tolerance (5±0.3 V dc) or missing at TP105	CR7401, C7401, Q7401
	-15 Vdc:	Out of tolerance (-15 ±2 Vdc) or missing at TP106	CR7402, C7402
Range Nautical Miles Circuit (numerical display) figures 927, 928, and 10.	RANGE NAUTICAL MILES 0.1 digit numerical indication is incorrect.		U104, U116, U129
	RANGE NAUTICAL MILES 1's digit numerical indication is incorrect.		U103, U115, U129
	RANGE NAUTICAL MILES 10's digit numerical indication is incorrect.		U102, U112, U123
	RANGE NAUTICAL MILES 100's digit numerical indication is incorrect.		U101, U111, U123
	RANGE NAUTICAL MILES entire numerical indication is incorrect.		U123, U129, U124, Q104, U202B, U203B, U202A, U203E, U204A, U203D, U201B, U201A, U202C, U130A, U204B

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 1 of 7)

Section	Symptom	Possible Cause
Range Nautical Miles Circuit (blank display) figures 927, 928, and 10.	RANGE NAUTICAL MILES 0.1 position is not blank when test set is in standby mode or during a DME failure.	U104, U116
	RANGE NAUTICAL MILES 1's position is not blank when test set is in standby mode or during a DME failure.	U103, U115
	RANGE NAUTICAL MILES 10's position is not blank when test set is in standby mode or during a DME failure.	U102, U112
	RANGE NAUTICAL MILES 100's position is not blank when test set is in standby mode or during a failure.	U101, U111
	RANGE NAUTICAL MILES is not blank (all positions) when test set is in standby mode.	U204C, U202B, U203B, U202A, CR202
	RANGE NAUTICAL MILES is not blank (all positions) during a DME failure.	U203F, U203A, U204C, U202B, U203B, U202A
Range Nautical Miles Circuit (dash display) figures 927, 928, and 10.	RANGE NAUTICAL MILES 0.1 position fails to display a dash when test set is operated in transmit mode and "no computed data bit" is a logical 1.	U104, U116
	RANGE NAUTICAL MILES 1's position fails to display a dash when test set is operated in transmit mode and "no computed data bit" is a logical 1.	U103, U115

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 2 of 7)

Section	Symptom	Possible Cause
Range Nautical Miles Circuit (Cont)	RANGE NAUTICAL MILES 10's position fails to display a dash when test set is operated in transmit mode and "no computed data bit" is a logical 1.	U102, U112
	RANGE NAUTICAL MILES 100's position fails to display all dashes when test set is operated in transmit mode and "no computed data bit" is a logical 1.	U101, U111
	RANGE NAUTICAL MILES fails to display all dashes when test set is operated in transmit mode and "no computed data bit" is a logical 1.	U202A
Bearing Degrees Circuit (numerical display) figures 927, 928, and 11.	BEARING DEGREES 0.1 digit numerical indication is incorrect.	U110, U122
	BEARING DEGREES 1's digit numerical indication is incorrect.	U109, U121
	BEARING DEGREES 10's digit numerical indication is incorrect.	U108, U118
	BEARING DEGREES 100's digit numerical indication is incorrect.	U107, U117
	BEARING DEGREES entire numerical display is incorrect.	U202D, U203C, U204D

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 3 of 7)

Section	Symptom	Possible Cause
Bearing Degrees Circuit (blank display) figures 927, 928, and 11.	BEARING DEGREES 0.1 position is not blank when BEARING FAILURE is illuminated.	U110, U122
	BEARING DEGREES 1's position is not blank when BEARING FAILURE is illuminated.	U109, U121
	BEARING DEGREES 10's position not blank when BEARING FAILURE is illuminated.	U108, U118
	BEARING DEGREES 100's position not blank when BEARING FAILURE is illuminated.	U107, U117
	BEARING DEGREES is not blank (all positions) when BEARING FAILURE is illuminated.	U204D
Bearing Degrees Circuit (dash display) figures 927, 928, and 11.	BEARING DEGREES 0.1 position fails to display a dash when test set is in search mode.	U110, U122
	BEARING DEGREES 1's position fails to display a dash when test set is in search mode.	U109, U121
	BEARING DEGREES 10's position fails to display a dash when test set is in search mode.	U108, U118

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 4 of 7)

Section	Symptom	Possible Cause
Bearing Degrees Circuit (Cont)	BEARING DEGREES 100's position fails to display a dash when test set is in search mode.	U107, U117
	BEARING DEGREES fails to display all dashes when test set is in search mode.	U203C, U202D
Function Over/ Under LED Indicating Circuits (except SQUITTER RATE OVER and UNDER) and TO/ FROM LED Indicating Circuits. See figures 927 and 928.	ANT. SPEED ±1.8 RPM, PHASE COHER ±5°, MRG, SIZE, and ARG SIZE OVER indicators, and ARG COUNT UNDER indicator fail to illuminate when applicable abnormal beacon operating condition is simulated, and TO or FROM indicators fail to illuminate at appropriate time.	Q106, Q107
Squitter Rate Function Over and Under LED Indicating Circuit (figures 927 and 928)	SQUITTER RATE ±5% OVER or UNDER indicators fail to illuminate when applicable abnormal operating condition is simulated.	Q108, U131 (over), U125 (under)
Antenna Speed Over and Under LED Indicating Circuit (figures 927 and 928)	ANT. SPEED ±1.8 RPM OVER or UNDER indicators fail to illuminate when applicable abnormal operating condition is simulated.	U120 (over), U114 (under)
Phase Coherency Over and Under LED Indicating Circuit (figures 927 and 928)	PHASE COHER ±5° OVER and UNDER indicators fail to illuminate when applicable abnormal operating condition is simulated.	U132 (over), U126 (under)

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 5 of 7)

Section	Symptom	Possible Cause
MRG Size Over and Under LED Indicating Circuit (figures 927 and 928)	MRG SIZE OVER and UNDER indicators fail to illuminate when applicable abnormal operating condition is simulated.	U133 (over), U127 (under)
ARG Size Over and Under LED Indicating Circuit (figures 927 and 928)	ARG SIZE OVER and UNDER indicators fail to illuminate when applicable abnormal operating condition is simulated.	U137 (over), U135 (under)
ARG Count Under Indicating Circuit (figures 927 and 928)	ARG COUNT UNDER indicator fails to illuminate when applicable abnormal operating condition is simulated.	U136
To/From Indicating Circuit (figures 927 and 928)	TO indicator fails to illuminate or extinguish and/or FROM indicator fails to illuminate or extinguish when the appropriate conditions occur.	Q101, Q102, Q103, U105 (TO), U106 (FROM)
Range Failure Indicating Circuit (figures 927 and 928)	RANGE FAILURE indicator fails to illuminate when there is a failure in the DME.	Q105, U113
Bearing Failure Indicating Circuit (figures 927 and 928)	BEARING FAILURE indicator fails to illuminate when there is a failure in the Digital Bearing Unit.	U119
Switch Circuits (figures 927 and 12)	Any suspected switch failure can be confirmed by performing a continuity check.	Faulty switches S7401, S7405, S7406, S7404, S7402, S7403 (see figures 927 and 12)

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 6 of 7)

Section	Symptom	Possible Cause
Course Select Degrees Thumb-wheel Switch Circuit (figure 927)	Outputs of COURSE SELECT DEGREES thumbwheel switches are incorrect (see figure 13)	Faulty wiring. Faulty card 300.

Figure 909. Panel Unit Troubleshooting Sequence Chart (Sheet 7 of 7)

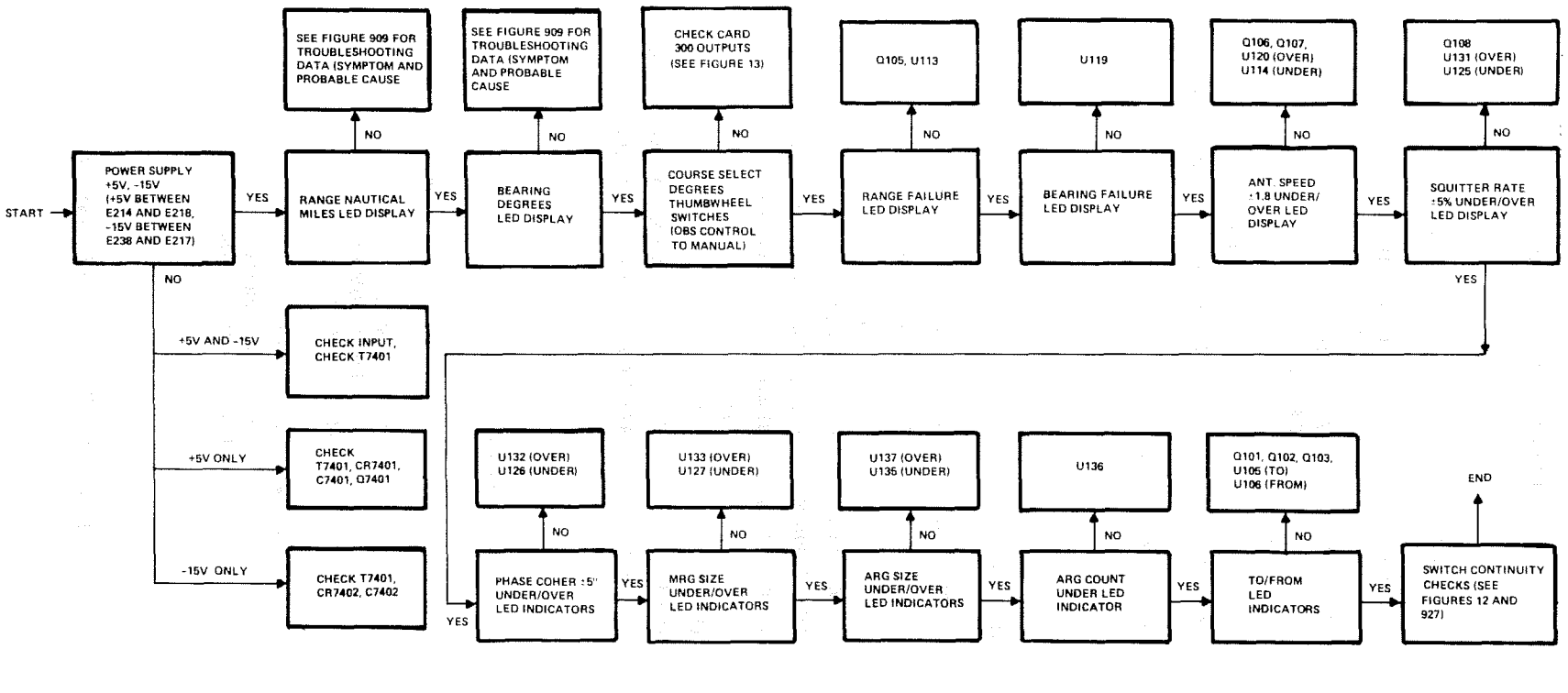


Figure 910. Panel Unit Troubleshooting Flow Chart

TEST POINT IDENTIFICATION DATA

A100 CARD, LED DISPLAY

TP101	–	U129, PIN 13	2ND SHIFT REGISTER, LAST STAGE, LAST BIT OF TENTHS DIGIT
TP102	–	U129, PIN 6	2ND SHIFT REGISTER, 4TH STAGE, LAST BIT OF UNITS DIGIT
TP103	–	U123, PIN 6	1ST SHIFT REGISTER, 4TH STAGE, LAST BIT OF HUNDREDS DIGIT
TP104	–	U123, PIN 13	1ST SHIFT REGISTER, LAST STAGE, LAST BIT OF TENS DIGIT
TP105	–	+5 VDC MAIN BUS	
TP106	–	-15 VDC UNREGULATED BUS	

A200 CARD, LED LOGIC

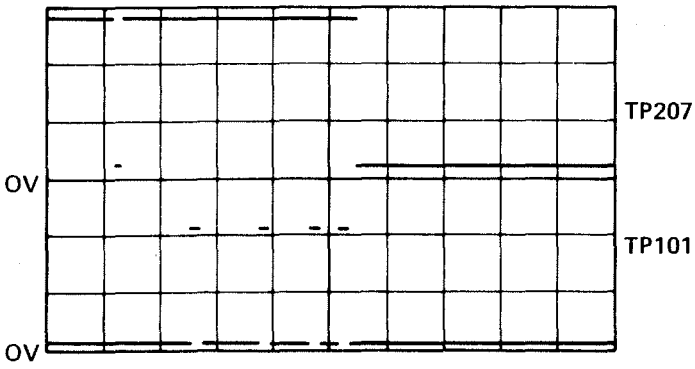
TP201	–	U202B, PIN 4	RANGE DISPLAY OVERRIDE
TP202	–	U204A, PIN 3	CLOCK, SYNC GATE
TP203	–	U204D, PIN 11	BEARING FAIL GATE
TP204	–	U203C, PIN 6	BRG DASHES BUFFER
TP205	–	U204C, PIN 8	RANGE FAIL, STANDBY GATE
TP206	–	U202D, PIN 13	BEARING DISPLAY OVERRIDE
TP207	–	INPUT	SYNC SIGNAL
TP208	–	U201B, PIN 9	1ST RANGE READOUT ENABLE FLIP-FLOP
TP209	–	U201A, PIN 5	2ND RANGE READOUT ENABLE FLIP-FLOP
TP210	–	U202B, PIN 5	RANGE READOUT SHIFT REGISTER MONITOR

POWER CIRCUIT DATA

TP105	+5.0 ± 0.4 VDC LESS THAN 50MV P-P NOISE AND/OR RIPPLE
TP106	-15.0 ± 4 VDC LESS THAN 400MV P-P NOISE AND/OR RIPPLE

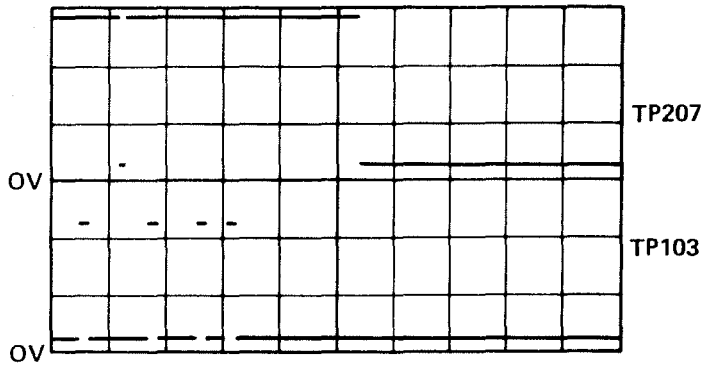
Figure 911. Panel Unit Test Point Data (Sheet 1 of 5)

RANGE INDICATING CIRCUIT DATA



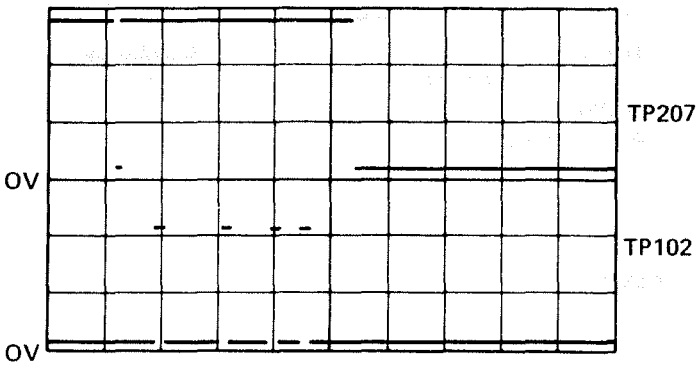
TP101 0.5 MS/CM
TP207 2V/CM

SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED
SERIAL BCD DISTANCE DATA INPUT
FROM DME IS 000.0 NAUTICAL MILES



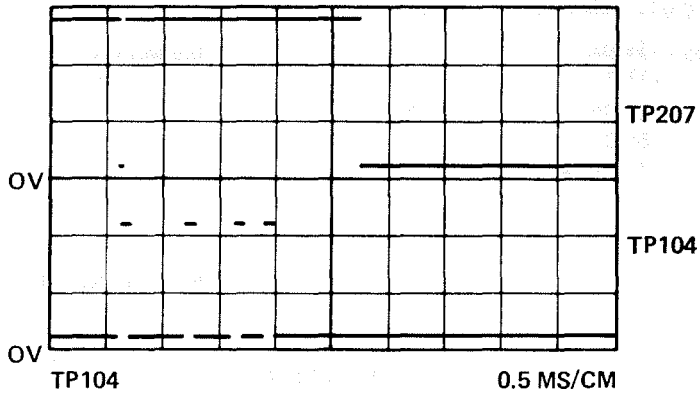
TP103 0.5 MS/CM
TP207 2V/CM

SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED
SERIAL BCD DISTANCE DATA
INPUT FROM DME IS 000.0 NAUTICAL MILES



TP102 0.5 MS/CM
TP207 2V/CM

SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED
SERIAL BCD DISTANCE DATA INPUT
FROM DME IS 000.0 NAUTICAL MILES



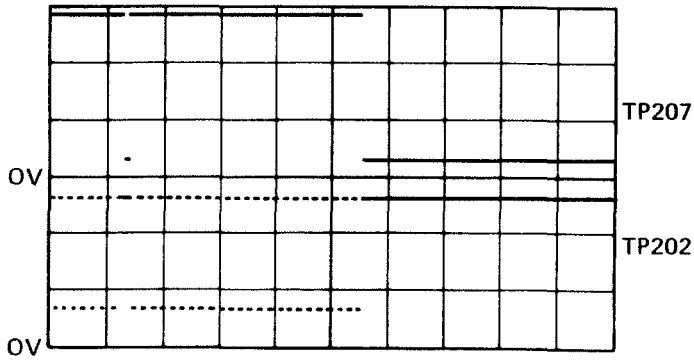
TP104 0.5 MS/CM
TP207 2V/CM

SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED
SERIAL BCD DISTANCE DATA
INPUT FROM DME IS 000.0 NAUTICAL MILES

Figure 911. Panel Unit Test Point Data (Sheet 2 of 5)

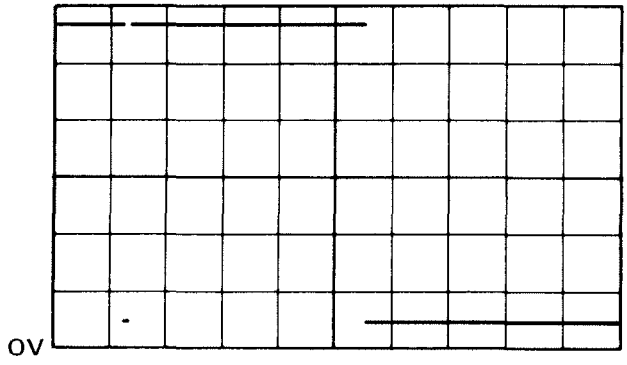
TP201 – RANGE DISPLAY OVERRIDE

TP201	TP205	TP210
1	0	0
0	1	0
0	0	1
0	1	1



TP202
TP207
SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED

0.5 MS/CM
2V/CM



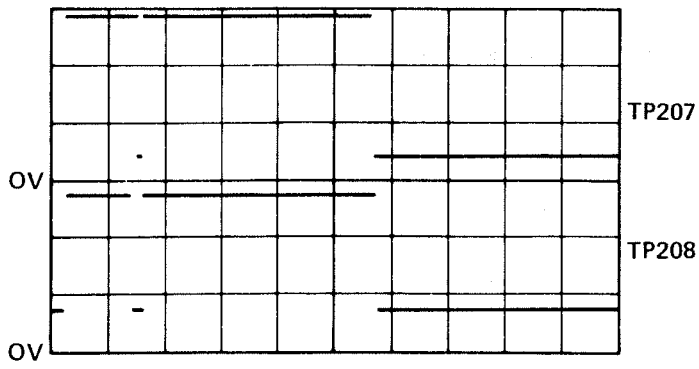
TP207
SLOPE SYNC ON TP207
SLOPE +
A-C COUPLED

0.5 MS/CM
1V/CM

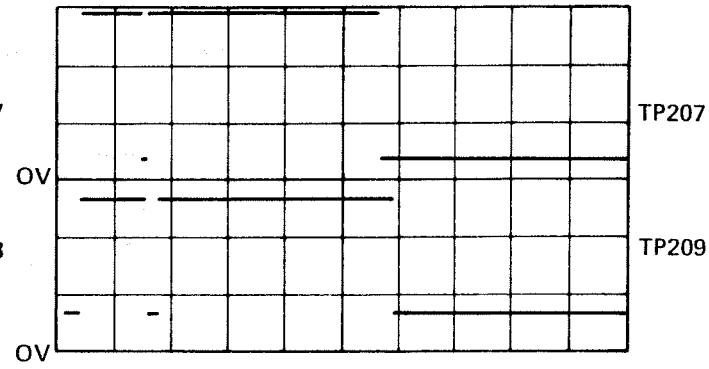
TP205 – RANGE FAIL STANDBY GATE

27.5 VDC FLAG ALARM	MANUAL STANDBY	TP205
1	1	0
1	0	1
0	1	1
0	0	1

Figure 911. Panel Unit Test Point Data (Sheet 3 of 5)



TP208 0.5 MS/CM
TP207 2V/CM
SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED



TP209 0.5 MS/CM
TP207 2V/CM
SCOPE SYNC ON TP207
SLOPE +
A-C COUPLED

TP210 – RANGE READOUT
SHIFT REGISTER
MONITOR

TP103	TP210
ACTIVE	0
NO DME LABEL CIRCULATING THROUGH 1ST SHIFT REGISTER	1

Figure 911. Panel Unit Test Point Data (Sheet 4 of 5)

BEARING INDICATING CIRCUIT DATA

TP203 – DIGITAL BEARING FAILURE BUFFER

DIGITAL BEARING FAILURE INPUT	TP203
1	0
0	1

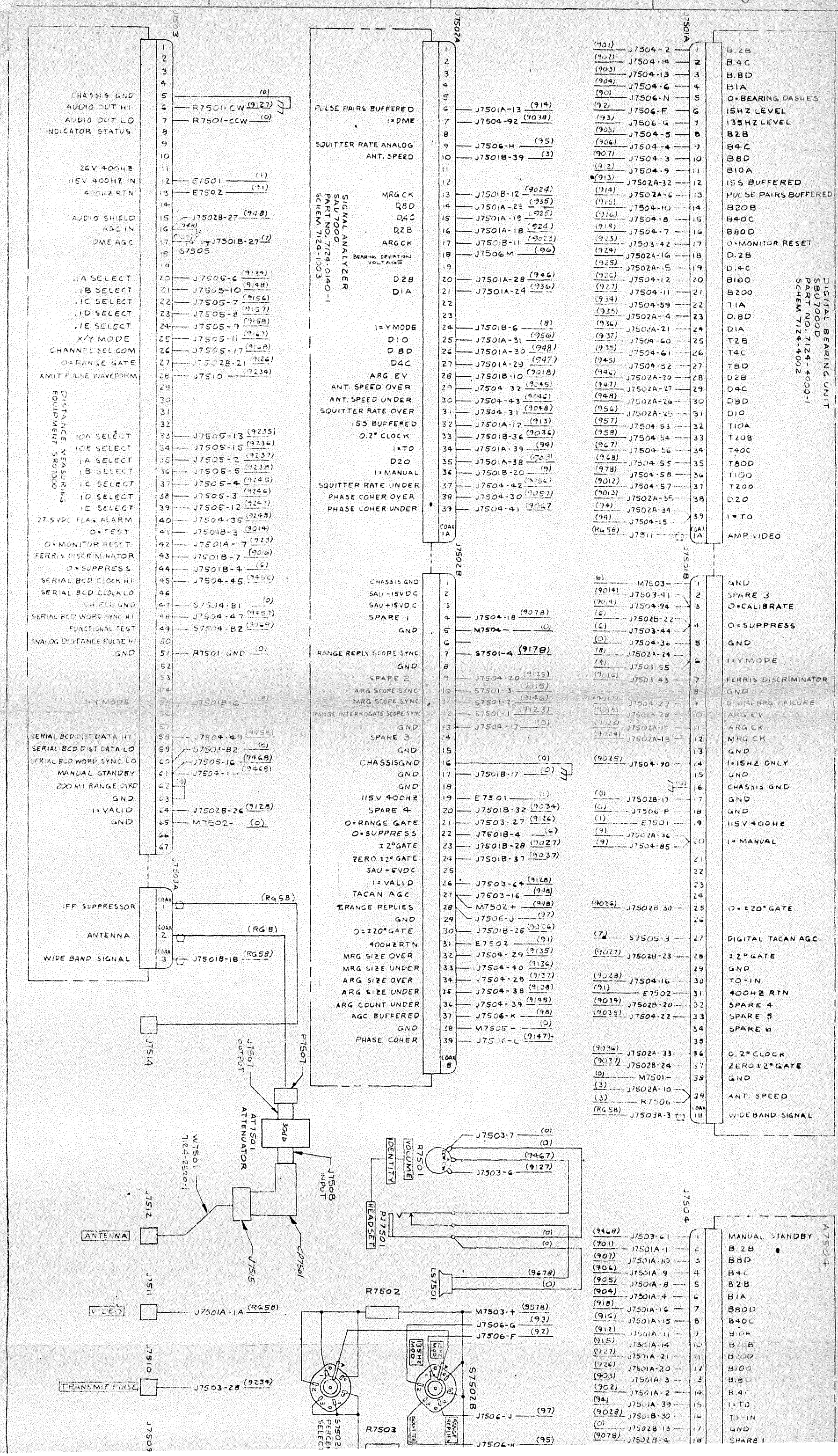
TP204 – BEARING DASHES BUFFER

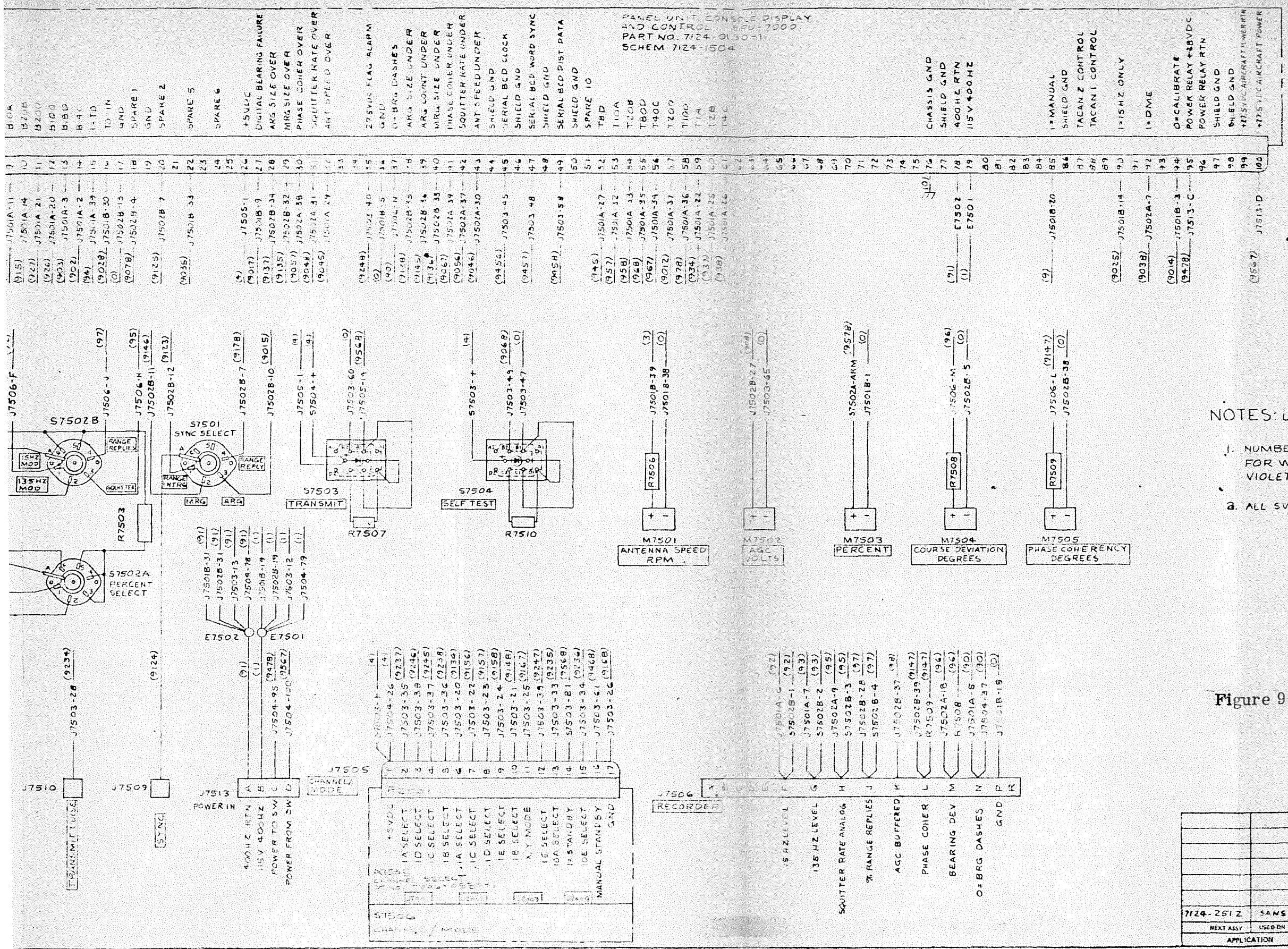
BEARING DASHES INPUT	TP204
1	0
0	1

TP206 – BEARING DISPLAY OVERRIDE

TP203	TP204	TP206
0	0	1
1	0	0
0	1	0
1	1	0

Figure 911. Panel Unit Test Point Data (Sheet 5 of 5)


J7503
CHASSIS GND
AUDIO OUT HI
AUDIO OUT LO
INDICATOR STATUS
26V 400HZ
115V 400HZ IN
400HZ RTN
AUDIO SHIELD
AGC IN
DME AGC
.1A SELECT
.1B SELECT
.1C SELECT
.1D SELECT
.1E SELECT
X/Y MODE
CHANNEL SEL COM
0=RANGE GATE
XMIT PULSE WAVEFORM
DISTANCE MEASURING EQUIPMENT SRU7000
10A SELECT
10E SELECT
1A SELECT
1B SELECT
1C SELECT
1D SELECT
1E SELECT
27.5VDC FLAG ALARM
0=TEST
0=MONITOR RESET
FERRIS DISCRIMINATOR
0=SUPPRESS
SERIAL BCD CLOCK HI
SERIAL BCD CLOCK LO
SHIELD GND
SERIAL BCD WORD SYNC HI
FUNCTIONAL TEST
ANALOG DISTANCE PULSE HI
GND
1=Y MODE
SERIAL BCD DIST DATA HI
SERIAL BCD DIST DATA LO
SERIAL BCD WORD SYNC LO
MANUAL STANDBY
200 MI RANGE OVRD
GND
1=VALID
GND
J7504A
IFF SUPPRESSOR
ANTENNA
WIDE BAND SIGNAL
J7514
J7507 OUTPUT
P7507
AT7501 ATTENUATOR
30db
W7501 7124-2520-1
J7508 INPUT
J7512
ANTENNA
J7515
CP7501
J7511
VIDEO
J7510
TRANSMIT PULSE
J7509
SIGNAL ANALYZER SAU7000 PART NO. 7124-0140-1 SCHEM 7124-1003
J7502A
PULSE PAIRS BUFFERED
1=DME
SQUITTER RATE ANALOG
ANT. SPEED
MRG CK
RBD
D4C
D2B
ARG CK
BEARING DEVIATION VOLTAGE
D2B
D1A
1=Y MODE
D1O
D8D
D4C
ARG EV
ANT. SPEED OVER
ANT. SPEED UNDER
SQUITTER RATE OVER
1SS BUFFERED
0.2° CLOCK
1=TO
D2O
1=MANUAL
SQUITTER RATE UNDER
PHASE COHER OVER
PHASE COHER UNDER
J7502B
CHASSIS GND
SAU -15VDC
SAU +15VDC
SPARE 1
GND
RANGE REPLY SCOPE SYNC
GND
SPARE 2
ARG SCOPE SYNC
MRG SCOPE SYNC
RANGE INTERROGATE SCOPE SYNC
GND
SPARE 3
GND
CHASSIS GND
GND
GND
115V 400HZ
SPARE 4
0=RANGE GATE
0=SUPPRESS
±2° GATE
ZERO ±2° GATE
SAU +5VDC
1=VALID
TACAN AGC
%RANGE REPLIES
GND
0=±20° GATE
400HZ RTN
MRG SIZE OVER
MRG SIZE UNDER
ARG SIZE OVER
ARG SIZE UNDER
ARG COUNT UNDER
AGC BUFFERED
GND
PHASE COHER
J7501A
B.2B
B.4C
B.8D
B1A
0=BEARING DASHES
15HZ LEVEL
135HZ LEVEL
B2B
B4C
B8D
B10A
1SS BUFFERED
PULSE PAIRS BUFFERED
B20B
B40C
B80D
0=MONITOR RESET
D.2B
D.4C
B100
B200
T1A
D.8D
D1A
T2B
T4C
T8D
T100
T200
D2O
1=TO
AMP VIDEO
J7501B
GND
SPARE 3
0=CALIBRATE
0=SUPPRESS
GND
1=Y MODE
FERRIS DISCRIMINATOR
GND
DIGITAL BRG FAILURE
ARG EV
ARG CK
MRG CK
GND
1=15HZ ONLY
GND
CHASSIS GND
GND
GND
0=±20° GATE
DIGITAL TACAN AGC
±2° GATE
GND
TO-IN
400HZ RTN
SPARE 4
SPARE 5
SPARE 6
0.2° CLOCK
ZERO ±2° GATE
GND
ANT. SPEED
WIDEBAND SIGNAL
DIGITAL BEARING UNIT SBU7000D PART NO. 7124-4000-1 SCHEM 7124-4002
J7504
A7504
MANUAL STANDBY
B.2B
B8D
B4C
B2B
B1A
B8D
B40C
B10A
B20B
B200
B100
B.8D
B.4C
1=TO
TO-IN
GND
SPARE 1
R7501
VOLUME
IDENTITY
PJ7501
HEADSET
LS7501
R7502
R7503
S7502A
PERCENT SELECT
S7502B
13.5HZ MOD
15HZ MOD
DIGITAL
RANGE REPLIES



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INC ECN [illegible]	[illegible]	[illegible]
	B	INC ECN 7124-080 RSS	[illegible]	[illegible]

NOTES: UNLESS OTHERWISE INDICATED

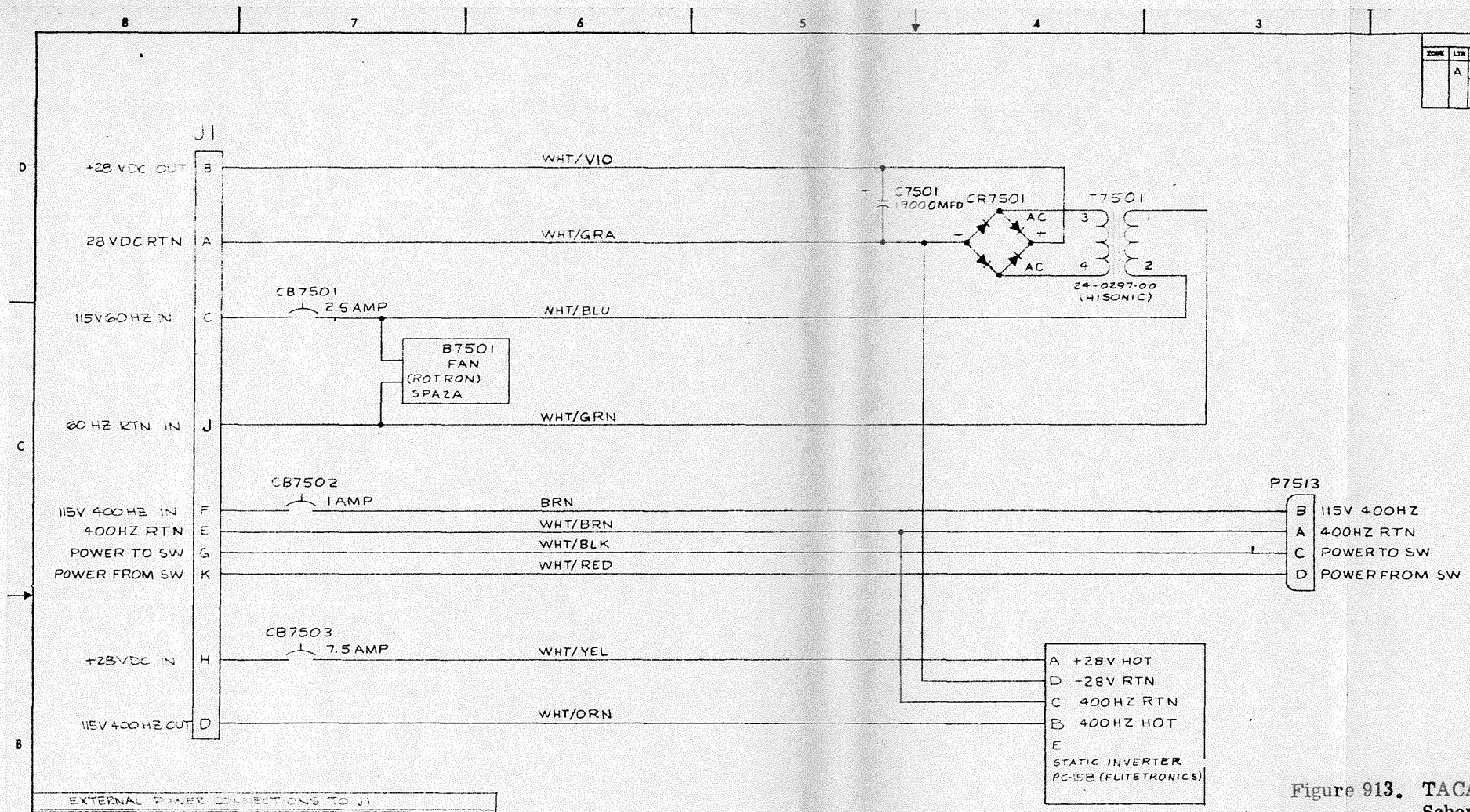
1. NUMBERS IN BRACKETS INDICATE COLOR CODE FOR WIRES I.E: (9147) IS WHITE, BROWN, YELLOW, VIOLET.

2. ALL SWITCHES SHOWN FROM REAR.

Figure 912. TACAN Beacon Test Set Interconnecting Wiring Diagram

7124-2512	SANS	DRAWN	SIERRA
NEXT ASSY	USED ON	DESIGNED	INTERCONNECTION WIRING DIAGRAM, FRONT PANEL
APPLICATION		CHECK	
		ENGRG RELEASE NOTICE	SIZE 2 / CODE IDENT NO. 12115 / 7124-2542
		CUSTOMER APPROVAL	SCALE NONE / SHEET 1 OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED J1 CONNECTION CHART ZONE 4B - PIN D WAS PIN B PIN B WAS PIN D INVERTER P/N WAS PC-14	7 MAR 73	



EXTERNAL POWER CONNECTIONS TO J1					
SOURCE POWER INPUT					
60 HZ		28 DC		400 HZ	
INPUT	TO PIN	INPUT	TO PIN	INPUT	TO PIN
115VAC	G	28 V	G	5VAC	G
115VAC RTN	J	28V RTN	A	115 AC RTN	E
JUMPER	K TO C	JUMPER	K TO H	JUMPER	K TO F
JUMPER	E TO H	JUMPER	D TO F		
JUMPER	D TO E				

Figure 913. TACAN Beacon Test Set Rear Panel Schematic Diagram

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

1.001 THRU 2.000	+.012 −.001	
.751 THRU 1.000	+.010 −.001	
.501 THRU .750	+.008 −.001	
.251 THRU .500	+.006 −.001	
.126 THRU .250	+.005 −.001	
.013 THRU .125	+.004 −.001	
NOMINAL DIA	TOLERANCE	
HOLE TOLERANCES		

NEXT ASSY	USED ON
7124-2523	SANS
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
XX ± .03 | .XXX ± .010 | ANGLES ± 0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

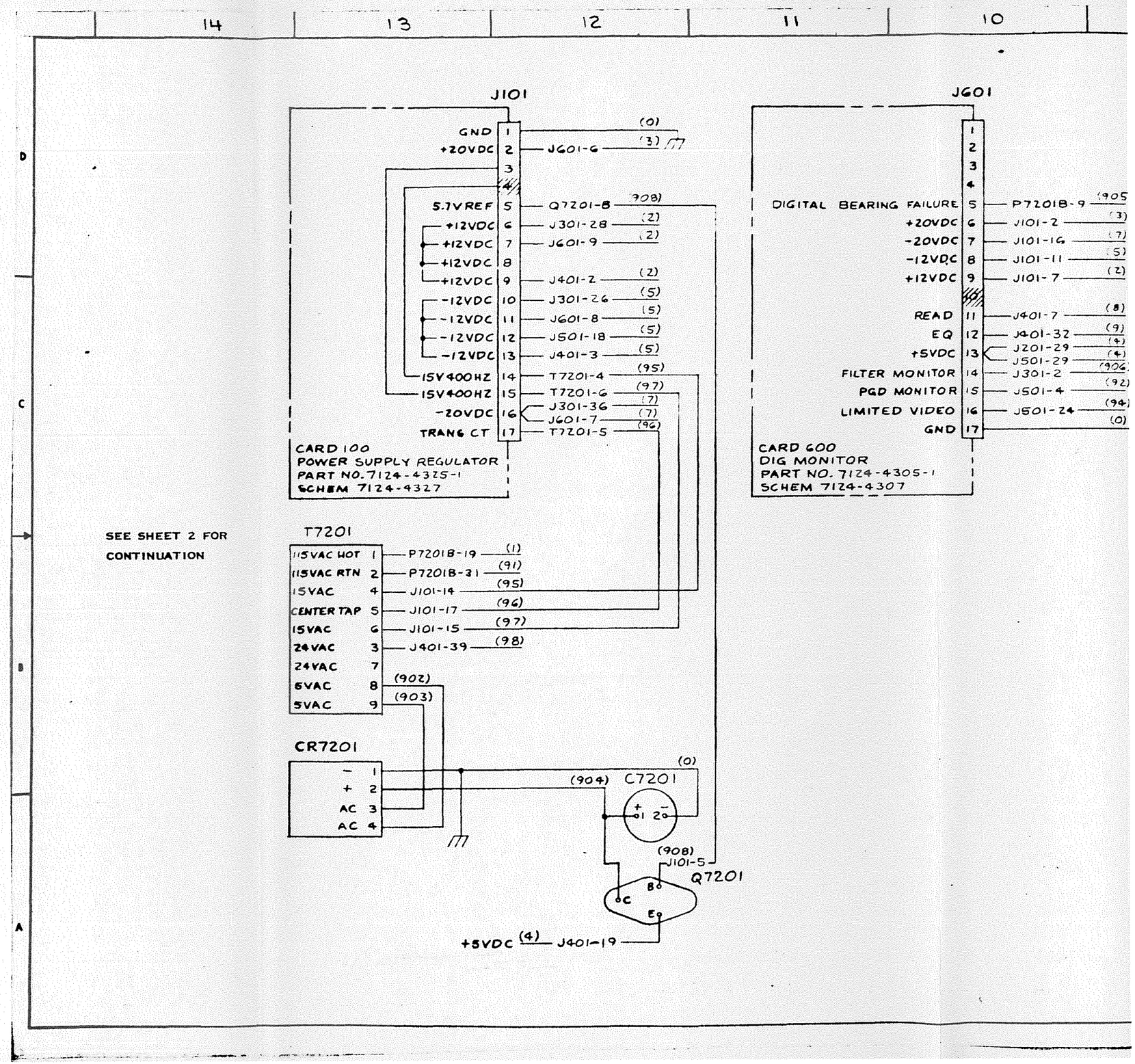
DRAWN 28 NOV 72
DESIGNER
CHECK
ENGR
APPD 20 MAR 73
CONT NO. 7124-052 20 MAR 73
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

SIERRA ELECTRONICS RESEARCH CORP.
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, FAA TACAN BEACON TEST SET, REAR PANEL

SIZE D | CODE IDENT NO. 12115 | 7124-2505

SCALE NONE | SHEET 1 OF 1


14
13
12
11
10
D
C
B
A
J101
GND 1
+20VDC 2
3
4
5.1VREF 5
+12VDC 6
+12VDC 7
+12VDC 8
+12VDC 9
-12VDC 10
-12VDC 11
-12VDC 12
-12VDC 13
15V400HZ 14
15V400HZ 15
-20VDC 16
TRANS CT 17
(0)
J601-6 (3)
Q7201-8 (908)
J301-28 (2)
J601-9 (2)
J401-2 (2)
J301-26 (5)
J601-8 (5)
J501-18 (5)
J401-3 (5)
T7201-4 (95)
T7201-6 (97)
J301-36 (7)
J601-7 (7)
T7201-5 (96)
CARD 100
POWER SUPPLY REGULATOR
PART NO. 7124-4325-1
SCHEM 7124-4327
J601
1
2
3
4
DIGITAL BEARING FAILURE 5
+20VDC 6
-20VDC 7
-12VDC 8
+12VDC 9
READ 11
EQ 12
+5VDC 13
FILTER MONITOR 14
PGD MONITOR 15
LIMITED VIDEO 16
GND 17
P7201B-9 (905)
J101-2 (3)
J101-16 (7)
J101-11 (5)
J101-7 (2)
J401-7 (8)
J401-32 (9)
J201-29 (4)
J501-29 (4)
J301-2 (906)
J501-4 (92)
J501-24 (94)
(0)
CARD 600
DIG MONITOR
PART NO. 7124-4305-1
SCHEM 7124-4307
SEE SHEET 2 FOR
CONTINUATION
T7201
115VAC HOT 1
115VAC RTN 2
15VAC 4
CENTER TAP 5
15VAC 6
24VAC 3
24VAC 7
6VAC 8
5VAC 9
P7201B-19 (1)
P7201B-31 (91)
J101-14 (95)
J101-17 (96)
J101-15 (97)
J401-39 (98)
(902)
(903)
CR7201
- 1
+ 2
AC 3
AC 4
(0)
(904)
C7201
+ 1 2 -
(908)
J101-5
Q7201
B
C
E
+5VDC (4) J401-19

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED AND REDRAWN ECN 7124-[redacted]046		
	C	INC ECN 7124-058	10 APR 73	

BOTTOM CONN P7201B

		Pin	Signal
(0)		1	GND
		2	SPARE 3
(93)	J501-22	3	0=CALIBRATE
(907)	J501-26	4	0=SUPPRESS
(0)		5	GND
(912)	J501-2	6	1=Y MODE
(913)	J501-16	7	FERRIS DISCRIMINATOR
(0)		8	GND
(905)	J601-5	9	DIGITAL BEARING FAILURE
(914)	J501-21	10	ARG EV
(915)	J501-13	11	MRG CK
(916)	J501-14	12	ARG CK
(0)		13	GND
(918)	J201-26	14	1=15HZ ONLY
(0)		15	GND
(0)		16	CHASSIS GND
(0)		17	GND
(0)		18	SHIELD GND
(1)	T7201-1	19	115V 400HZ
(923)	J201-4	20	1=MANUAL
		21	
		22	
		23	SPARE 12
		24	
(924)	J201-6	25	0=±20° GATE
		26	
(925)	J301-30	27	DIGITAL TACAN AGC
(6)	J401-4	28	±2° GATE
(0)		29	GND
(926)	J401-8	30	TO-IN
(91)	T7201-2	31	400HZ RTN
		32	SPARE 4
		33	SPARE 5
		34	SPARE 6
		35	SPARE 11
(927)	J201-2	36	0.2° CLOCK BUFFERED
(90)	J401-38	37	ZERO ±2° GATE
(0)		38	GND
(934)	J401-41	39	ANT. SPEED
RG-58/U	J301-27	1A (COAX)	WIDEBAND SIGNAL

TOP CONN P7201A

		Pin	Signal
(935)	J401-29	1	B.2B
(936)	J401-28	2	B.4C
(937)	J401-30	3	B.8D
(938)	J401-27	4	B1A
(945)	J301-34	5	0=BEARING DASHES
(946)	J301-8	6	15HZ LEVEL
(947)	J301-4	7	135HZ LEVEL
(948)	J401-25	8	B2B
(956)	J401-26	9	B4C
(957)	J401-20	10	B8D
(958)	J401-18	11	B10A
(967)	J301-12	12	15S BUFFERED
(968)	J301-10	13	PULSE PAIRS BUFFERED
(978)	J401-16	14	B20B
(9012)	J401-15	15	B40C
(9013)	J401-17	16	B80D
(9014)	J301-35	17	0=MONITOR RESET
(9015)	J201-18	18	D.2B
(9016)	J201-20	19	D.4C
(9017)	J401-14	20	B100
(9018)	J401-9	21	B200
(9023)	J401-23	22	T1A
(9024)	J201-16	23	D.8D
(9025)	J201-14	24	D1A
(9026)	J401-33	25	T2B
(9027)	J401-34	26	T4C
(9028)	J401-24	27	T8D
(9034)	J201-11	28	D2B
(9035)	J201-10	29	D4C
(9036)	J201-12	30	D8D
(9037)	J201-9	31	D10
(9038)	J401-21	32	T10A
(9045)	J401-13	33	T20B
(9046)	J401-12	34	T40C
(9047)	J401-22	35	T80D
(9048)	J401-10	36	T100
(9056)	J401-11	37	T200
(9057)	J201-7	38	D20
(9058)	J201-22	39	1=TO
RG-58/U	J301-14	1A (COAX)	AMP VIDEO

NOTES: UNLESS OTHERWISE INDICATED

1. NUMBERS IN PARENTHESES INDICATE COLOR CODE FOR WIRES I.E. (912) - WHITE/BROWN/RED.
2. WIRES TO BE 24AWG, TEFLON INSULATION.
3. REFERENCE DRAWINGS:
   ASSEMBLY 7124-4000
   PARTS LIST PL7124-4000

Figure 914. Digital Bearing Unit Interconnecting, Wiring Diagram (Sheet 1 of 2)

34-50-00
Page 967/968
Oct. 1973

REV	ZONE	REQ'D	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V - VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F - FEET I - INCHES △ SEE NOTE INDICATED

1.001 THRU 2.000	+.012 -.001	
.501 THRU 1.000	+.010 -.001	
.251 THRU .500	+.008 -.001	
.121 THRU .250	+.006 -.001	
.061 THRU .120	+.005 -.001	
.002 THRU .060	+.004 -.001	7124-4000 SANS
NOMINAL DIA	TOLERANCE	NEXT ASSY USED ON
HOLE TOLERANCES		APPLICATION

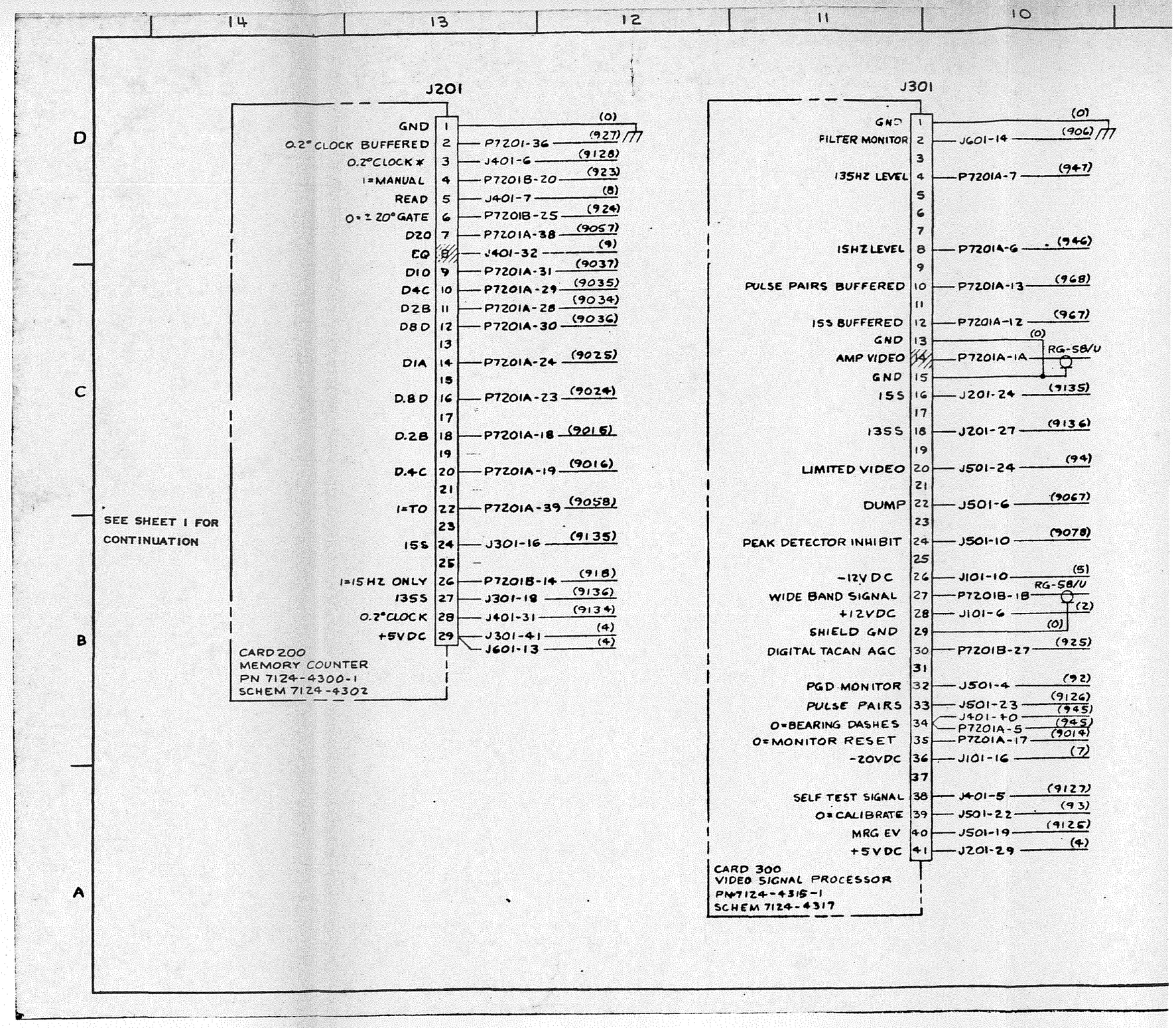
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
XX ± .03 XXX ± .010 ANGLES ± 0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

DRAWN Wmehlo 12 Feb 73
DESIGNER
CHECK
ENGR Gustlemick 4/6/73
APPR
SHEET NO.
7124-027 16 JAN 73
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

SIERRA RESEARCH CORP. ELECTRONICS
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

INTERCONNECTION WIRING DIAGRAM
DIGITAL BEARING UNIT

SIZE R | CODE IDENT NO. 12115 | 7124-4002
SCALE NONE | SHEET 1 OF 2


14
13
12
11
10
D
C
B
A
J201
GND 1 (0)
0.2° CLOCK BUFFERED 2 P7201-36 (927)
0.2° CLOCK * 3 J401-6 (9128)
1=MANUAL 4 P7201B-20 (923)
READ 5 J401-7 (8)
0=±20° GATE 6 P7201B-25 (924)
D20 7 P7201A-38 (9057)
EQ 8 J401-32 (9)
D10 9 P7201A-31 (9037)
D4C 10 P7201A-29 (9035)
D2B 11 P7201A-28 (9034)
D8D 12 P7201A-30 (9036)
13
DIA 14 P7201A-24 (9025)
15
D.8D 16 P7201A-23 (9024)
17
D.2B 18 P7201A-18 (9015)
19
D.4C 20 P7201A-19 (9016)
21
1=TO 22 P7201A-39 (9058)
23
15S 24 J301-16 (9135)
25
1=15HZ ONLY 26 P7201B-14 (918)
135S 27 J301-18 (9136)
0.2° CLOCK 28 J401-31 (9134)
+5VDC 29 J301-41 (4)
J601-13 (4)
CARD 200
MEMORY COUNTER
PN 7124-4300-1
SCHEM 7124-4302
SEE SHEET 1 FOR
CONTINUATION
J301
GND 1 (0)
FILTER MONITOR 2 J601-14 (906)
3
135HZ LEVEL 4 P7201A-7 (947)
5
6
7
15HZ LEVEL 8 P7201A-6 (946)
9
PULSE PAIRS BUFFERED 10 P7201A-13 (968)
11
15S BUFFERED 12 P7201A-12 (967)
GND 13 (0)
AMP VIDEO 14 P7201A-1A RG-58/U
GND 15
15S 16 J201-24 (9135)
17
135S 18 J201-27 (9136)
19
LIMITED VIDEO 20 J501-24 (94)
21
DUMP 22 J501-6 (9067)
23
PEAK DETECTOR INHIBIT 24 J501-10 (9078)
25
-12V DC 26 J101-10 (5)
WIDE BAND SIGNAL 27 P7201B-18 RG-58/U
+12VDC 28 J101-6 (2)
SHIELD GND 29 (0)
DIGITAL TACAN AGC 30 P7201B-27 (925)
31
PGD MONITOR 32 J501-4 (92)
PULSE PAIRS 33 J501-23 (9126)
J401-10 (945)
0=BEARING DASHES 34 P7201A-5 (945)
0=MONITOR RESET 35 P7201A-17 (9014)
-20VDC 36 J101-16 (7)
37
SELF TEST SIGNAL 38 J401-5 (9127)
0=CALIBRATE 39 J501-22 (93)
MRG EV 40 J501-19 (9126)
+5VDC 41 J201-29 (4)
CARD 300
VIDEO SIGNAL PROCESSOR
PN 7124-4316-1
SCHEM 7124-4317

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		

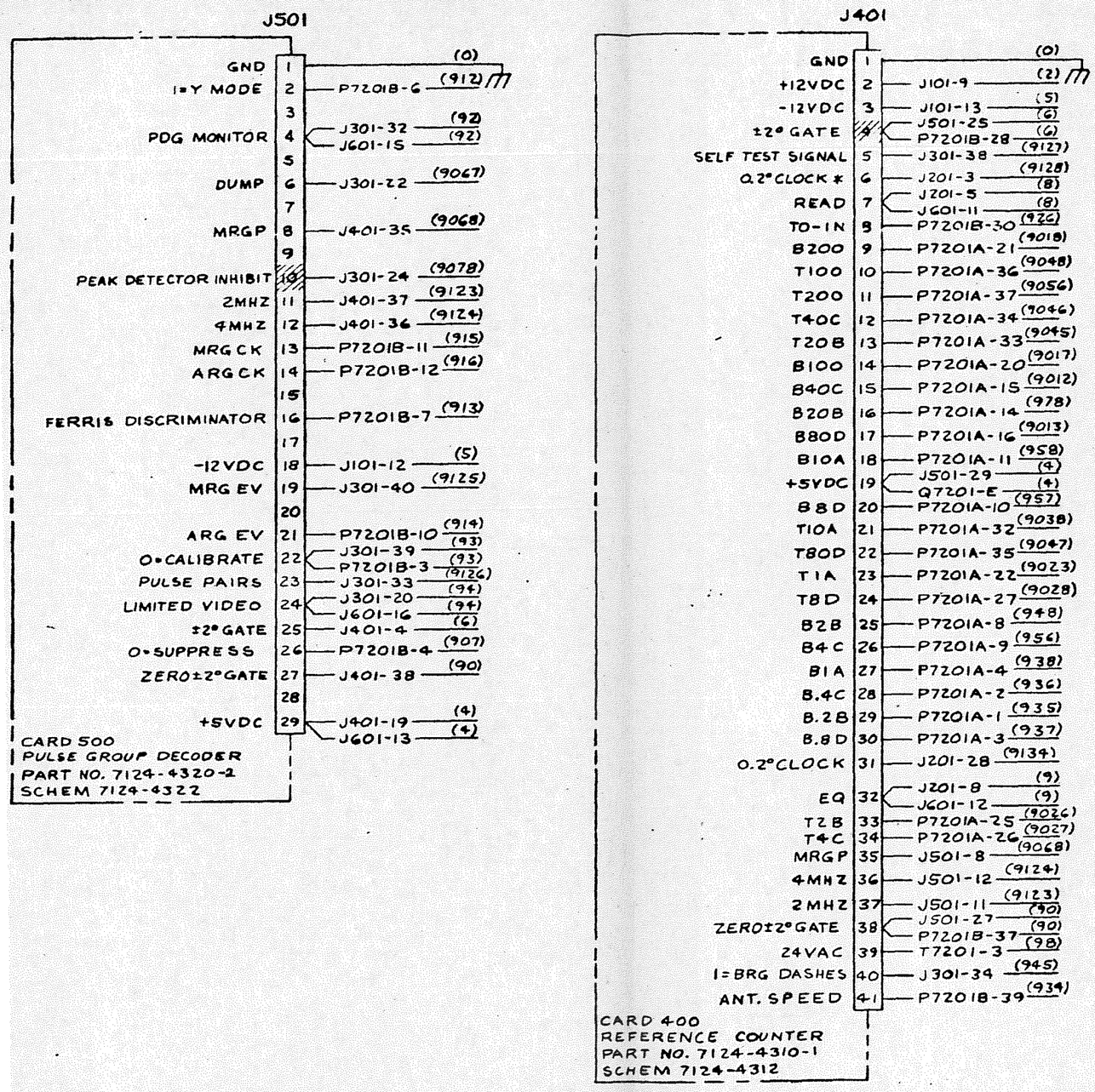


Figure 914. Digital Bearing Unit Interconnecting Wiring Diagram (Sheet 2 of 2)

QTY REQD	REV	ITEM NO.	CODE IDENT	PART OR IDENT. & FING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SCHEM CONTROL DWG # FEET I INCHES △ SEE NOTE INDICATED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: .XX ± .03 .XXX ± .010 ANGLES ± 0° 30'

BREAK ALL SHARP EDGES .015 MAXIMUM OR CHAMFER

MATERIAL

FINISH

NOMINAL DIA	TOLERANCE
1.001 THRU 2.000	+.012 −.001
.501 THRU 1.000	+.010 −.001
.251 THRU .500	+.008 −.001
.121 THRU .250	+.006 −.001
.125 THRU .250	+.006 −.001
.013 THRU .125	+.004 −.001

HOLE TOLERANCES

7124-4000 SANS

NEXT ASSY USED ON

APPLICATION

Transcribe 12 FEB 73

Tech Check 4/6/73

7124-027 16 JAN 73

SIERRA RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

INTERCONNECTION WIRING DIAGRAM
DIGITAL BEARING UNIT

SIZE	CODE IDENT NO.	
R	12115	7124-4002

SCALE NONE SHEET 2 OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
4C	A	INC ECN 7124-049 RES.	2 MAR 73	

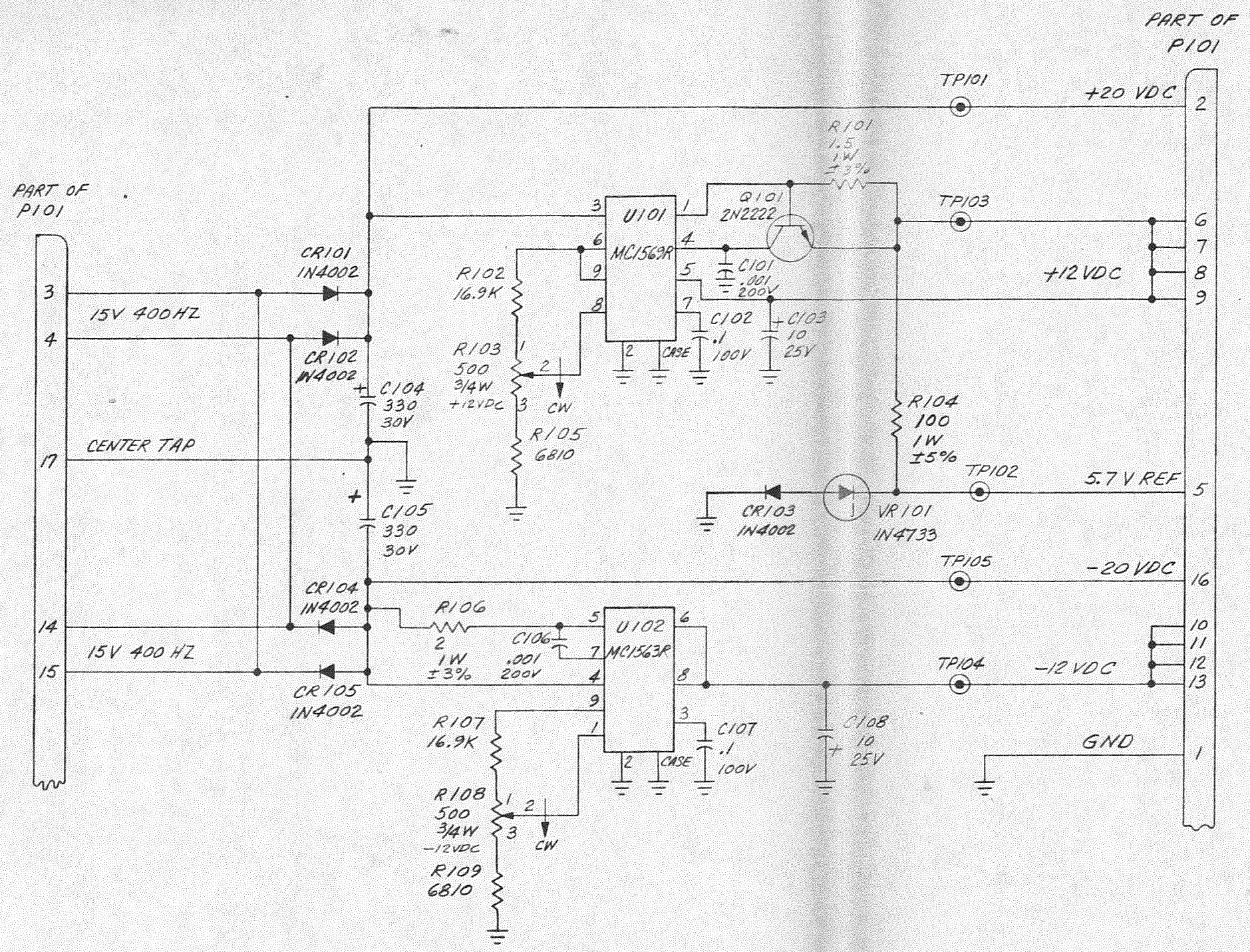


Figure 915. DBU Power Supply Regulator A100 Schematic Diagram

NOTES: UNLESS OTHERWISE INDICATED
1. ALL CAPACITANCES ARE IN MICROFARADS, UF
ALL RESISTANCES ARE IN OHMS, 1/8W, 1%.

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001	7109-3020	
NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
HOLE TOLERANCES		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ± .03 .XXX ± .010 ANGLES ± 0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

DRAWN 23MAY72
DESIGNER
CHECK
ENGR. 2AUG72
APPROV. 2AUG72
CONT NO.
7109-001 2AUG72
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

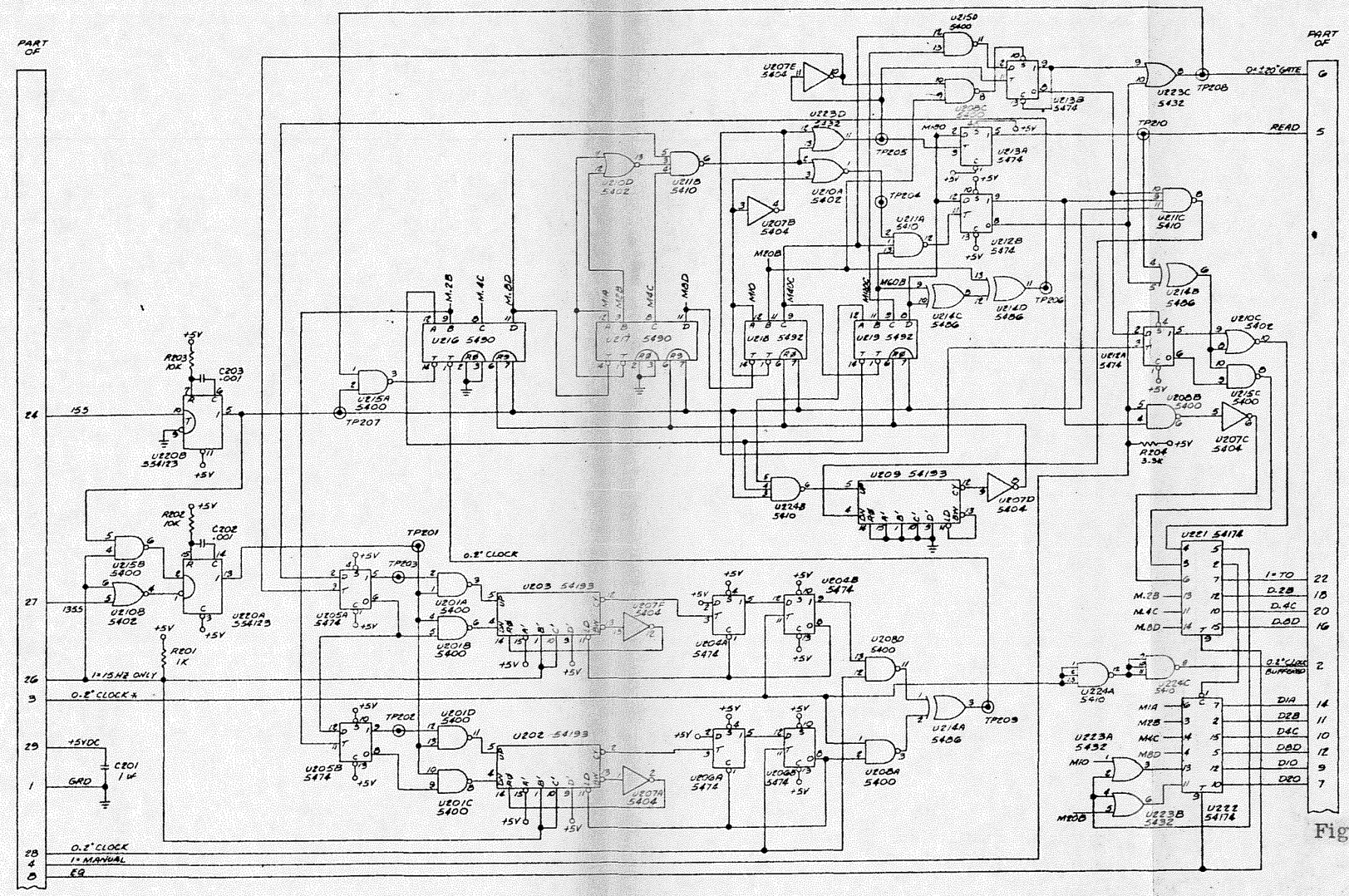
SIERRA ELECTRONICS RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM; POWER SUPPLY REGULATOR

SIZE	CODE IDENT NO.	
D	12115	7109-3022

SCALE NONE SHEET 1 OF 1

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
A	REVISED	12/11/72	
B	INC ECN 7124-038	3/14/74	



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL INTEGRATED CIRCUITS +5V ON PIN 14 AND GROUND ON PIN 7.
4. ALL 54123, 54174 AND 54193 HAVE +5V ON PIN 16 AND GROUND ON PIN 8.
5. ALL 5490 AND 5492 HAVE +5V ON PIN 5 AND GROUND ON PIN 10.

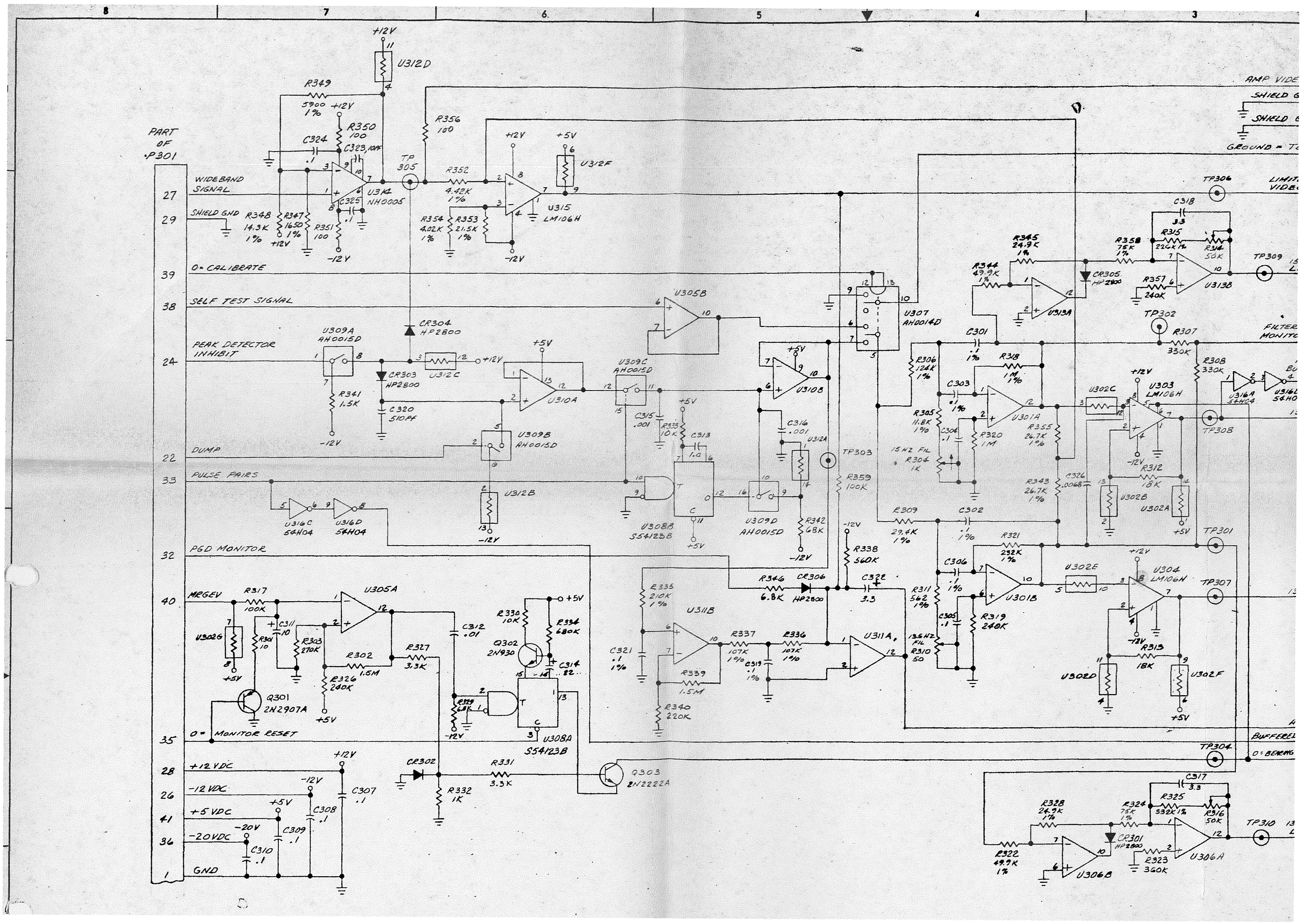
Figure 916. Memory Counter A200 Logic Diagram

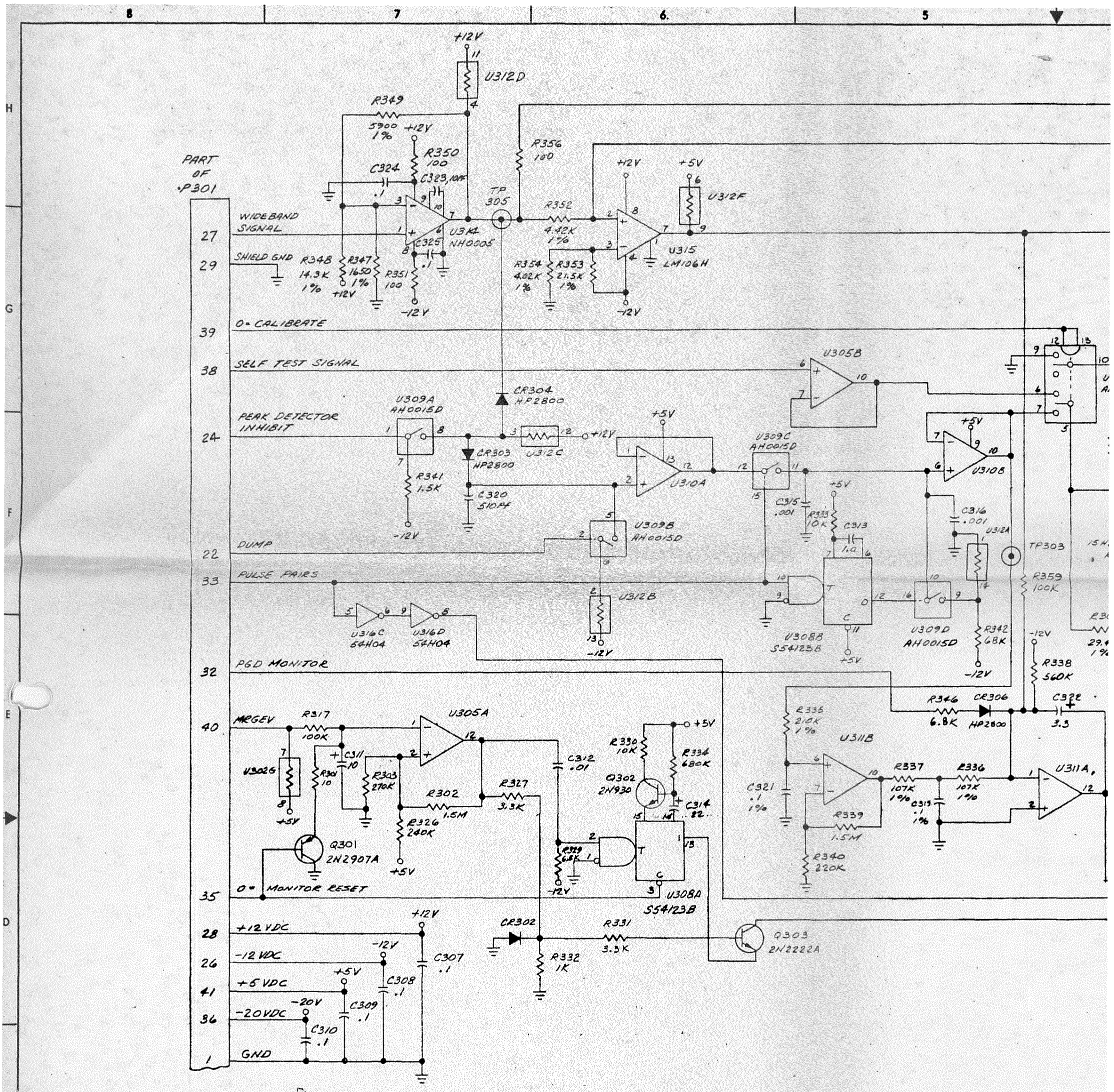
PARTS LIST

SIERRA

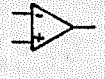
LOGIC DIAGRAM MEMORY COUNTER

E 12115 7124-4302


PART OF P301
WIDEBAND SIGNAL
SHIELD GND
0= CALIBRATE
SELF TEST SIGNAL
PEAK DETECTOR INHIBIT
DUMP
PULSE PAIRS
PGD MONITOR
MRGEV
0= MONITOR RESET
+12 VDC
-12 VDC
+5 VDC
-20VDC
GND
AMP VIDEO
SHIELD G
SHIELD G
GROUND = T
LIMIT VIDEO
FILTER MONITO
BUFFERED
0= BEARING
U312D
R349 5900 1%
R350 100
C324 .1
C323 10K
U312K NH0005
C325 .1
R348 14.3K 1%
R347 1650 1%
R351 100
R356 100
TP 305
R352 4.42K 1%
R354 4.02K 1%
R353 21.5K 1%
U312F
U315 LM106H
CR304 HP2800
U309A AH0015D
R341 1.5K
CR303 HP2800
C320 510PF
U312C
U310A
U309C AH0015D
U309B AH0015D
U312B
U316C 54H04
U316D 54H04
U308B S54123B
U309D AH0015D
U305B
U310B
C315 .001
R333 10K
C313 1.0
C316 .001
U312A
R342 68K
TP303
R359 100K
R338 560K
U307 AH0014D
R345 24.9K 1%
R344 49.9K 1%
U313A
CR305 HP2800
R358 75K 1%
C318 3.3
R315 226K 1%
R314 50K
R357 240K
U313B
TP306
TP309
TP302
R307 330K
R308 330K
U316A 54H04
TP308
C301 .1 1%
R306 124K 1%
R318 1M 1%
C303 .1 1%
R305 11.8K 1%
C304 .1
R320 1M
U301A
R355 26.7K 1%
U302C
U303 LM106H
15 HZ FIL
R304 1K
R343 26.7K 1%
C326 .0068
R312 18K
U302B
U302A
TP301
R309 29.4K 1%
C302 .1 1%
R321 232K 1%
C306 .1 1%
U301B
U302E
U304 LM106H
TP307
R311 562 1%
C305 .1
R319 240K
135 HZ FIL
R310 50
R313 18K
U302D
U302F
R335 210K 1%
U311B
C321 .1 1%
R339 1.5M
R340 220K
R337 107K 1%
R336 107K 1%
C319 .1 1%
U311A
R346 6.8K
CR306 HP2800
C322 3.3
R317 100K
U305A
C311 10
R301 10
R303 270K
R302 1.5M
R326 240K
R327 3.3K
C312 .01
U302G
Q301 2N2907A
R330 10K
R334 680K
Q302 2N930
C314 .82
R329 68K
U308A S54123B
CR302
R331 3.3K
R332 1K
Q303 2N2222A
C307 .1
C308 .1
C309 .1
C310 .1
R328 24.9K 1%
R322 49.9K 1%
U306B
C317 3.3
R325 332K 1%
R324 75K 1%
R316 50K
CR301 HP2800
R323 360K
U306A
TP310
TP304



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITORS ARE IN MICROFARADS.
3. ALL DIODES ARE 1N4148.
4. INTEGRATED CIRCUIT UGW7747312 INDICATED AS SHOWN  PIN 4 (-12V), PIN 9 & 13 (+12V)

REF DES	+5 VDC PIN	GND PIN	-20V PIN	+12 V PIN
U307	14	3	11	4
U308	16	8	—	—
U309	14	3	13	4
U316	14	7	—	—

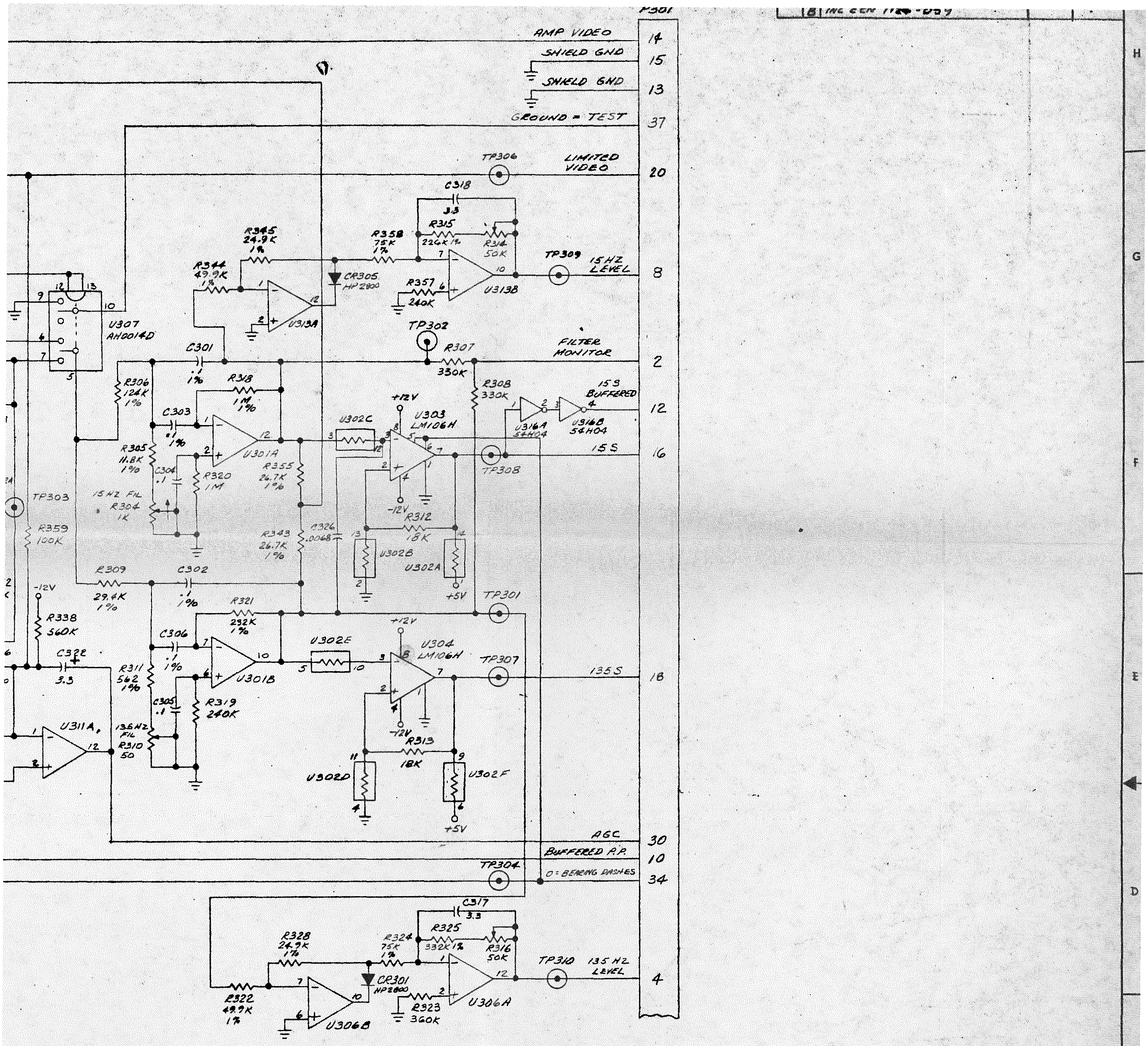


Figure 917. Digital Video Signal Processor A300
Logic Diagram

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001		
HOLE TOLERANCES		APPLICATION	

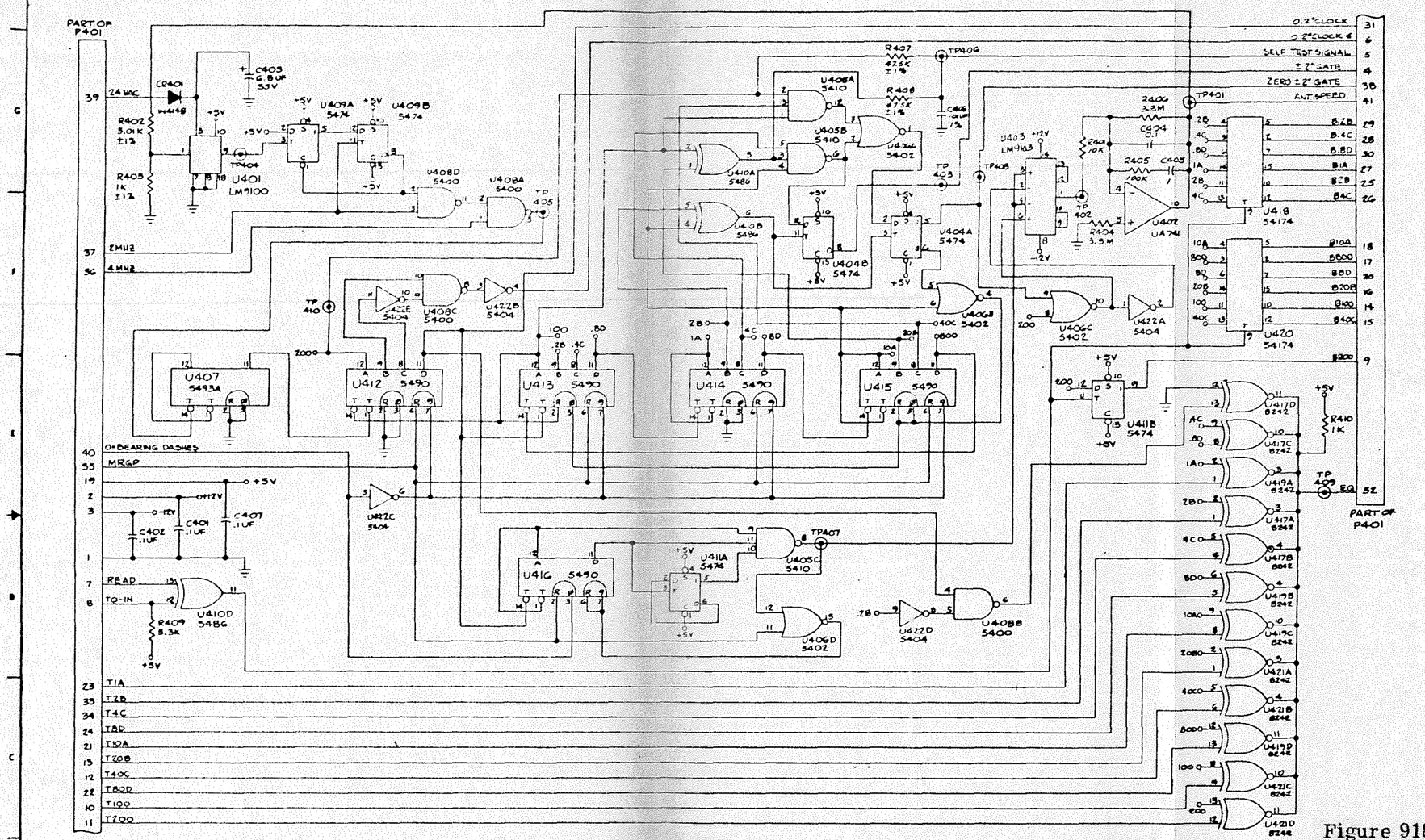
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ± .03 | .XXX ± .010 | ANGLES ± 0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

DRAWN 15 Nov 72
DESIGNER
CHECK
ENGR 12/21/72
APPD 2 JAN 73
CONT NO. 7124-022 2 JAN 73
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

ELECTRONICS SIERRA RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, DIGITAL VIDEO SIGNAL PROCESSOR

SIZE E | CODE IDENT NO. 12115 | 7124-4317
SCALE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL 54174 IC'S HAVE +5V ON PIN 16 AND GROUND ON PIN 8.
4. ALL 5490 & 5493 IC'S HAVE +5V ON PIN 5 AND GROUND ON PIN 10.
5. ALL 741 IC'S HAVE -12V ON PIN 6 AND +12V ON PIN 11.
6. ALL REMAINING IC'S HAVE +5V ON PIN 14 AND GND ON PIN 7.

Figure 918. Reference Counter A400 Logic Diagram

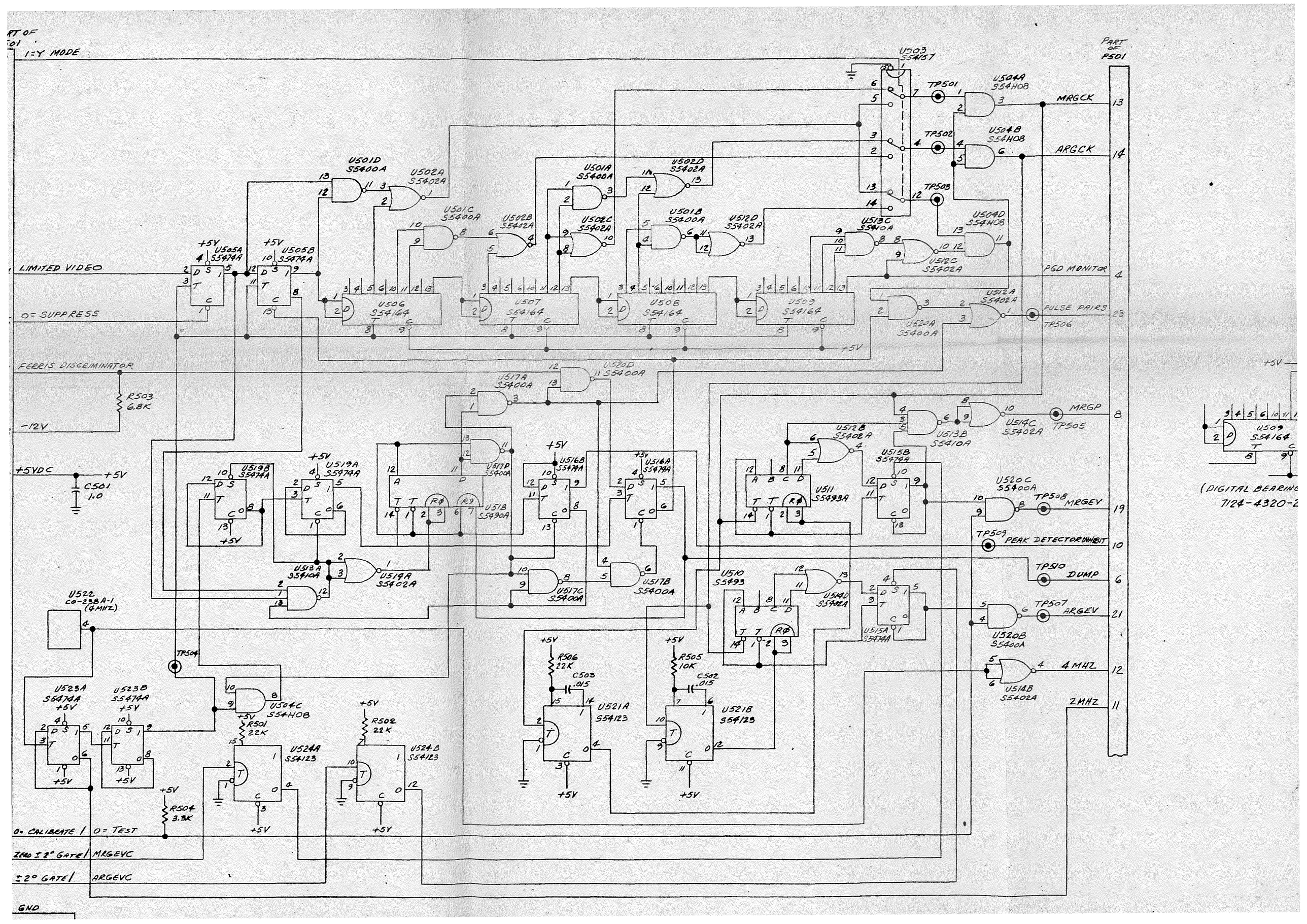
SIERRA

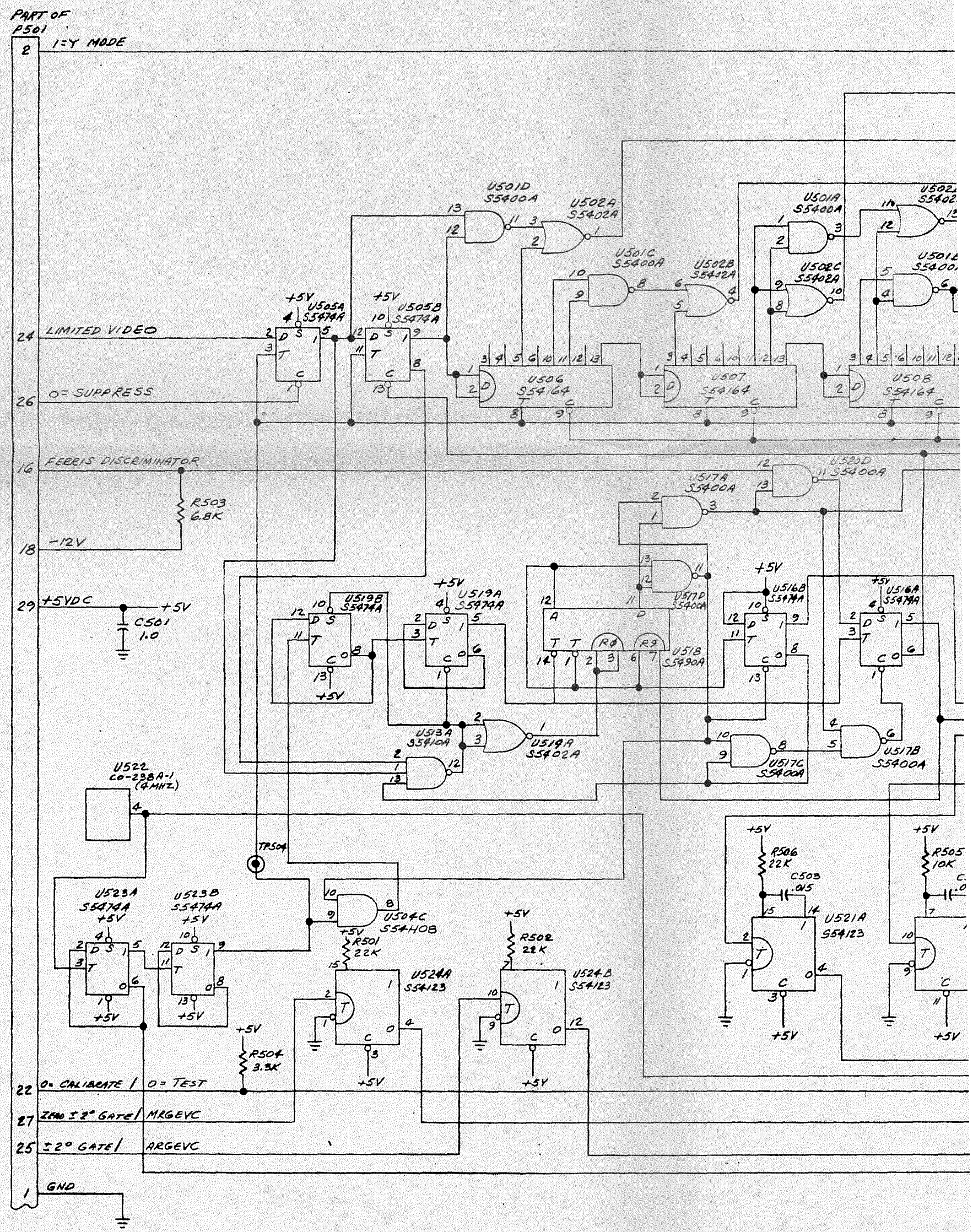
LOGIC DIAGRAM, REFERENCE COUNTER

E 12115 7124-4312

SCALE NONE

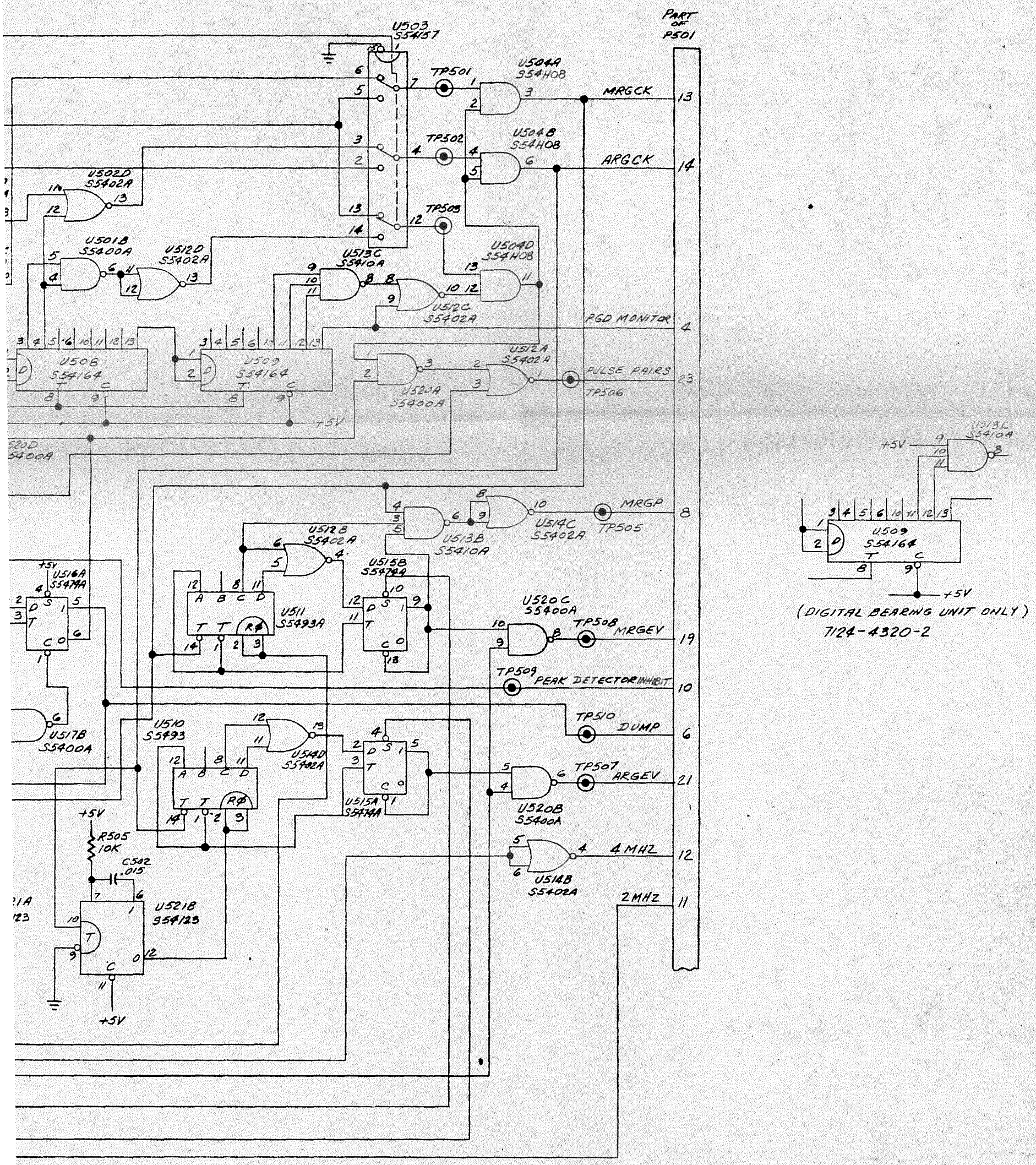
7124-4310


PART OF P501
1=Y MODE
LIMITED VIDEO
0= SUPPRESS
FERRIS DISCRIMINATOR
R503 6.8K
-12V
+5VDC
C501 1.0
U501D S5400A
U502A S5402A
U501C S5400A
U502B S5402A
U501A S5400A
U502C S5402A
U502D S5402A
U501B S5400A
U512D S5402A
U513C S5410A
U512C S5402A
U505A S5474A
U505B S5474A
U506 S54164
U507 S54164
U508 S54164
U509 S54164
U503 S54157
TP501
TP502
TP503
U504A S54H08
U504B S54H08
U504D S54H08
MRGCK
ARGCK
PGD MONITOR
U512A S5402A
PULSE PAIRS
TP506
U520A S5400A
U517A S5400A
U520D S5400A
U519B S5474A
U519A S5474A
U517D S5400A
U518 S5490A
U516B S5474A
U516A S5474A
U512B S5402A
U513B S5410A
U514C S5402A
MRGP
TP505
U511 S5493A
U515B S5474A
U520C S5400A
TP508
MRGEV
TP509
PEAK DETECTOR INHIBIT
TP510
DUMP
U513A S5410A
U514A S5402A
U517C S5400A
U517B S5400A
U510 S5493
U514D S5402A
U515A S5474A
TP507
ARGEV
U520B S5400A
U514B S5402A
4 MHZ
2 MHZ
U522 CO-238A-1 (4MHZ)
TP504
U523A S5474A
U523B S5474A
U504C S54H08
R501 22K
U524A S54123
R502 22K
U524B S54123
R504 3.3K
R506 22K
C503 .015
U521A S54123
R505 10K
C502 .015
U521B S54123
0= CALIBRATE / 0= TEST
ZERO ± 2° GATE / MRGEVC
± 2° GATE / ARGEVC
GND
(DIGITAL BEARING
7124-4320-2



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
3. ALL INTEGRATED CIRCUITS HAVE +5V ON PIN 14 AND GROUND ON PIN 7 EXCEPT U510, U511 AND U518 HAVE +5V ON PIN 5 AND GROUND ON PIN 10, AND U503, U521 AND U524 HAVE +5V ON PIN 16 AND GROUND ON PIN 8.
4. ON PINS 22, 25 AND 27 THE FIRST SIGNAL IS FOR THE DIGITAL BEARING UNIT AND THE SECOND SIGNAL IS FOR THE ANALOG BEARING UNIT.
5. U503 SWITCH SHOWN IN Y-MODE POSITION.



(DIGITAL BEARING UNIT ONLY)
7124-4320-2

Figure 919. Pulse Group Decoder A500 Logic Diagram

QTY REQD		KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001		

HOLE TOLERANCES — APPLICATION

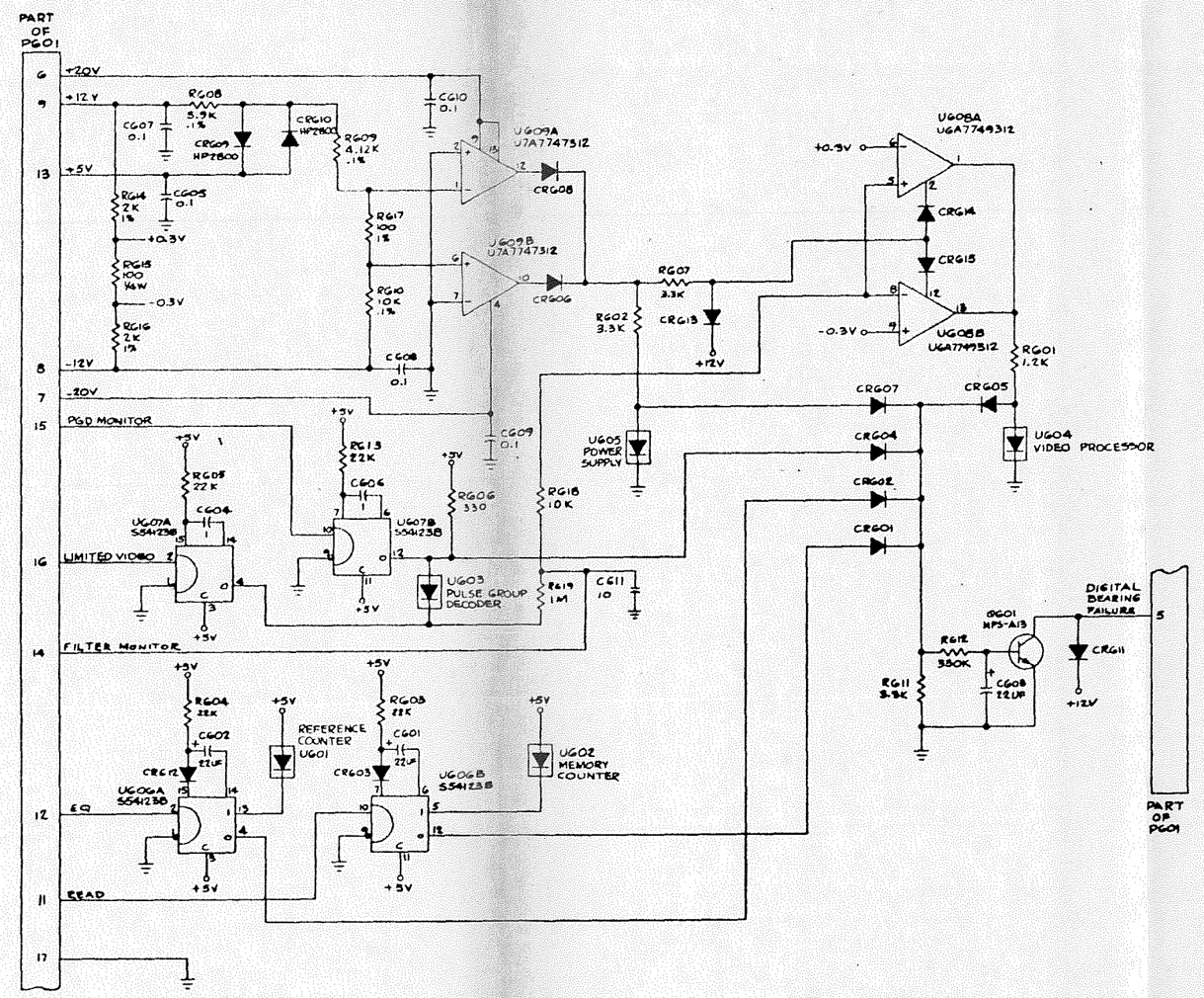
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

DRAWN G Allen 1 DEC 72
DESIGNER
CHECK
ENGR C Bartkowiak 27 DEC 72
APPD 27 DEC 72
CONT NO.
7124-019 27 DEC 72
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

SIERRA ELECTRONICS RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

LOGIC DIAGRAM, PULSE GROUP DECODER

SIZE E | CODE IDENT NO. 12115 | 7124-4322
SCALE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ½W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DIODES ARE 1N4148.
4. ON INTEGRATED CIRCUITS UG06 & UG07, GND IS PIN 8 & +5V IS PIN 16.
   ON UG08 -12V IS PIN 7 & +12V IS PIN 14.

Figure 920. Digital Bearing Unit Monitor A600 (7124-4305-1) Logic Diagram

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	INC ECN 7124-040	FEB 13 1973	

SIERRA

LOGIC DIAGRAM, DIGITAL BEARING UNIT MONITOR

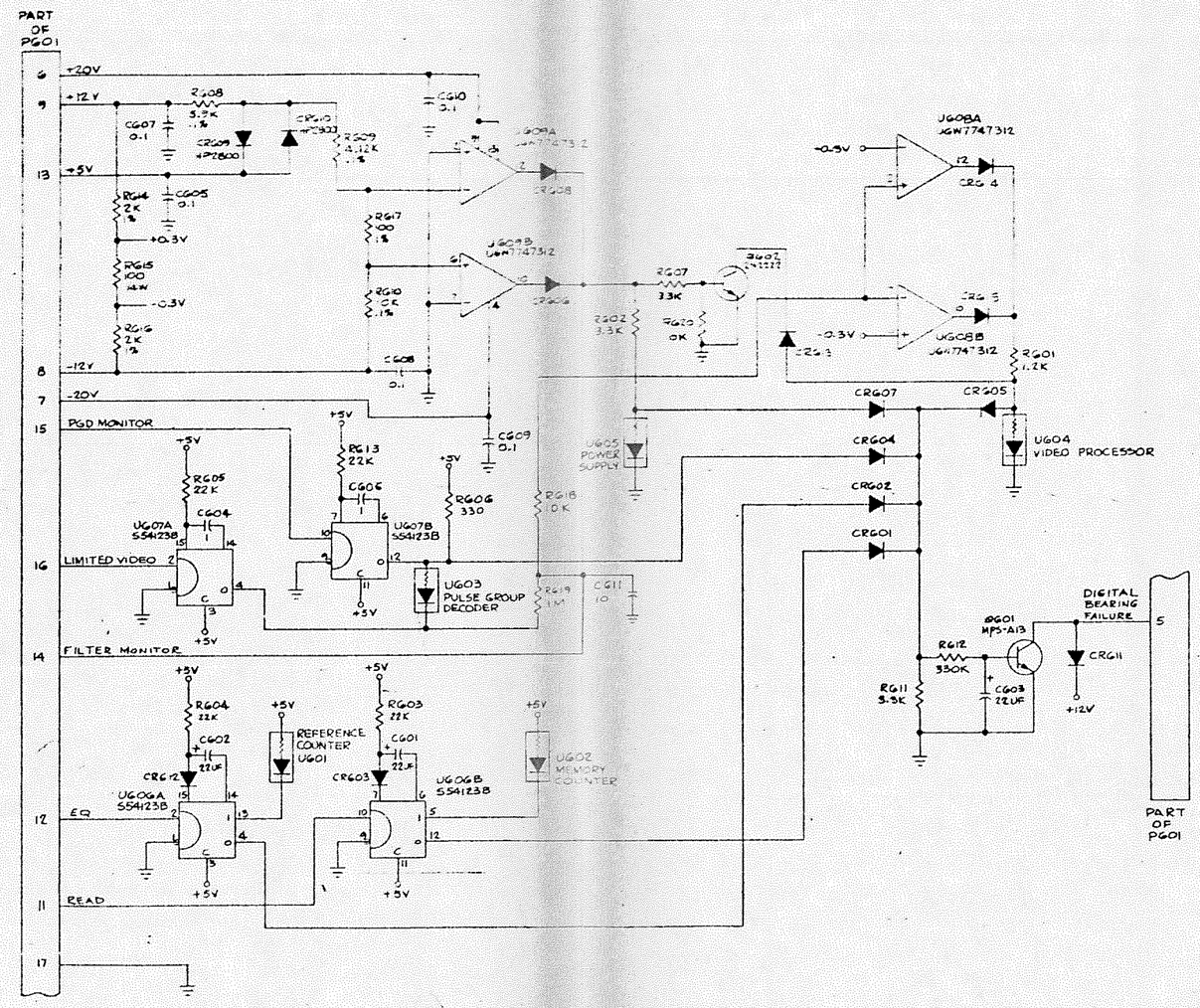
E 12115 7124-4307

7124-4305

HOLE TOLERANCES

APPLICATION

PARTS LIST



NOTES: UNLESS OTHERWISE INDICATED

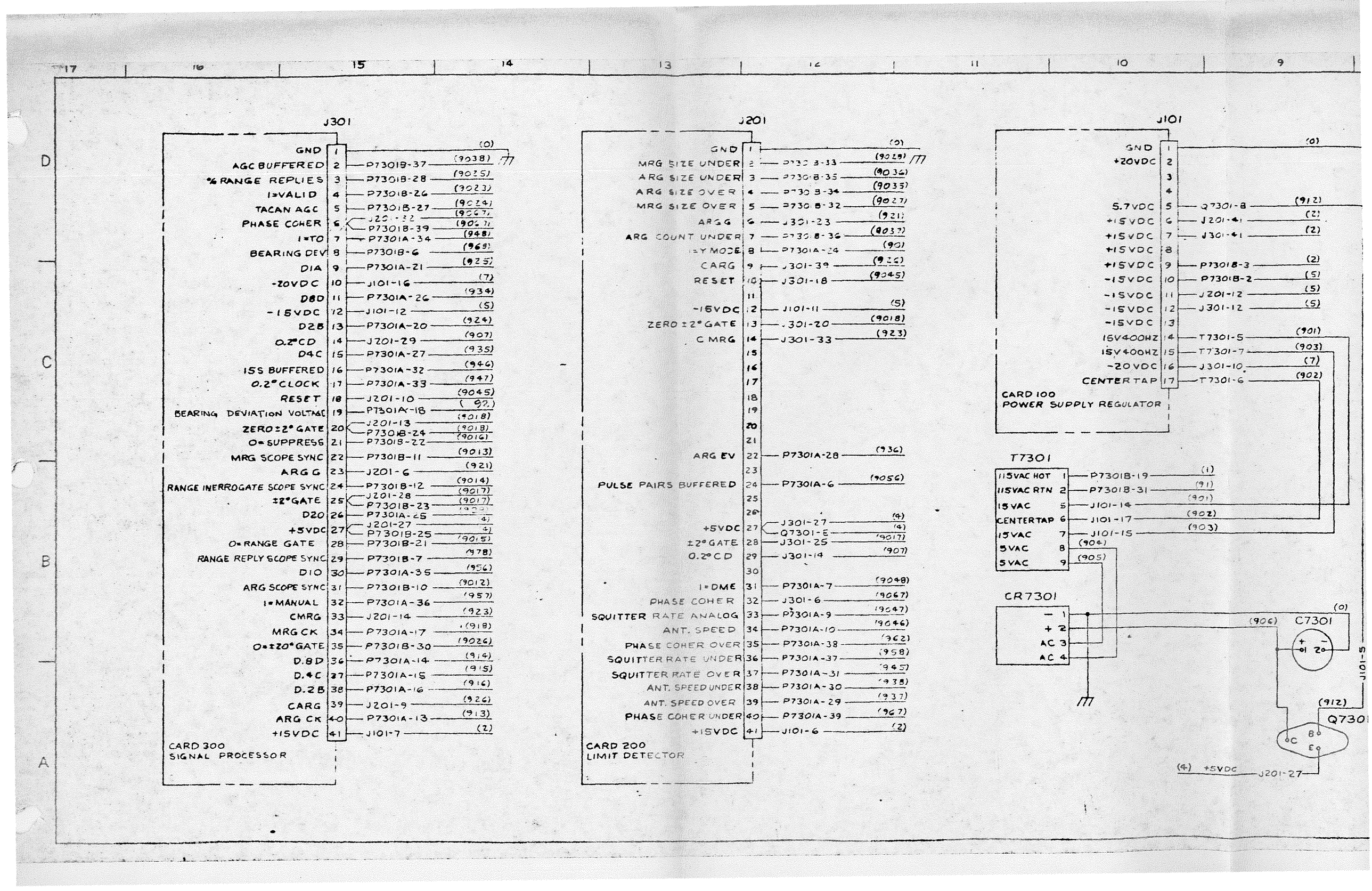
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DIODES ARE 1N4148.
4. ON INTEGRATED CIRCUITS UG06 & UG07, GND IS PIN 8 & +5V IS PIN 16.
   ON UG08 -12V IS PIN 4 & +12V IS PINS 9 & 13.

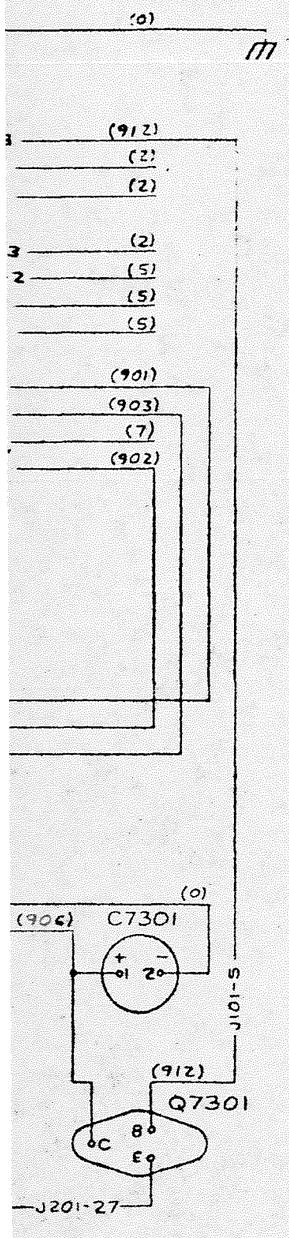
Figure 921. Digital Bearing Unit Monitor A600 (7124-4305-2) Logic Diagram

SIERRA

LOGIC DIAGRAM, DIGITAL BEARING UNIT MONITOR

E 12115 7124-4337


J301
GND 1 (0)
AGC BUFFERED 2 P7301B-37 (9038)
% RANGE REPLIES 3 P7301B-28 (9025)
1=VALID 4 P7301B-26 (9023)
TACAN AGC 5 P7301B-27 (9024)
PHASE COHER 6 J201-32 (9067) P7301B-39 (9067)
1=TO 7 P7301A-34 (948)
BEARING DEV 8 P7301B-6 (969)
D1A 9 P7301A-21 (925)
-20VDC 10 J101-16 (7)
D8D 11 P7301A-26 (934)
-15VDC 12 J101-12 (5)
D2B 13 P7301A-20 (924)
0.2°CD 14 J201-29 (907)
D4C 15 P7301A-27 (935)
1SS BUFFERED 16 P7301A-32 (946)
0.2° CLOCK 17 P7301A-33 (947)
RESET 18 J201-10 (9045)
BEARING DEVIATION VOLTAGE 19 P7301A-18 (92)
ZERO ±2° GATE 20 J201-13 (9018) P7301B-24 (9018)
0=SUPPRESS 21 P7301B-22 (9016)
MRG SCOPE SYNC 22 P7301B-11 (9013)
ARG G 23 J201-6 (921)
RANGE INERROGATE SCOPE SYNC 24 P7301B-12 (9014)
±2° GATE 25 J201-28 (9017) P7301B-23 (9017)
D20 26 P7301A-25 (904)
+5VDC 27 J201-27 (4) P7301B-25 (4)
0=RANGE GATE 28 P7301B-21 (9015)
RANGE REPLY SCOPE SYNC 29 P7301B-7 (978)
D10 30 P7301A-35 (956)
ARG SCOPE SYNC 31 P7301B-10 (9012)
1=MANUAL 32 P7301A-36 (957)
CMRG 33 J201-14 (923)
MRG CK 34 P7301A-17 (918)
0=±20° GATE 35 P7301B-30 (9026)
D.8D 36 P7301A-14 (914)
D.4C 37 P7301A-15 (915)
D.2B 38 P7301A-16 (916)
CARG 39 J201-9 (926)
ARG CK 40 P7301A-13 (913)
+15VDC 41 J101-7 (2)
CARD 300
SIGNAL PROCESSOR
J201
GND 1 (0)
MRG SIZE UNDER 2 P7301B-33 (9029)
ARG SIZE UNDER 3 P7301B-35 (9036)
ARG SIZE OVER 4 P7301B-34 (9035)
MRG SIZE OVER 5 P7301B-32 (9027)
ARG G 6 J301-23 (921)
ARG COUNT UNDER 7 P7301B-36 (9037)
1=Y MODE 8 P7301A-24 (901)
CARG 9 J301-39 (926)
RESET 10 J301-18 (9045)
11
-15VDC 12 J101-11 (5)
ZERO ±2° GATE 13 J301-20 (9018)
C MRG 14 J301-33 (923)
15
16
17
18
19
20
21
ARG EV 22 P7301A-28 (936)
23
PULSE PAIRS BUFFERED 24 P7301A-6 (9056)
25
26
+5VDC 27 J301-27 (4) Q7301-E (4)
±2° GATE 28 J301-25 (9017)
0.2° CD 29 J301-14 (907)
30
1=DME 31 P7301A-7 (9048)
PHASE COHER 32 J301-6 (9067)
SQUITTER RATE ANALOG 33 P7301A-9 (9047)
ANT. SPEED 34 P7301A-10 (9046)
PHASE COHER OVER 35 P7301A-38 (962)
SQUITTER RATE UNDER 36 P7301A-37 (958)
SQUITTER RATE OVER 37 P7301A-31 (945)
ANT. SPEED UNDER 38 P7301A-30 (938)
ANT. SPEED OVER 39 P7301A-29 (937)
PHASE COHER UNDER 40 P7301A-39 (967)
+15VDC 41 J101-6 (2)
CARD 200
LIMIT DETECTOR
J101
GND 1 (0)
+20VDC 2
3
4
5.7VDC 5 Q7301-8 (912)
+15VDC 6 J201-41 (2)
+15VDC 7 J301-41 (2)
+15VDC 8
+15VDC 9 P7301B-3 (2)
-15VDC 10 P7301B-2 (5)
-15VDC 11 J201-12 (5)
-15VDC 12 J301-12 (5)
-15VDC 13
15V400HZ 14 T7301-5 (901)
15V400HZ 15 T7301-7 (903)
-20VDC 16 J301-10 (7)
CENTER TAP 17 T7301-6 (902)
CARD 100
POWER SUPPLY REGULATOR
T7301
115VAC HOT 1 P7301B-19 (1)
115VAC RTN 2 P7301B-31 (91)
15VAC 5 J101-14 (901)
CENTERTAP 6 J101-17 (902)
15VAC 7 J101-15 (903)
5VAC 8 (904)
5VAC 9 (905)
CR7301
- 1
+ 2
AC 3
AC 4
(0)
(906)
C7301
+ 1 - 2
J101-5
(912)
Q7301
C B E
(4) +5VDC J201-27



BOTTOM CONN P7301B

		1	GND
(5)	J101-10	2	SAU -15VDC
(2)	J101-9	3	SAU +15VDC
		4	SPARE 1
		5	GND
(968)	J301-8	6	BEAR NG DEV
(978)	J301-29	7	RANGE REPLY SCOPE SYNC
		8	GND
		9	SPARE 2
(9012)	J301-31	10	ARG SCOPE SYNC
(9013)	J301-22	11	MRG SCOPE SYNC
(9014)	J301-24	12	RANGE INTERROGATE SCOPE SYNC
		13	GND
		14	SPARE 3
		15	GND
		16	GND
		17	GND
		18	GND
(1)	T7301-1	19	115V 400HZ
		20	SPARE 4
(9015)	J301-28	21	0=RANGE GATE
(9016)	J301-21	22	0=SUPPRESS
(9017)	J301-25	23	±2°GATE
(9018)	J301-20	24	ZERO±2°GATE
(4)	J301-27	25	SAU +5VDC
(9023)	J301-4	26	1=VALID
(9024)	J301-5	27	TACAN AGC
(9025)	J301-3	28	%RANGE REPLIES
		29	GND
(9026)	J301-35	30	0±20° GATE
(91)	T7301-2	31	400HZ RTN
(9027)	J201-5	32	MRG SIZE OVER
(9028)	J201-2	33	MRG SIZE UNDER
(9035)	J201-4	34	ARG SIZE OVER
(9036)	J201-3	35	ARG SIZE UNDER
(9037)	J201-7	36	ARG COUNT UNDER
(9038)	J301-2	37	AGC BUFFERED
		38	SHIELD GND
(9067)	J301-6	39	PHASE COHER
		1B COAX	

△ PINS INDICATED ARE SHORTED TO GROUND IN CONNECTOR

TOP CONN P7301A

		1	SPARE 8
		2	SPARE 9
		3	
		4	
		5	
(905C)	J201-24	6	PULSE PAIRS BUFFERED
(904B)	J201-31	7	1=DME
		8	
(9047)	J201-33	9	SQUITTER RATE ANALOG
(9046)	J201-34	10	ANT. SPEED
		11	
		12	
(913)	J301-40	13	ARG CK
(914)	J301-36	14	D.8B
(915)	J301-37	15	D.4C
(916)	J301-38	16	D.2B
(918)	J301-34	17	MRG CK
(92)	J301-19	18	BEARING DEVIATION VOLTAGE
		19	
(924)	J301-13	20	D2B
(925)	J301-9	21	D1A
		22	
		23	
(90)	J201-8	24	1=Y MODE
(928)	J301-26	25	D10
(934)	J301-11	26	D8D
(935)	J301-15	27	D4C
(936)	J201-22	28	ARG EV
(937)	J201-39	29	ANT. SPEED-OVER
(938)	J201-38	30	ANT. SPEED UNDER
(945)	J201-37	31	SQUITTER RATE OVER
(946)	J301-16	32	155 BUFFERED
(947)	J301-17	33	0.2° CLOCK
(948)	J301-7	34	1=TO
(956)	J301-30	35	D20
(957)	J301-32	36	1=MANUAL
(958)	J201-36	37	SQUITTER RATE UNDER
(962)	J201-35	38	PHASE COHER OVER
(967)	J201-40	39	PHASE COHER UNDER
		1A COAX	

NOTES: UNLESS OTHERWISE INDICATED

1. NUMBERS IN PARENTHESES INDICATE COLOR CODE FOR WIRES I.E.: (912) — WHITE/BROWN// RED.
2. WIRES TO BE 24AWG, TEFLON INSULATION.

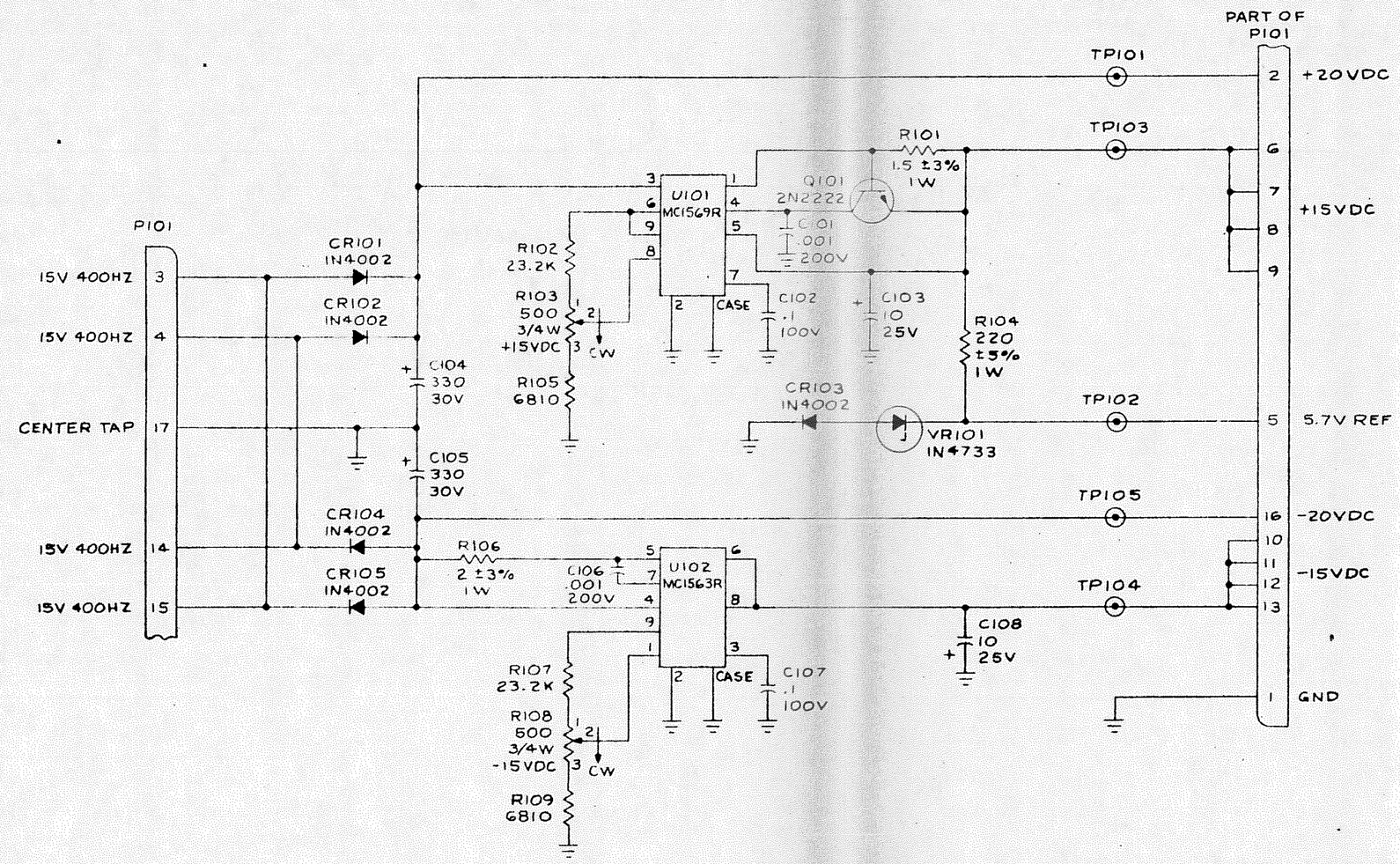
Figure 922. Signal Analyzer Unit Interconnecting Wiring Diagram

7124-0140	SAWS	J	12115	7124-1005

SIERRA

INTERCONNECTION WIRING DIAGRAM, SIGNAL ANALYZER

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	–	DWG 7124-1122 REV-DTD 27SEP72 REDRAWN WITHOUT CHANGE	14 OCT 72	



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES IN OHMS, ±1%, 1/8 W.
2. ALL CAPACITANCE VALUES IN MICROFARADS.

Figure 923. SAU Power Supply Regulator A100 Schematic Diagram

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001	7109-3020	

HOLE TOLERANCES — APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ±.03 | .XXX ±.010 | ANGLES ±0°30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

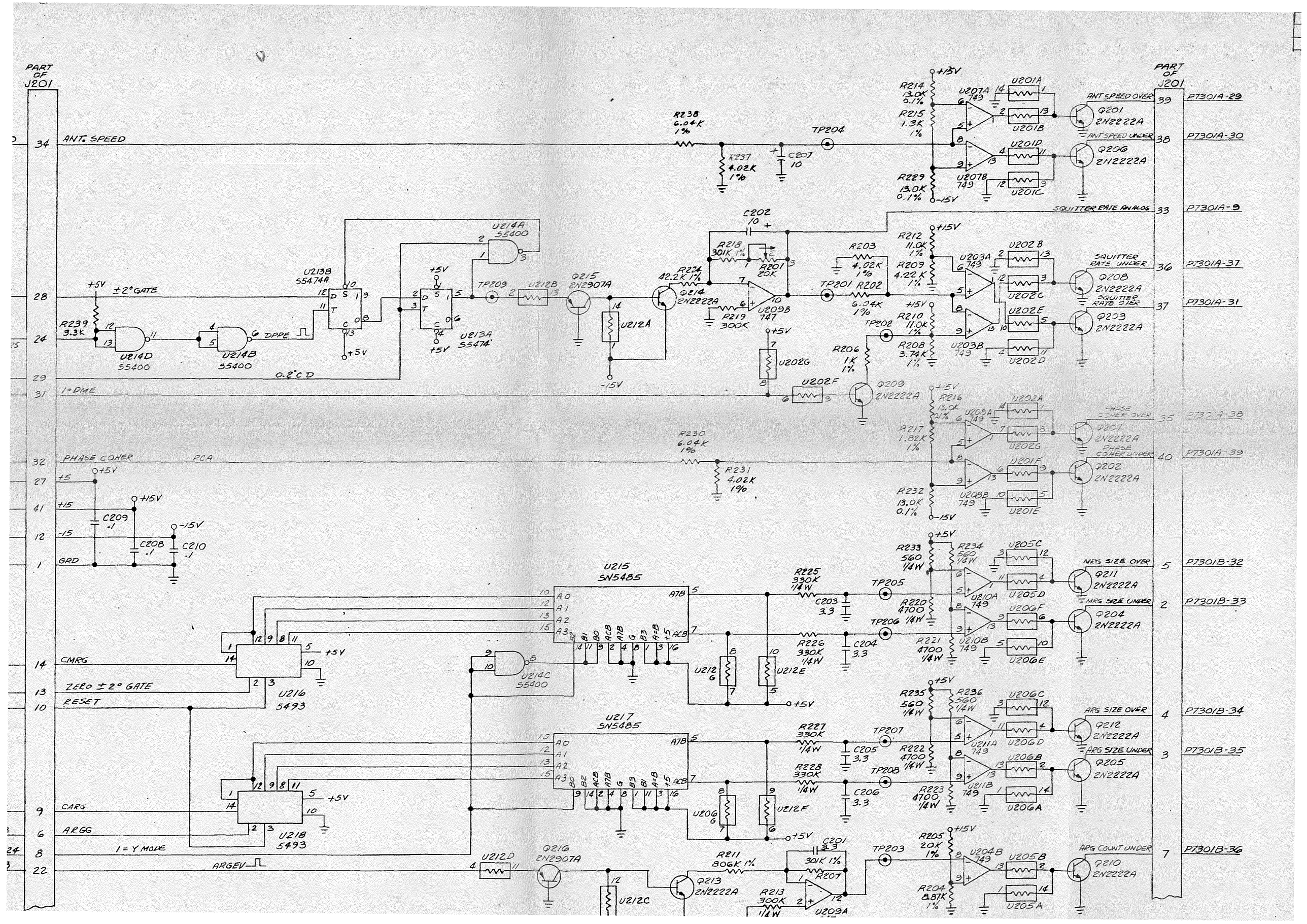
DRAWN W. Smith 4 DEC 72
DESIGNED
CHECK 5 DEC 72
ENGR R. Wilson 8 DEC 72
APPD 14 DEC 72
CONT NO. 7124-008 16 OCT 72
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

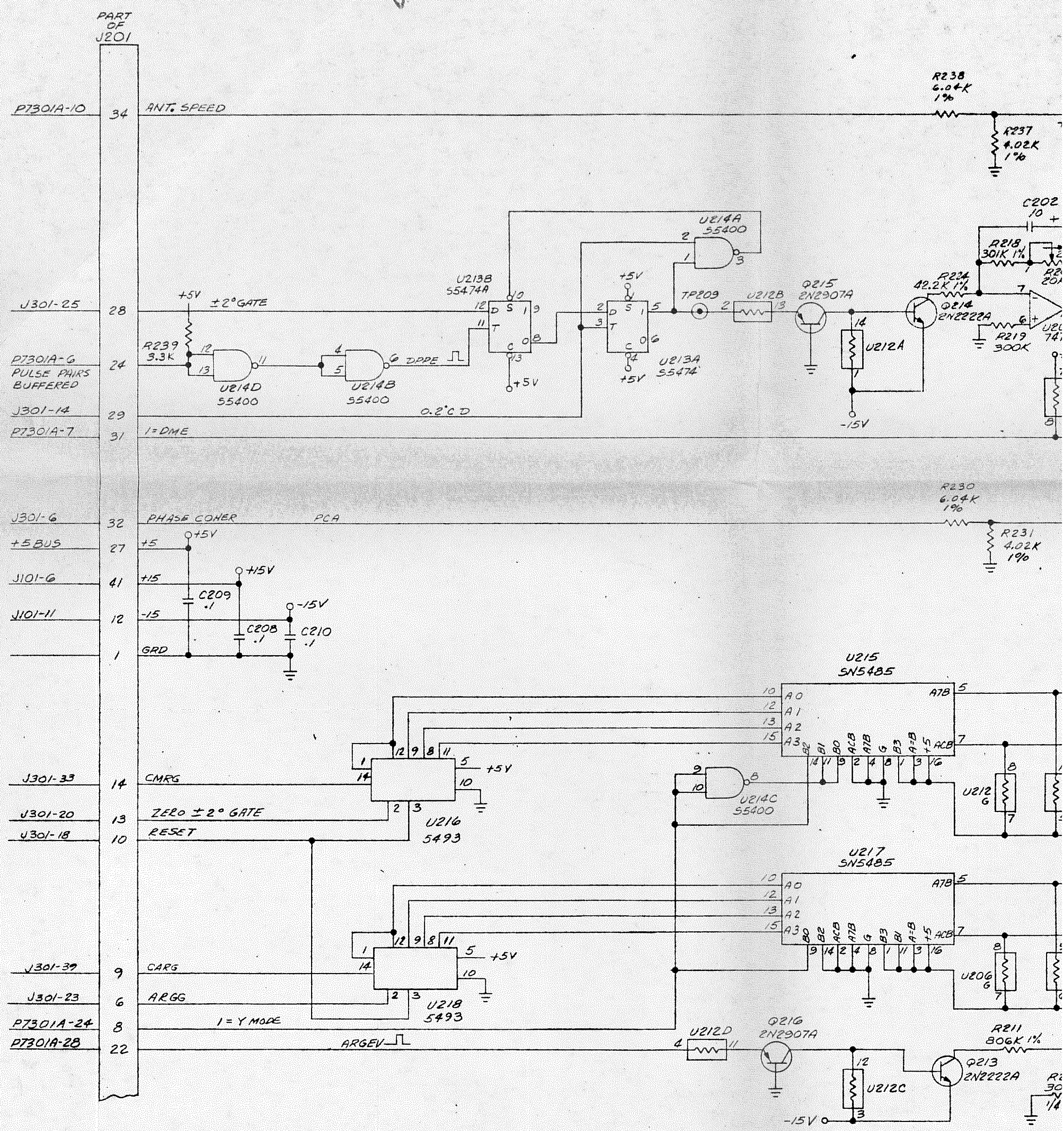
SIERRA ELECTRONICS DIVISION CORP.
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, POWER SUPPLY REGULATOR

SIZE D | CODE IDENT NO. 12115 | 7124-1122

SCALE NONE | SHEET 1 OF 1


PART OF J201
34 ANT. SPEED
28 ±2° GATE
24 0.2°C D
29
31 1=DME
32 PHASE COHER PCA
27 +5
41 +15
12 -15
1 GRD
14 CMRG
13 ZERO ±2° GATE
10 RESET
9 CARG
6 ARGG
8 1 = Y MODE
22 ARGEV
R238 6.04K 1%
R237 4.02K 1%
C207 10
TP204
R214 13.0K 0.1%
R215 1.3K 1%
R229 13.0K 0.1%
U207A 749
U207B 749
U201A
U201B
U201D
U201C
ANT SPEED OVER
ANT SPEED UNDER
Q201 2N2222A
Q206 2N2222A
SQUITTER RATE ANALOG
C202 10
R218 301K 1%
R201 20K
R224 42.2K 1%
Q214 2N2222A
U209B 747
R219 300K
R203 4.02K 1%
TP201
R202 6.04K 1%
R212 11.0K 1%
R209 4.22K 1%
U203A 749
U202B
U202C
U202E
U202D
U203B 749
SQUITTER RATE UNDER
SQUITTER RATE OVER
Q208 2N2222A
Q203 2N2222A
TP202
R210 11.0K 1%
R208 3.74K 1%
R206 1K 1%
U202G
U202F
Q209 2N2222A
R216 13.0K 1%
R217 1.82K 1%
U208A 749
U202A
U202G
U201F
U208B 749
U201E
PHASE COHER OVER
PHASE COHER UNDER
Q207 2N2222A
Q202 2N2222A
R230 6.04K 1%
R231 4.02K 1%
R232 13.0K 0.1%
C209 .1
C208 .1
C210 .1
U213B 55474A
U214A 55400
U214D 55400
U214B 55400
U213A 55474
TP209
U212B
Q215 2N2907A
U212A
U202G
R233 560 1/4W
R234 560 1/4W
U205C
U205D
U206F
U206E
U210A 749
U210B 749
R220 4700 1/4W
R221 4700 1/4W
MRG SIZE OVER
MRG SIZE UNDER
Q211 2N2222A
Q204 2N2222A
R235 560 1/4W
R236 560 1/4W
U206C
U206D
U206B
U206A
U211A 749
U211B 749
R222 4700 1/4W
R223 4700 1/4W
ARG SIZE OVER
ARG SIZE UNDER
Q212 2N2222A
Q205 2N2222A
U215 SN5485
U216 5493
U217 SN5485
U218 5493
U214C 55400
U212G
U212E
U212F
U206G
R225 330K 1/4W
R226 330K 1/4W
R227 330K 1/4W
R228 330K 1/4W
C203 3.3
C204 3.3
C205 3.3
C206 3.3
TP205
TP206
TP207
TP208
U212D
Q216 2N2907A
U212C
Q213 2N2222A
R211 806K 1%
R213 300K 1/4W
C201 33
301K 1%
R207
U209A
TP203
R205 20K 1%
R204 8.87K 1%
U204B 749
U205B
U205A
ARG COUNT UNDER
Q210 2N2222A
PART OF J201
39 P7301A-29
38 P7301A-30
33 P7301A-9
36 P7301A-37
37 P7301A-31
35 P7301A-38
40 P7301A-39
5 P7301B-32
2 P7301B-33
4 P7301B-34
3 P7301B-35
7 P7301B-36



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8 W.
2. ALL CAPACITANCE VALUES ARE MICROFARADS.
3. ALL INTEGRATED CIRCUITS HAVE +5V ON PIN 14 AND GROUND ON PIN 7
4. INTEGRATED CIRCUIT UGW7747312 HAS -15V ON PIN 4 AND +15V ON PIN 9 AND PIN 13, INTEGRATED CIRCUIT UGW7749312 HAS -15V ON PIN 7 AND +15V ON PIN 4.

	B	INC ECN 7124-037	20JAN73	
	C	INC ECN 7124-044	26APR73	
	D	INC ECN 7124-058	10APR73	

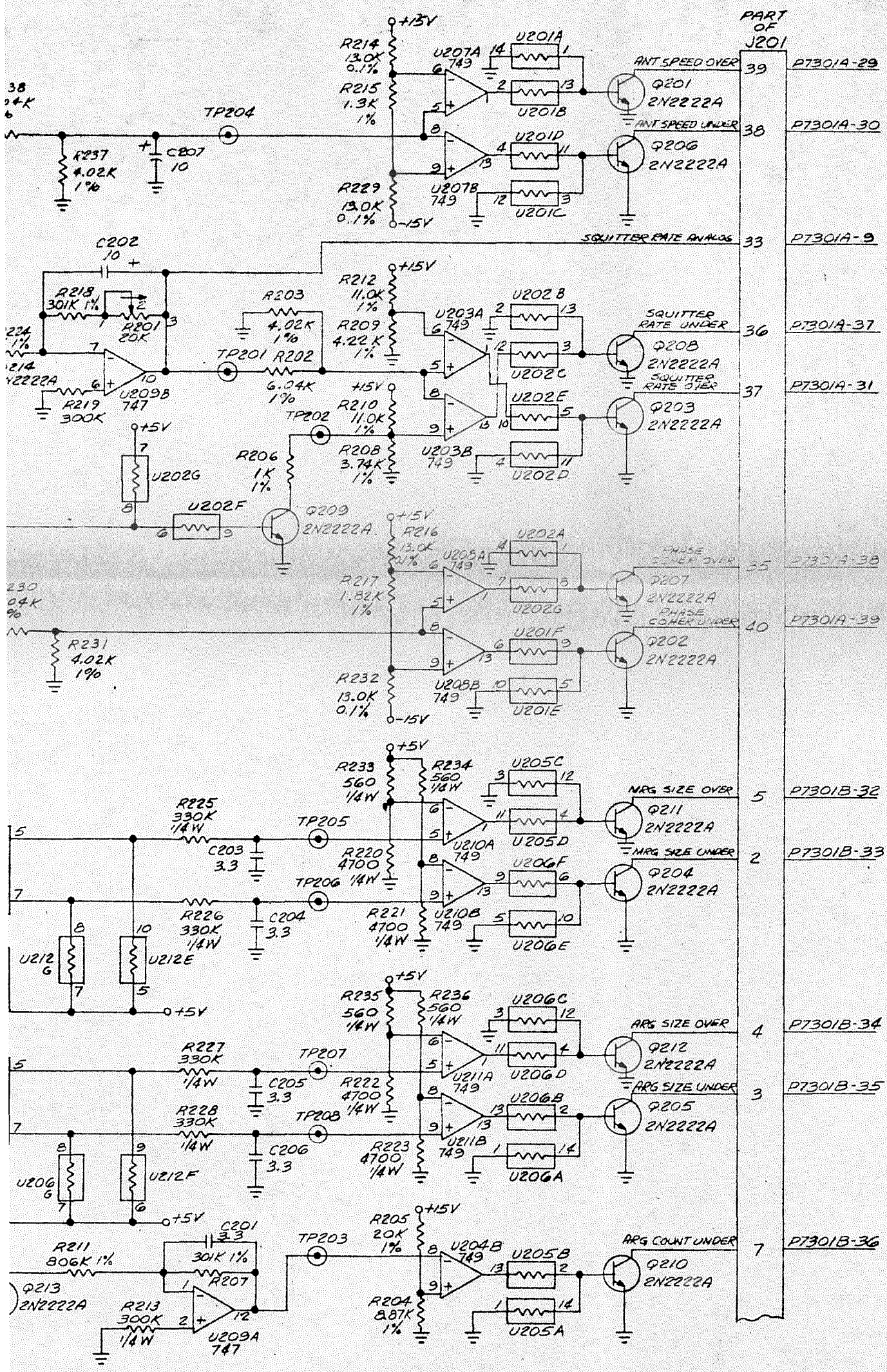


Figure 924. Limit Detector A200 (7124-1110-1)
Schematic Diagram

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001		

HOLE TOLERANCES — APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

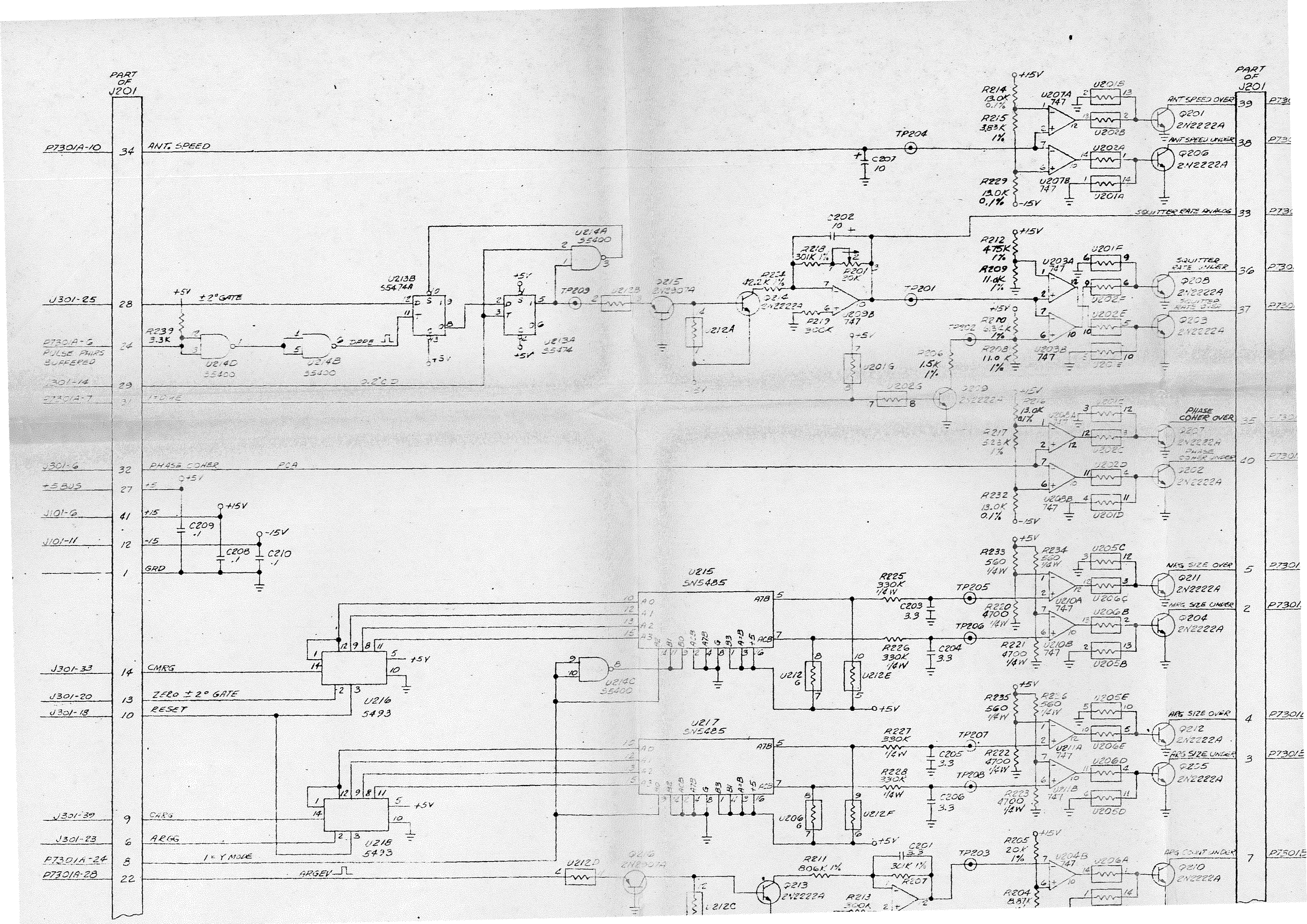
DRAWN 21 OCT 72
DESIGNER
CHECK
ENGR
APPD 2 JAN 73
CONT NO.
7124-023 2 JAN 73
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

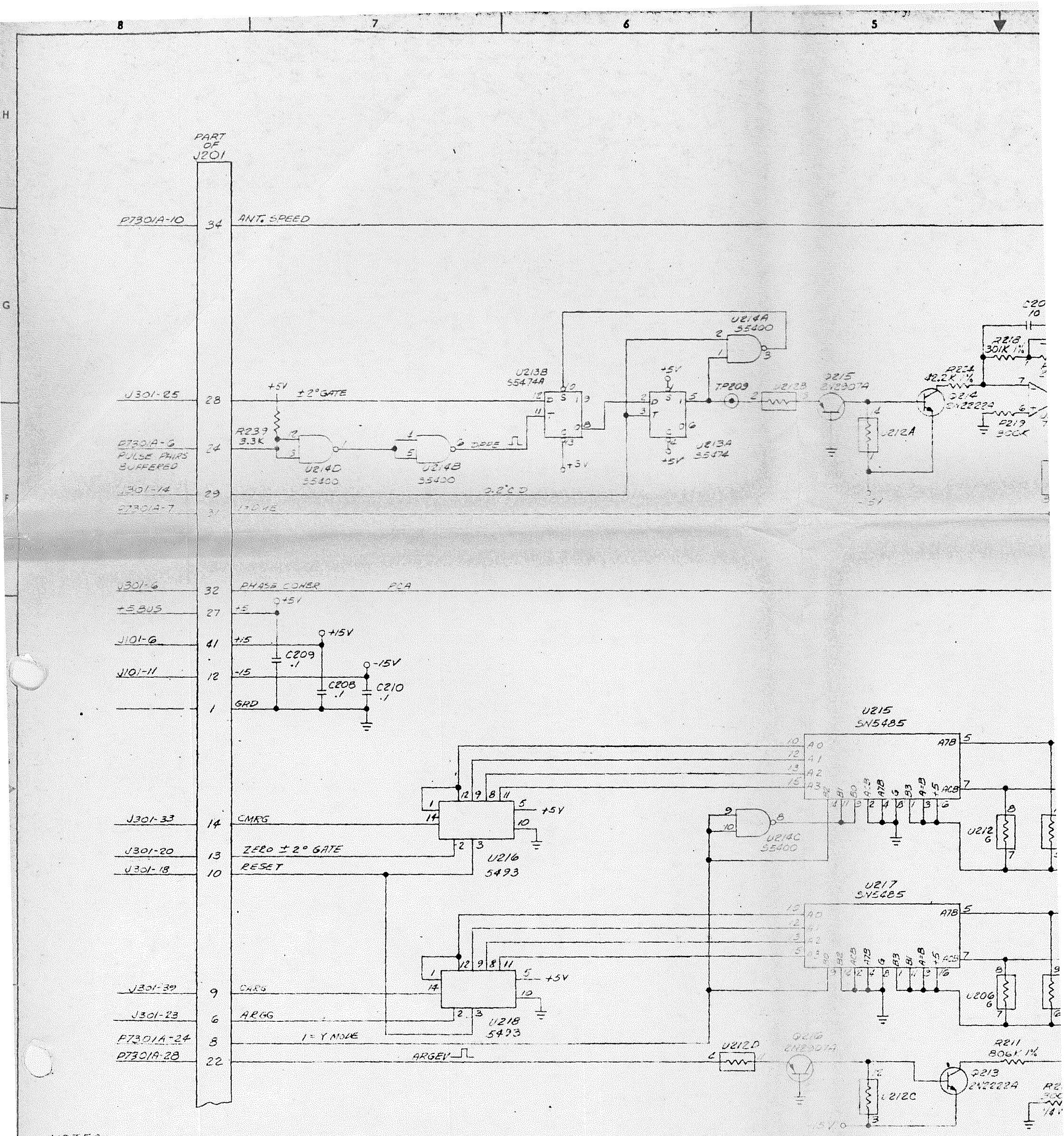
SIERRA RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, LIMIT DETECTOR

SIZE E | CODE IDENT NO. 12115 | 7124-1112

SCALE | SHEET 1 OF 1


PART OF J201
P7301A-10
34
ANT. SPEED
TP204
C207 10
R214 13.0K 0.1%
R215 3.83K 1%
R229 13.0K 0.1%
U207A 747
U207B 747
U201B
U202B
U202A
U201A
ANT SPEED OVER
Q201 2N2222A
ANT SPEED UNDER
Q206 2N2222A
SQUITTER RATE ANALOG
J301-25
28
±2° GATE
+5V
R239 3.3K
U214D 55400
U214B 55400
DPPE
0.2°C D
U213B 55474A
U214A 55400
TP209
U213A 55474
U212B
Q215 2N2907A
U212A
R224 42.2K 1%
Q214 2N2222A
R218 301K 1%
R201 20K
C202 10
R219 300K
U209B 747
TP201
U201G
U202G
R206 1.5K 1%
Q209 2N2222A
R212 4.75K 1%
R209 11.0K 1%
U203A 747
U201F
U202F
U202E
Q208 2N2222A
SQUITTER RATE OVER
Q203 2N2222A
R210 6.36K 1%
R208 11.0K 1%
U203B 747
U201E
P7301A-6
PULSE PHASE BUFFERED
24
J301-14
29
P7301A-7
31
1=DPPE
J301-6
32
PHASE COHER
PCA
+5 BUS
27
J101-6
41
J101-11
12
GRD
1
C209 .1
C208 .1
C210 .1
-15V
R216 13.0K 0.1%
R217 5.23K 1%
U208A 747
U202C
U202D
U208B 747
U201C
U201D
PHASE COHER OVER
Q207 2N2222A
PHASE COHER UNDER
Q202 2N2222A
R232 13.0K 0.1%
U215 SN5485
U216 5493
U217 SN5485
U218 5493
U214C 55400
CMRG
J301-33
14
ZERO ±2° GATE
J301-20
13
RESET
J301-18
10
CARG
J301-39
9
ARGG
J301-23
6
1=Y MODE
P7301A-24
8
ARGEV
P7301A-28
22
U212D
Q210 2N2907A
U212C
Q213 2N2222A
R211 806K 1%
R213 300K
C201 3.3
301K 1%
R207
TP203
R225 330K 1/4W
C203 3.3
TP205
R226 330K 1/4W
C204 3.3
TP206
U212G
U212E
R227 330K 1/4W
C205 3.3
TP207
R228 330K 1/4W
C206 3.3
TP208
U206G
U212F
R233 560 1/4W
R234 560 1/4W
R220 4700 1/4W
R221 4700 1/4W
U210A 747
U210B 747
U205C
U206C
U206B
U205B
NRG SIZE OVER
Q211 2N2222A
NRG SIZE UNDER
Q204 2N2222A
R235 560 1/4W
R236 560 1/4W
R222 4700 1/4W
R223 4700 1/4W
U211A 747
U211B 747
U205E
U206E
U206D
U205D
ARG SIZE OVER
Q212 2N2222A
ARG SIZE UNDER
Q205 2N2222A
R205 20K 1%
R204 8.81K
U204B 747
U206A
ARG COUNT UNDER
Q210 2N2222A
P7301A-39
P7301A-23
P7301A-20
P7301A-18
P7301A-33
P7301A-6
P7301A-7
P7301A-10



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8 W.
2. ALL CAPACITANCE VALUES ARE MICROFARADS.
3. ALL INTEGRATED CIRCUITS HAVE +5V ON PIN 14 AND GROUND ON PIN 7
4. INTEGRATED CIRCUIT U6W7747312 HAS -15V ON PIN 4 AND +15V ON PIN 9 AND PIN 13,

ZONE	LTR	DESCRIPTION	DATE	APPROVED

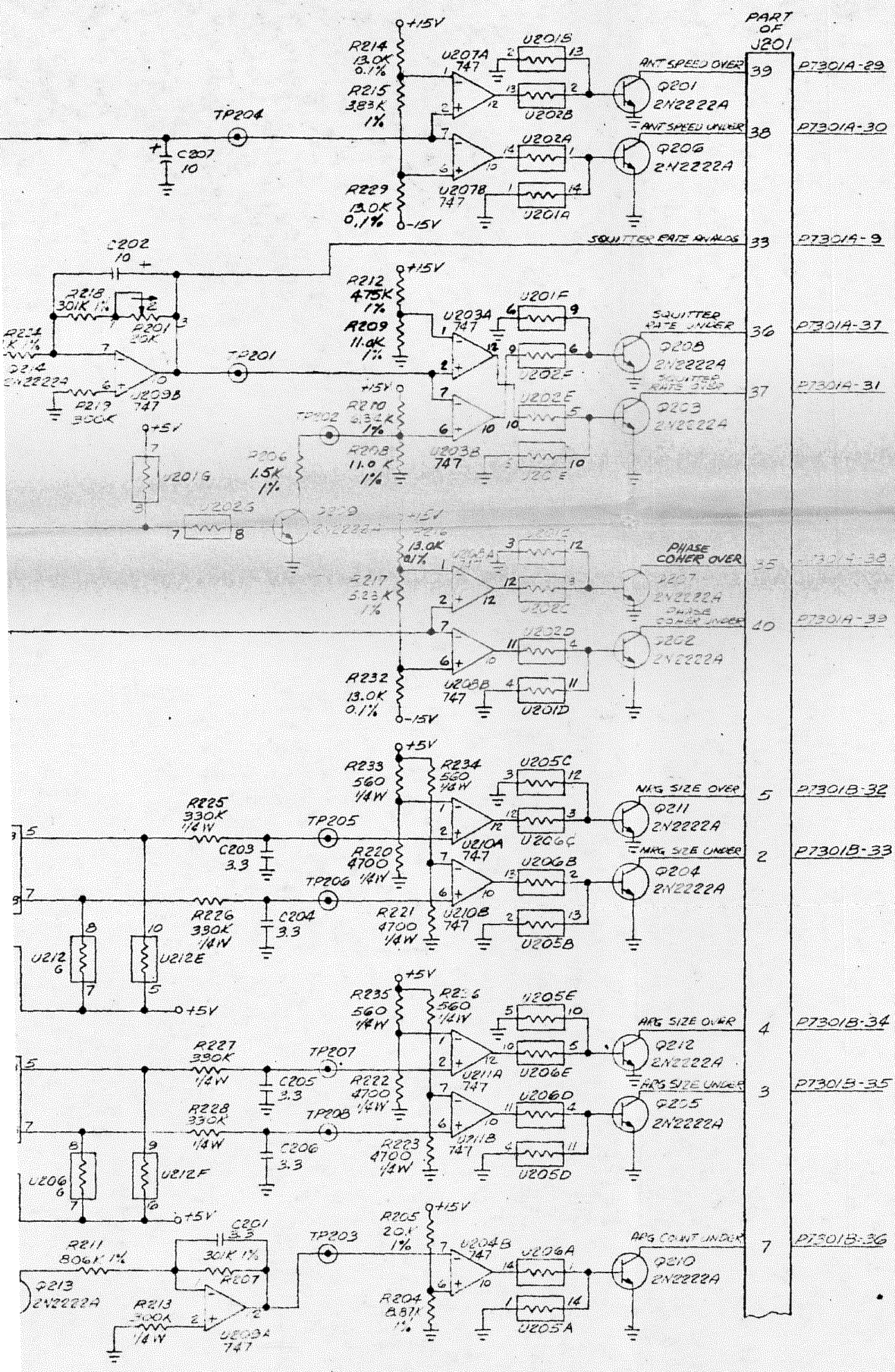


Figure 925. Limit Detector A200 (7124-1127-2) Schematic Diagram

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V — VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F FEET I — INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.001 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ±.03 | .XXX ±.010 | ANGLES ±0°30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

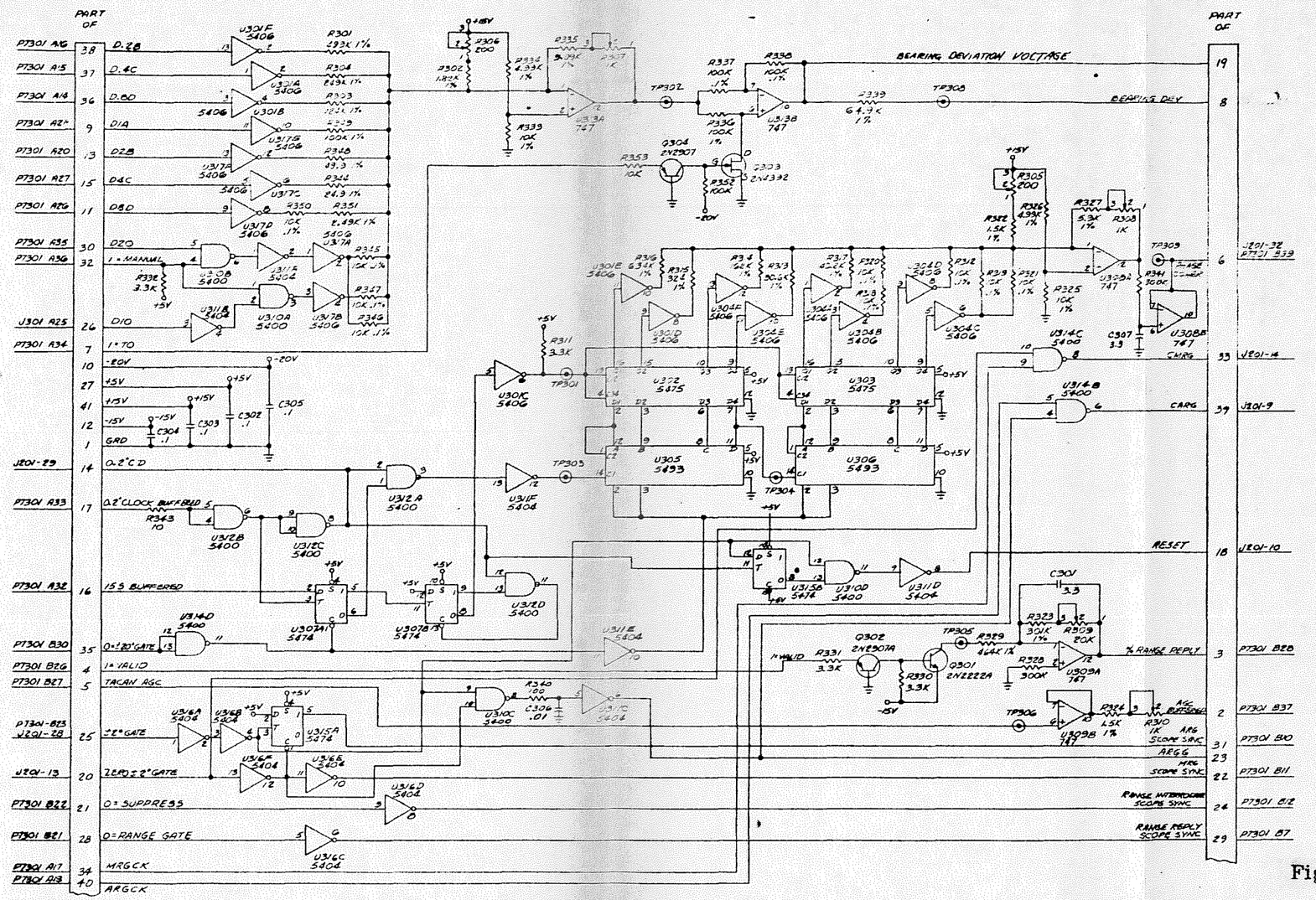
DRAWN
DESIGNER
CHECK
ENGR
APPR
CONT NO.
ENGRG RELEASE NOTICE

SIERRA RESEARCH CORP.
POST OFFICE BOX 227 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, LIMIT DETECTOR

SIZE	CODE IDENT NO.	
E	12115	7124-1127

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	INC ECN 7124-029		
	B	INC ECN 7124-027		
	C	INC ECN 7124-041		



NOTES: UNLESS OTHERWISE SPECIFIED

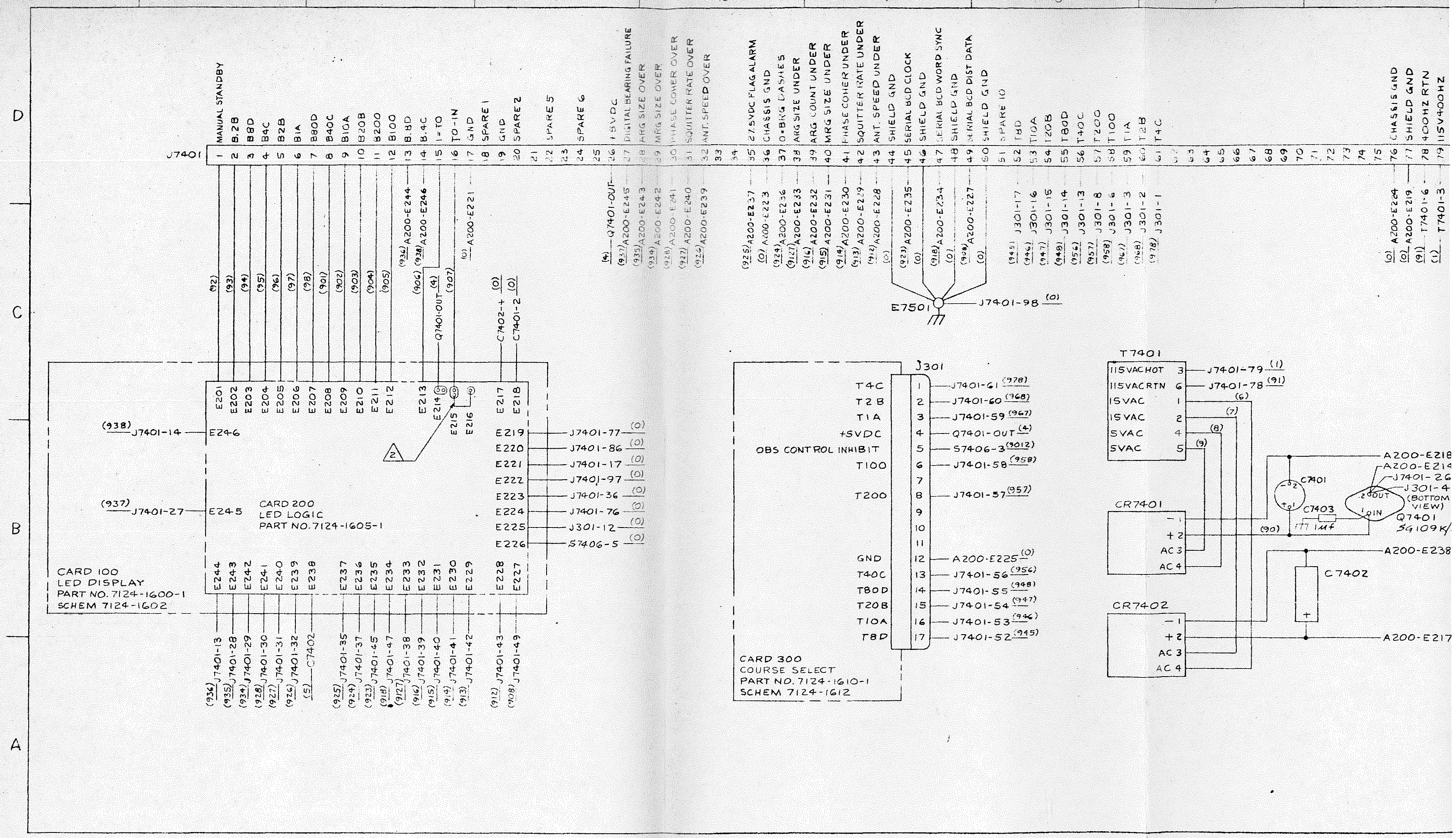
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL INTEGRATED CIRCUITS HAVE +5V ON PIN 14 AND GROUND ON PIN 7.
4. ALL 747 INTEGRATED CIRCUITS HAVE -15V ON PIN 4 AND +15V ON PIN 9 AND PIN 13.
5. ALL 5475 INTEGRATED CIRCUITS HAVE +5V ON PIN 5 AND GROUND ON PIN 12, ALL 5493 INTEGRATED CIRCUITS HAVE +5V ON PIN 5 AND GROUND ON PIN 10.

Figure 926. Signal Processor A300 Logic Diagram

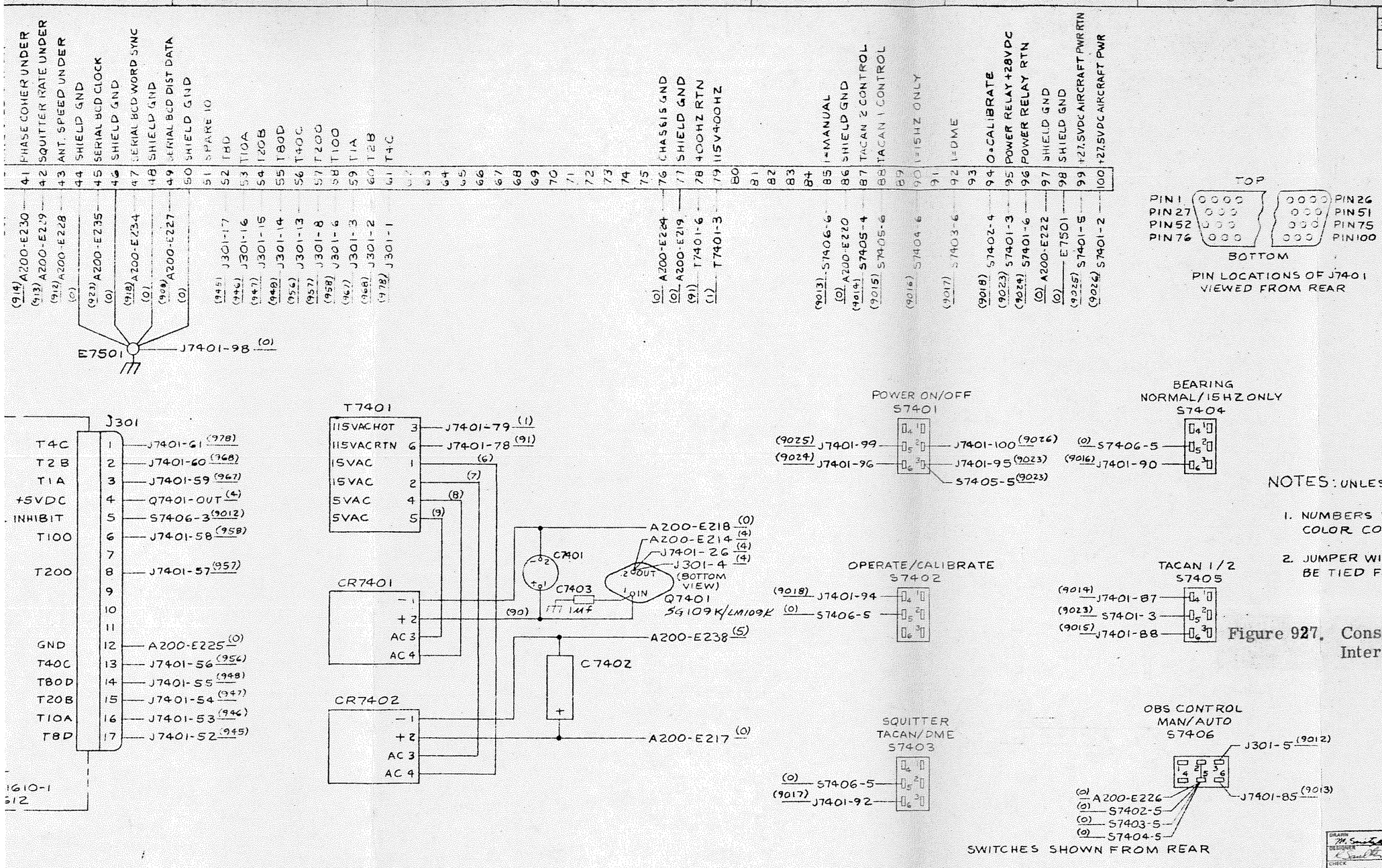
SIERRA

LOGIC DIAGRAM, SIGNAL PROCESSOR

E 12115 7124-1107


J7401
MANUAL STANDBY
B.2B
B8D
B4C
B2B
B1A
B80D
B40C
B10A
B20B
B200
B100
B.8D
B.4C
TO-IN
GND
SPARE 1
GND
SPARE 2
SPARE 5
SPARE 6
+5VDC
DIGITAL BEARING FAILURE
ARG SIZE OVER
MRG SIZE OVER
PHASE COHER OVER
SQUITTER RATE OVER
ANT. SPEED OVER
+27.5VDC FLAG ALARM
CHASSIS GND
O-BRG CASHES
ARG SIZE UNDER
ARG COUNT UNDER
MRG SIZE UNDER
PHASE COHER UNDER
SQUITTER RATE UNDER
ANT. SPEED UNDER
SHIELD GND
SERIAL BCD CLOCK
SHIELD GND
SERIAL BCD WORD SYNC
SHIELD GND
SERIAL BCD DIST DATA
SHIELD GND
SPARE 10
T8D
T10A
T20B
T80D
T40C
T200
T100
T1A
T2B
T4C
CHASSIS GND
SHIELD GND
400HZ RTN
115V400HZ
Q7401-OUT
A200-E245
A200-E243
A200-E242
A200-E241
A200-E240
A200-E239
A200-E237
A200-E223
A200-E236
A200-E233
A200-E232
A200-E231
A200-E230
A200-E229
A200-E228
A200-E235
A200-E234
A200-E227
J301-17
J301-16
J301-15
J301-14
J301-13
J301-8
J301-6
J301-3
J301-2
J301-1
A200-E244
A200-E246
A200-E221
C7402-+
C7401-2
E7501
J7401-98
CARD 200
LED LOGIC
PART NO. 7124-1605-1
J7401-14
E246
J7401-27
E245
E219 J7401-77
E220 J7401-86
E221 J7401-17
E222 J7401-97
E223 J7401-36
E224 J7401-76
E225 J301-12
E226 S7406-5
CARD 100
LED DISPLAY
PART NO. 7124-1600-1
SCHEM 7124-1602
J7401-13
J7401-28
J7401-29
J7401-30
J7401-31
J7401-32
C7402
J7401-35
J7401-37
J7401-45
J7401-47
J7401-38
J7401-39
J7401-40
J7401-41
J7401-42
J7401-43
J7401-49
J301
T4C
T2B
T1A
+5VDC
OBS CONTROL INHIBIT
T100
T200
GND
T40C
T80D
T20B
T10A
T8D
J7401-61
J7401-60
J7401-59
Q7401-OUT
S7406-3
J7401-58
J7401-57
A200-E225
J7401-56
J7401-55
J7401-54
J7401-53
J7401-52
CARD 300
COURSE SELECT
PART NO. 7124-1610-1
SCHEM 7124-1612
T7401
115VAC HOT
115VAC RTN
15VAC
15VAC
5VAC
5VAC
J7401-79
J7401-78
CR7401
CR7402
AC 3
AC 4
C7401
C7403
1uf
OUT
IN
Q7401
SG109K
A200-E218
A200-E214
J7401-26
J301-4
(BOTTOM VIEW)
A200-E238
C7402
A200-E217

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INC ECN 7124-026 RES	16 Jan 73	
	B	INC ECN 7124-040 RES	[illegible] 73	



NOTES: UNLESS OTHERWISE INDICATED

1. NUMBERS IN BRACKETS INDICATE WIRE COLOR CODE. I.E: (912) WHT/BRN/RED
2. JUMPER WIRE FROM E215 TO E216 MAY BE TIED FROM E215 TO E214.

Figure 927. Console Display and Control Panel Unit Interconnecting Wiring Diagram

7124-0130	SANS
NEXT ASSY	USED ON
APPLICATION	

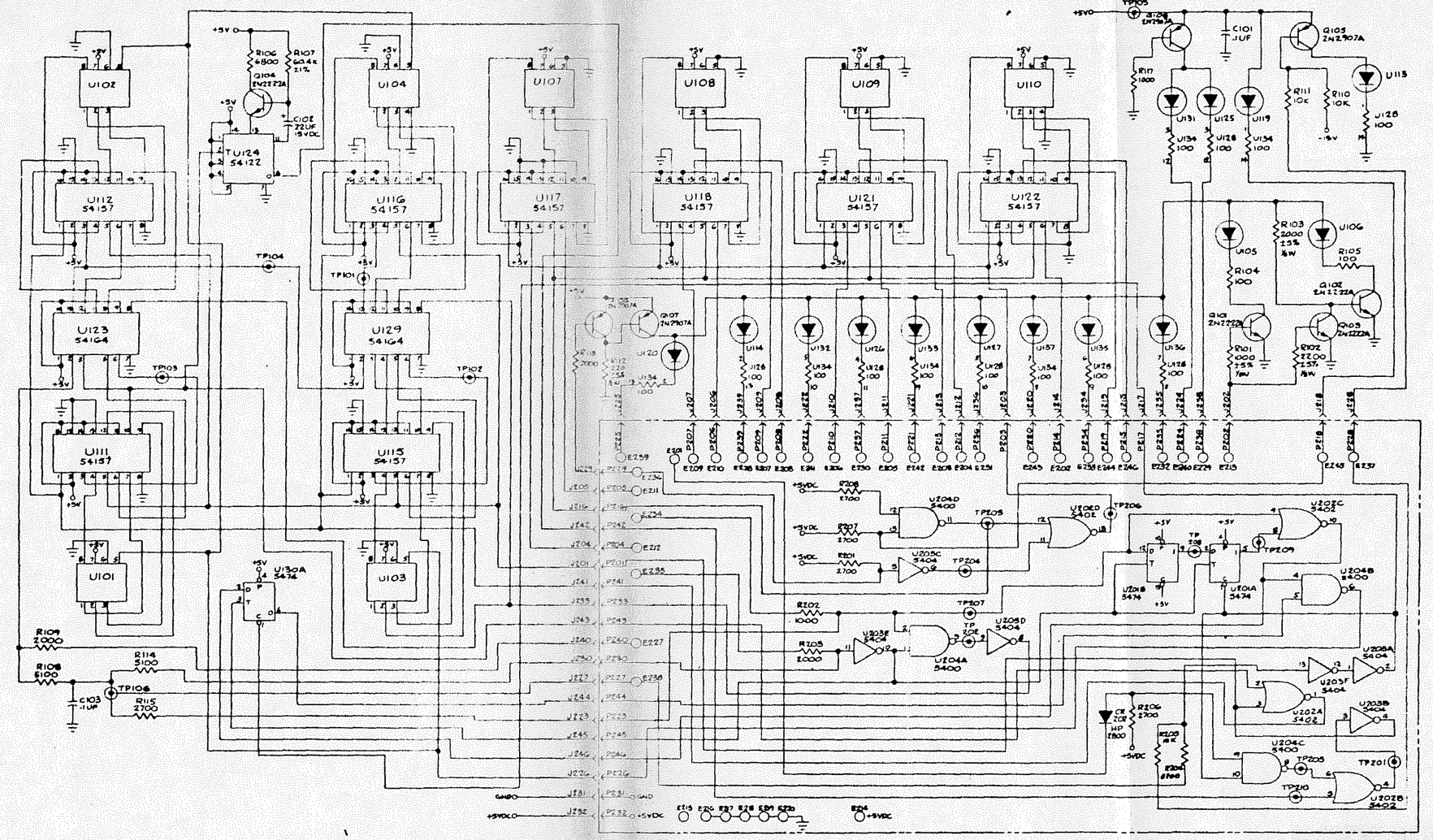
DRAWN 30 OCT 72
DESIGNED 6 DEC 72
CHECK
ENGR 5 Dec 72
APPD 19 DEC 72
CONT NO. 7124-020 19 DEC 72
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

SIERRA RESEARCH CORP. ELECTRONICS
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

INTERCONNECTION WIRING DIAGRAM, PANEL UNIT, CONSOLE DISPLAY AND CONTROL

SIZE J | CODE IDENT NO. 12115 | 7124-1504
SCALE NONE | SHEET 1 OF 1

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	INC ECN 7124-024		
	B	INC ECN 7124-037		



NOTES: UNLESS OTHERWISE INDICATED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL 5400, 5402, 5404 AND 5474 INTEGRATED CIRCUITS HAVE +5V ON PIN 14 AND GROUND ON PIN 7.

SIGNAL INPUTS		SIGNAL INPUTS	
E NO.	SIGNAL NAME	E NO.	SIGNAL NAME
E201	MANUAL STANDBY	E238	AN SPEED UNDER
E202	B.E.B	E239	SCATTER RATE UNDER
E203	B&D	E240	PHASE COHER UNDER
E204	B&C	E241	MAJ. SIZE UNDER
E205	B2A	E242	MAJ. COUNT UNDER
E206	B1A	E243	MEG SIZE UNDER
E207	B300	E234	SIGNAL BLD WORD SYNC
E208	B&C	E235	SIGNAL BLD CLOCK
E209	B104	E236	BY BEARING DASHES
E210	B2B	E237	ANY VDC FLAG ALARM
E211	B200B	E238	+5V DC
E212	B100A	E239	ANT SPEED OVER
E213	1-TO	E240	SCATTER RATE OVER
E214	+5V	E241	PHASE COHER OVER
E215	TO-IN	E242	MEG SIZE OVER
E216-E220	GND	E243	MEG SIZE OVER
E221-E226		E244	B.E.D
E227	SIGNAL BLD DIST DATA	E245	DISPLAY BEARING FAILURE
		E246	B&C

Figure 928. LED Display Logic Diagram

QTY REQD	ITEM NO.	CODE IDENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION
			PARTS LIST		

REV V - VENDOR ITEM SEE SPEC ON DRAWING CONTROL DWG. X FEET 1 - INCHES ALL NOTE INDICATED

1.000 THRU 3.000	± .005		
.101 THRU 1.000	± .001		
.001 THRU .100	± .0005		
.000 THRU .000	± .0005		
.000 THRU .000	± .0005		
.000 THRU .000	± .0005		
.000 THRU .000	± .0005		
.000 THRU .000	± .0005		
DECIMAL DIM.	TOL BALANCE	FINISH ALL	MATERIAL
HOLE TOLERANCES		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOL BALANCE: .XX ±.010, .XXX ±.005, ANGLES ±1°30'. DIMENSIONS ON DRAWING ARE FINISHED. DO NOT SCALE DRAWING. FINISH.

DRAWN 8-21-73
CHECKED 1-28-73
ENGINEER 1-28-73
MFG 8-21-73
7-16-73

SIERRA RESEARCH CORP. PORT JEFFERSON, NEW YORK 11777

LOGIC DIAGRAM, LED DISPLAY

SIZE E | CODE IDENT NO. 12115 | 7124-1602

SCALE NONE | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

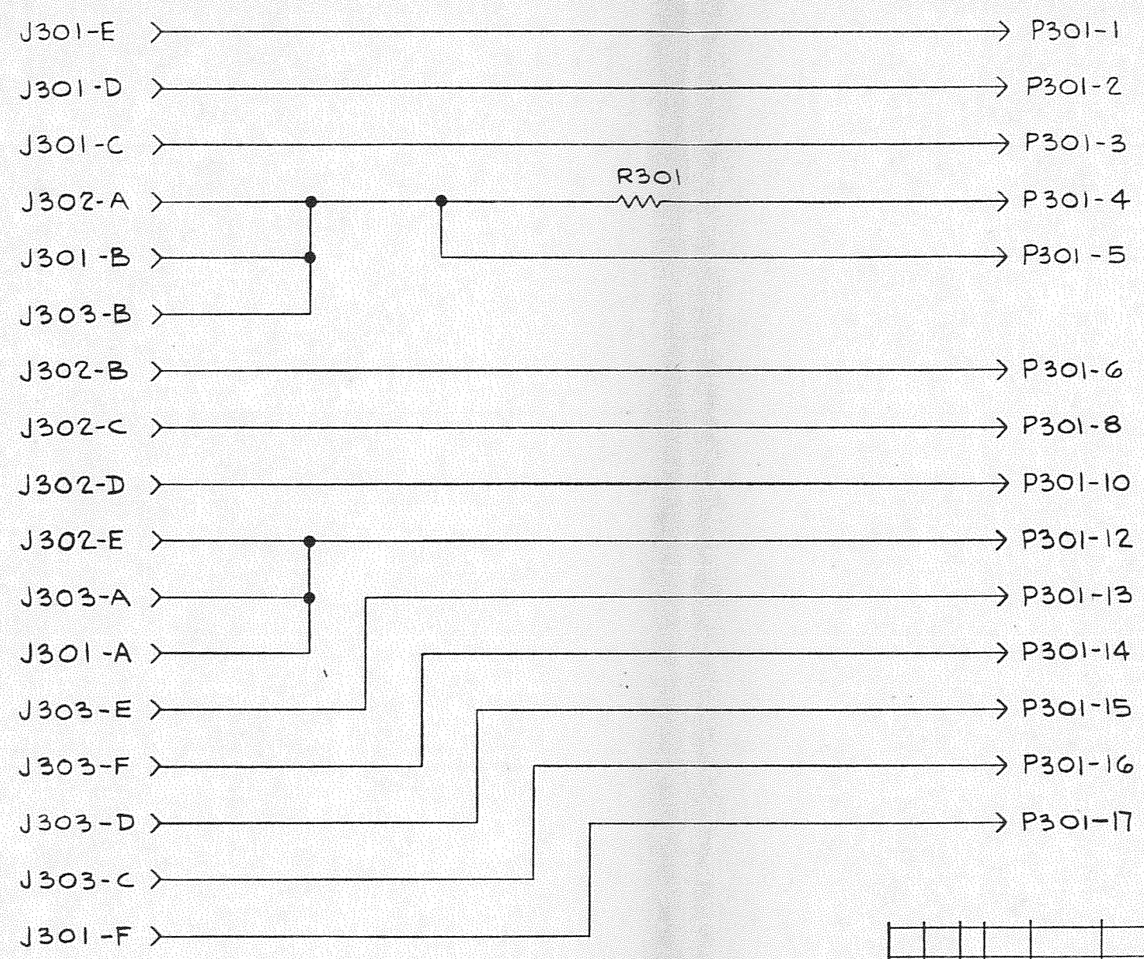


Figure 929. Course Select Schematic Diagram

34-50-00
Page 999/999.0
Oct. 1973

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

1.001 THRU 2.000	+ .012 – .001		
.751 THRU 1.000	+ .010 – .001		
.501 THRU .750	+ .008 – .001		
.251 THRU .500	+ .006 – .001		
.126 THRU .250	+ .005 – .001		
.013 THRU .125	+ .004 – .001	7124-1610	
NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
HOLE TOLERANCES		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: .XX ± .03 | .XXX ± .010 | ANGLES ± 0° 30'
BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER
MATERIAL:
FINISH:

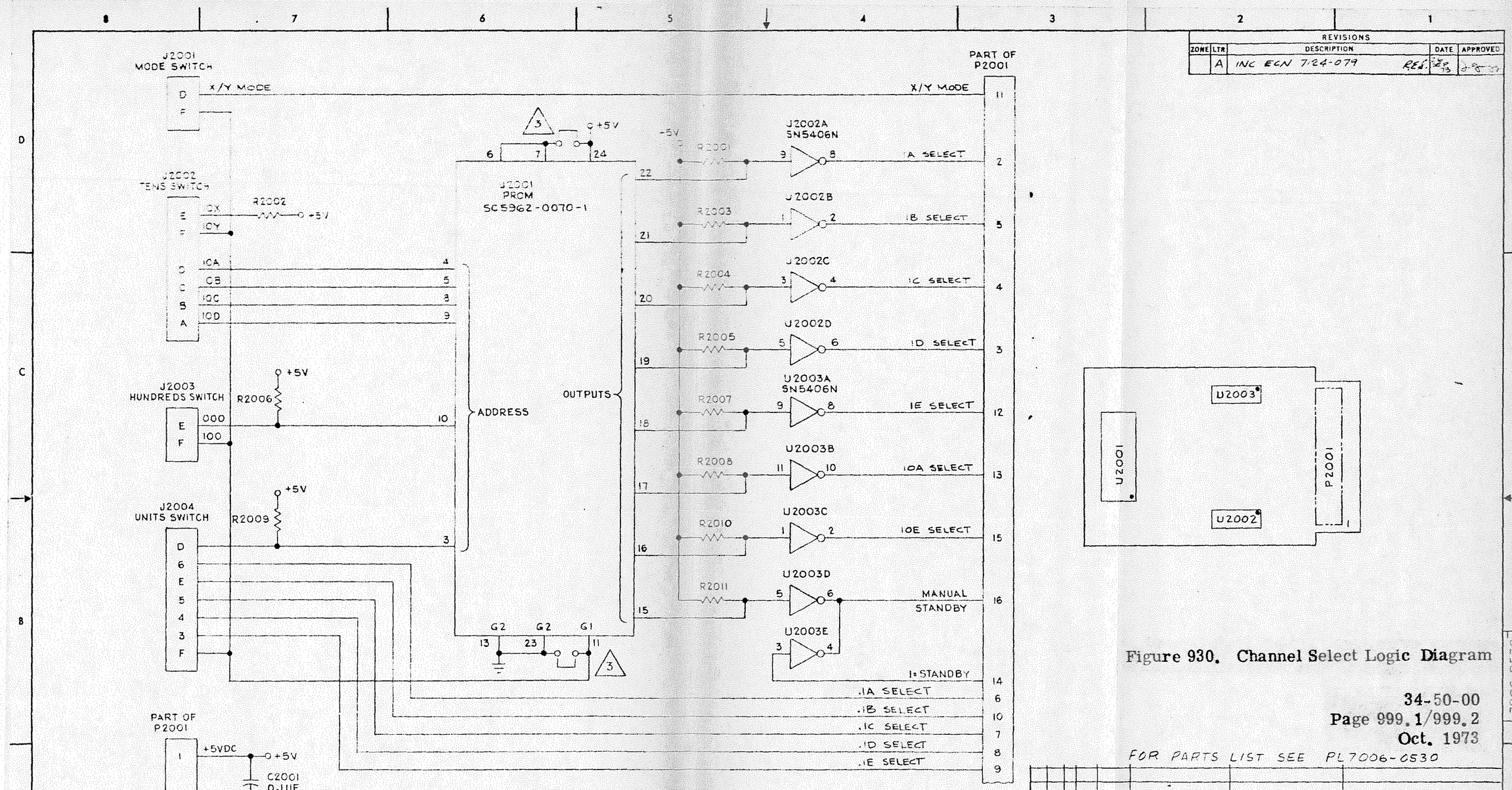
DRAWN R Saulter 2 FEB 73
DESIGNER R Saulter 4 FEB 73
CHECK
ENGR J Keffner 2 Feb 73
APPD
CONT NO.
7124-042
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

ELECTRONICS SIERRA RESEARCH CORP.
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

SCHEMATIC DIAGRAM, COURSE SELECT

SIZE	CODE IDENT NO.	
C	12115	7124-1612

SCALE NONE SHEET 1 OF 1



ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	INC ECN 7124-079 REV.	SEP 73	

Figure 930. Channel Select Logic Diagram

34-50-00
Page 999.1/999.2
Oct. 1973

FOR PARTS LIST SEE PL7006-0530

NOTES: UNLESS OTHERWISE INDICATED.

1. ALL RESISTORS ARE 10K, 1/4 WATT, 5%.
2. ON IC PACKS U2002 AND U2003, PIN 7 IS GND AND PIN 14 IS +5VDC.
3. JUMPER INSTALLED AFTER PROGRAMMING.

QTY REQD	KEY	ITEM NO.	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

PARTS LIST

KEY: V – VENDOR ITEM SEE SPEC OR SOURCE CONTROL DWG F – FEET I – INCHES △ SEE NOTE INDICATED

NOMINAL DIA	TOLERANCE	NEXT ASSY	USED ON
1.901 THRU 2.000	+.012 −.001		
.751 THRU 1.000	+.010 −.001		
.501 THRU .750	+.008 −.001		
.251 THRU .500	+.006 −.001		
.126 THRU .250	+.005 −.001		
.013 THRU .125	+.004 −.001		
HOLE TOLERANCES		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: .XX ±.03, .XXX ±.010, ANGLES ±0°30'. BREAK ALL SHARP EDGES .015R MAXIMUM OR CHAMFER. MATERIAL: FINISH:

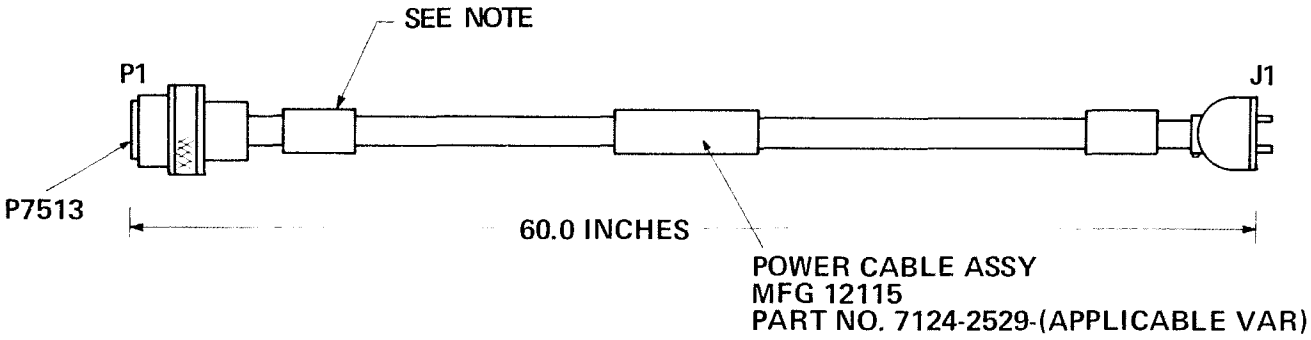
DRAWN 15 OCT 70
DESIGNER
CHECK
ENGR
APPD 21 Jul 73
CONT NO
7124-070 31 JUL 73
ENGRG RELEASE NOTICE
CUSTOMER APPROVAL

SIERRA RESEARCH CORP
POST OFFICE BOX 222 • BUFFALO, NEW YORK 14225

LOGIC DIAGRAM, CHANNEL SELECT

SIZE D | CODE IDENT NO. 12115 | 7006-0532

SCALE NONE | SHEET 1 OF 1



POWER CABLE ASSEMBLIES 7124-2529							
-1		-2		-3		-4	
P1(60 Hz)		P1(400 Hz)		P1(28 VDC)		P7513(400 Hz)	
Input	To Pin	Input	To Pin	Input	To Pin	Input	To Pin
115 VAC	G	115 VAC	G	28 VDC	G	115 VAC	C
115 VAC RTN	J	115 VAC RTN	E	28 VDC RTN	A	115 VAC RTN	A
JUMPER	K to C	JUMPER	K to F	JUMPER	K to H	JUMPER	D to B
JUMPER	B to H			JUMPER	D to F		
JUMPER	D to F						

NOTES:
1. Cable Assemblies 7124-2529-1, -2, and -3 connector P1 mates with J1 on TACAN Beacon Test Set.
2. Cable Assembly 7124-2529-4 connector P7513 mates with J7513 on TACAN Beacon Test Set.

Figure 931. Power Cable Assembly Diagram

CONTENTS
STORAGE INSTRUCTIONS

Paragraph		Page
1.	General	1001

STORAGE INSTRUCTIONS

1. GENERAL

A. Store the TACAN Beacon Test Set in its transit case (if provided). Figure 1001 illustrates the transit case.

Figure 1001. TACAN Beacon Test Set Transit Case

CONTENTS

SPECIAL TOOLS, FIXTURES, AND TEST EQUIPMENT

Paragraph		Page
1.	Test Equipment	1101
2.	Special Tools	1102
3.	Special Fixtures	1102

SPECIAL TOOLS, FIXTURES, AND TEST EQUIPMENT

1. TEST EQUIPMENT

The following test equipment or equivalent is required to test and trouble-shoot the TACAN Beacon Test Set. All test equipment must be properly calibrated.

NOTE: Testing and alignment of the KDM-7000 Digital DME requires that the test equipment be precisely calibrated particularly for the power and sensitivity measurements. Refer to Overhaul Manual for KDM-7000 Digital DME.

Nomenclature	Model	Characteristics Required	Manufacturer
TACAN Beacon Simulator	DTS-101A modified	Refer to TACAN Beacon Simulator Manual	Republic Electronics Industries
Oscilloscope	454	Refer to Oscilloscope Manual	Tektronix
Frequency Counter	5246L	DC to 1213 MHz	Hewlett-Packard
Frequency Converter	5254C	Used in conjunction with Frequency Counter	Hewlett-Packard
Digital Voltmeter	8100A	D-c volts ± 0.05% plus 0.01% of range	Fluke
Peak Power Meter	8900B	Basic scale 200 mv	Boonton
RF Microwatt Meter	41A	70 db dynamic range	Boonton
RF Signal Generator	8614A	962 MHz to 1213 MHz frequency range, calibrated output 0 dbm to -100 dbm	Hewlett-Packard
Multimeter	TS-352/U	—	—
Attenuator	—	10 db, Type N	—
Attenuator	—	20 db, Type N	—
Attenuator	—	30 db, Type N	—
Attenuator	—	40 db, Type N	—

Nomenclature	Model	Characteristics Required	Manufacturer
Power Supply	4010	Digital stability within 0.1% + 1 millivolt. Stability better than 0.001% + 100 microvolt after warmup	Power Designs Inc.

2. SPECIAL TOOLS

Special tools required for the TACAN Beacon Test Set DME are identified in the Overhaul Manual for KDM-7000 Digital DME.

2. SPECIAL FIXTURES

Special fixtures required for the TACAN Beacon Test Set DME are identified in the Overhaul Manual for KDM-7000 Digital DME.

CONTENTS
ILLUSTRATED PARTS LIST

	Description	Page
1.	TACAN Beacon Test Set	1201
2.	Panel and Chassis Assembly	1205
3.	Modified DME Rack	1210
4.	SAU Rack	1212
5.	Modified DBU Rack	1214
6.	Connector Keying Information	1216
7.	Channel Select Printed Wiring Assembly	1217
8.	Rear Panel Assembly	1219
9.	Digital Bearing Unit	1221
10.	DBU Cover	1224
11.	Power Supply Regulator	1226
12.	Memory Counter	1229
13.	Digital Video Signal	1233
14.	Reference Counter	1239
15.	Pulse Group Decoder	1243
16.	Digital Bearing Unit Monitor (7124-4305-1)	1247
17.	Digital Bearing Unit Monitor (7124-4305-2)	1251
18.	Signal Analyzer Unit	1254
19.	SAU Cover	1256
20.	Power Supply Regulator	1258
21.	Limit Detector (7124-1110-1)	1261
22.	Limit Detector (7124-1110-2)	1266
23.	Signal Processor	1271
24.	Console Display and Control Panel Unit	1276
25.	Led Display	1280
26.	Led Logic	1285
27.	Course Select	1288
28.	Manufacturer's Name/Code	1290

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1200-	7124-0160-2	TACAN BEACON TEST SET V-12115		1
	7124-2512-2*	PANEL AND CHASSIS ASSEMBLY V-12115		2
	7124-2523-1*	REAR PANEL ASSEMBLY V-12115		3
	7124-2508	IDENTIFICATION PLATE V-12115 (Selected Item)		4
	7124-5000-2	DISTANCE MEASURING EQUIPMENT V-12115		5
	7124-4000-2	DIGITAL BEARING UNIT V-12115		6
	7124-0140-2	SIGNAL ANALYZER UNIT V-12115		7
	7124-0130-2	CONSOLE DISPLAY AND CONTROL PANEL UNIT V-12115		8
	E121920H*	CASE V-10110		9
	7124-2529-1	CABLE ASSEMBLY, 115V, 60 HZ V-12115		10
P1	MS3116F12-10S	CONNECTOR		11
J1	5264	CONNECTOR V-72268		12
	7124-2529-2	CABLE ASSEMBLY, 115V, 400 HZ V-12115		13
P1	MS3116F12-10S	CONNECTOR		14
J1	9970	CONNECTOR V-72268		15
	7124-2529-3	CABLE ASSEMBLY, 28 VDC V-12115		16
P1	MS3116F12-10S	CONNECTOR		17
J1	7436	CONNECTOR V-72268		18

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1200-	7124-0160-2	TACAN BEACON TEST SET V-12115 (Cont)		
	7124-2529-4	CABLE ASSEMBLY, RACK 400 HZ V-12115		19
P7513	MS3116F8-4S	CONNECTOR		20
J1	9970	CONNECTOR V-72268		21
	7124-2531-2	INTERCONNECTING CABINET V-12115 (Consists of Items Identified by Single Asterisk)		22
1001	7124-2532-2	TRANSIT CASE V-12115 (Selected Item)		23
		NOTE		
		* PART OF 7124-2531-2		

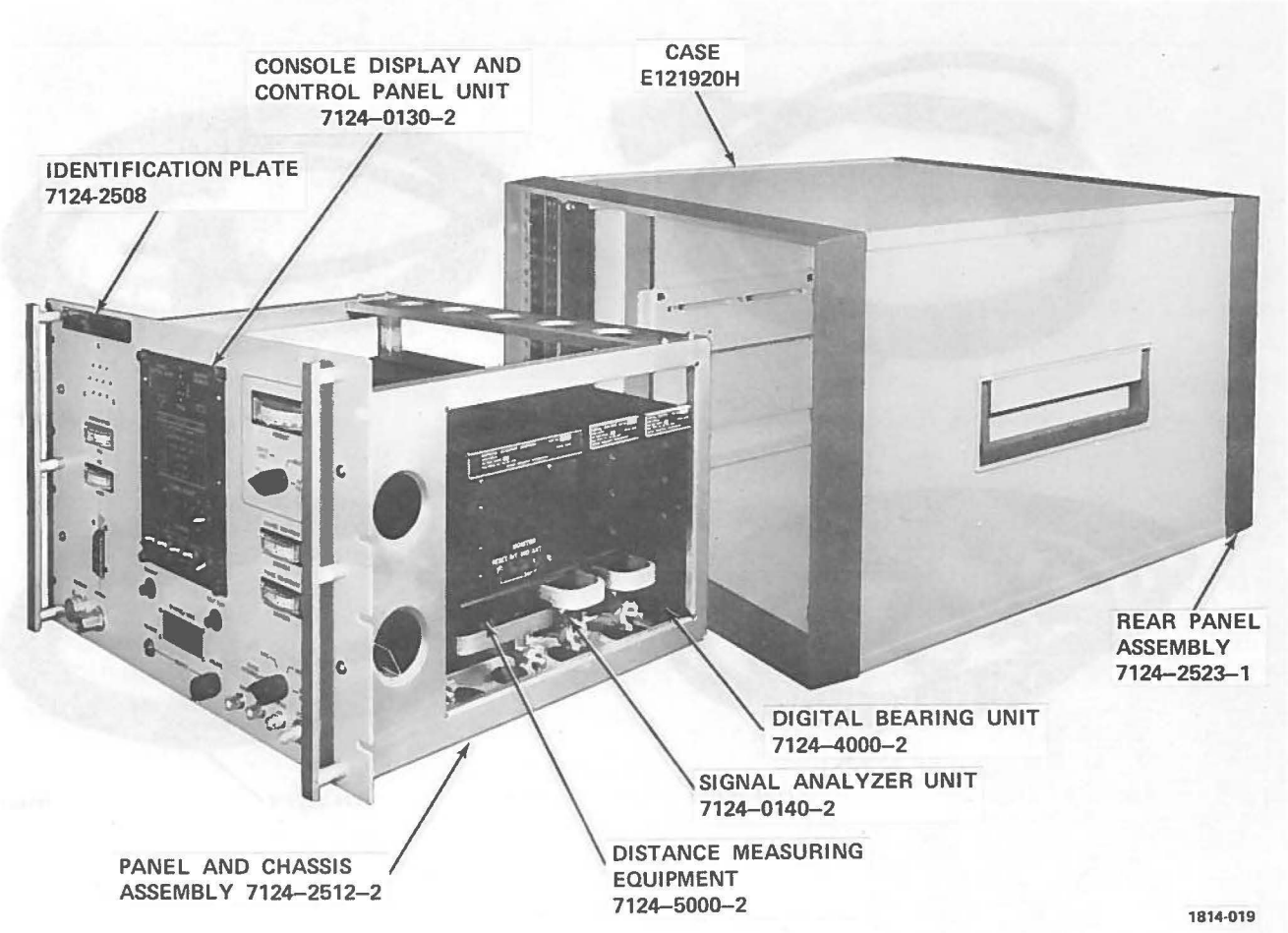


Figure 1200. TACAN Beacon Test Set (Sheet 1 of 2)

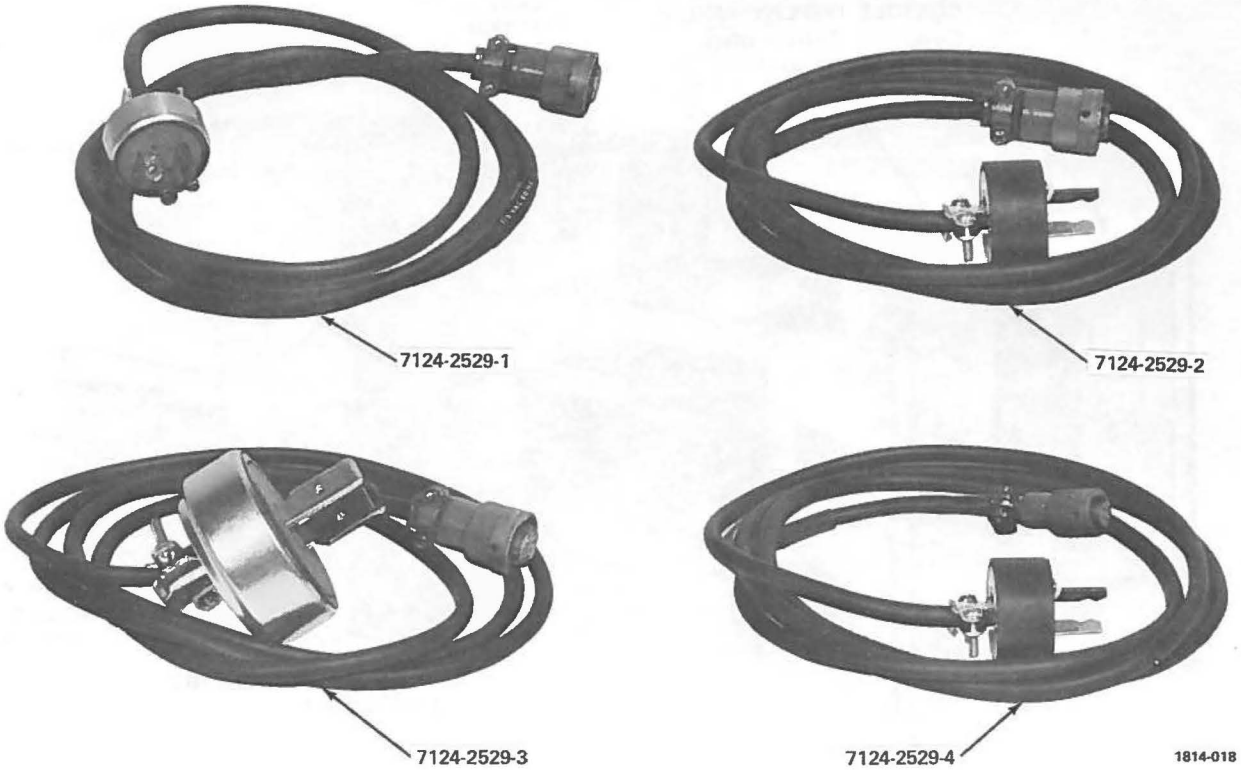


Figure 1200. TACAN Beacon Test Set (Sheet 2 of 2)

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1201-	7124-2512-2	PANEL AND CHASSIS ASSEMBLY V-12115		1
A7505	7006-0530-1	CHANNEL SELECT PRINTED WIRING ASSEMBLY V-12115		2
AT7501	7124-2528-1	ATTENUATOR SWITCH V-12115		3
CP7501	UG-27B/U	COAXIAL CONNECTOR		4
J7501		(SEE FIG. 1204)		5
J7502		(SEE FIG. 1203)		6
J7503		(SEE FIG. 1202)		7
J7504	2-DD-100P	CONNECTOR V-71468		8
J7505	00-7008-017-163-001	CONNECTOR V-91662		9
J7506	MS3112E14-15S	CONNECTOR		10
J7509	UG-1094/U	COAXIAL CONNECTOR		11
J7510	UG-1094/U	COAXIAL CONNECTOR		12
J7511	UG-1094/U	COAXIAL CONNECTOR		13
J7512	UG-160C/U	COAXIAL CONNECTOR (PART OF CABLE ASSEMBLY W7501)		14
J7513	MS3114E8-4P	CONNECTOR		15
	MS3116F14-15P	CONNECTOR (MATES WITH J7506 FOR RECORDER CONNECTIONS)		16
J7514	UG-1094/U	COAXIAL CONNECTOR		17
J7515	UG-23B/U	COAXIAL CONNECTOR (PART OF CABLE ASSEMBLY W7501)		18
LS7501	22A062100	SPEAKER V-74199		19
M7501	SC6625-0005-3	METER V-12115		20
M7502	SC6625-0005-4	METER V-12115		21

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1201-	7124-2512-2	PANEL AND CHASSIS ASSEMBLY V-12115 (Cont)		
M7503	SC6625-0004-1	METER V-12115		22
M7504	SC6625-0005-1	METER V-12115		23
M7505	SC6625-0005-2	METER V-12115		24
P7501	12A	PHONE JACK		25
P7507	3190-1	COAXIAL CONNECTOR V-95712		26
R7501	RV4NAYSD102A	RESISTOR, VARIABLE		27
R7502	RN60C1243F	RESISTOR		28
R7503	RN60C1003F	RESISTOR		29
R7506	RN60C1003F	RESISTOR		30
R7507	RCR07G101JS	RESISTOR		31
R7508	RN60C2003F	RESISTOR		32
R7509	RN60C2003F	RESISTOR		33
R7510	RCR07G101JS	RESISTOR		34
S7501	PA2043	SWITCH V-71590		35
S7502	PA2045	SWITCH V-71590		36
S7503	01-700155	SWITCH, PUSHBUTTON V-04426		37
S7504	01-700155	SWITCH, PUSHBUTTON V-04426		38
S7505	MST105D	SWITCH, TOGGLE V-95146		39
S7506	8-S-45A	SWITCH V-07126		40
W7501	7124-2520-1	CABLE ASSY, R-F V-12115		41
	7006-0738-2	NAMEPLATE HOLDER V-12115		42

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1201-	7124-2512-2	PANEL AND CHASSIS ASSEMBLY V-12115 (Cont)		
		RACK, MODIFIED, DME V-12115 (SEE FIG. 1202)		43
		RACK, SAU V-81860 (SEE FIG. 1203)		44
		RACK, MODIFIED, DBU V-12115 (SEE FIG. 1204)		45
	7124-2510-2	PANEL, FRONT V-12115		46
	7124-2518-1	FRAME, LEFT SIDE V-12115		47
	7124-2519-1	FRAME, RIGHT SIDE V-12115		48
	7124-2522-1	BRACKET, REAR V-12115		49
	DD-19977-4	HOOD (FOR J7504) V-71468		50
	DD-51223-1	SLIP LOCK (FOR J7504) V-71468		51
	406074	CLAMP (3) V-06773		52
	80-70319	NUT (FOR S7503 AND S7504) V-04426		53
	H12	HANDLE (2) V-10110		54
	1131C	WASHER, INTERNAL THREADED (FOR MOUNTING S7501, S7502, AND R7501) V-83330		55
	751-2	TERMINAL LUG V-79963		56
	207-160351-00-0101	BUTTON (6) V-02768		57

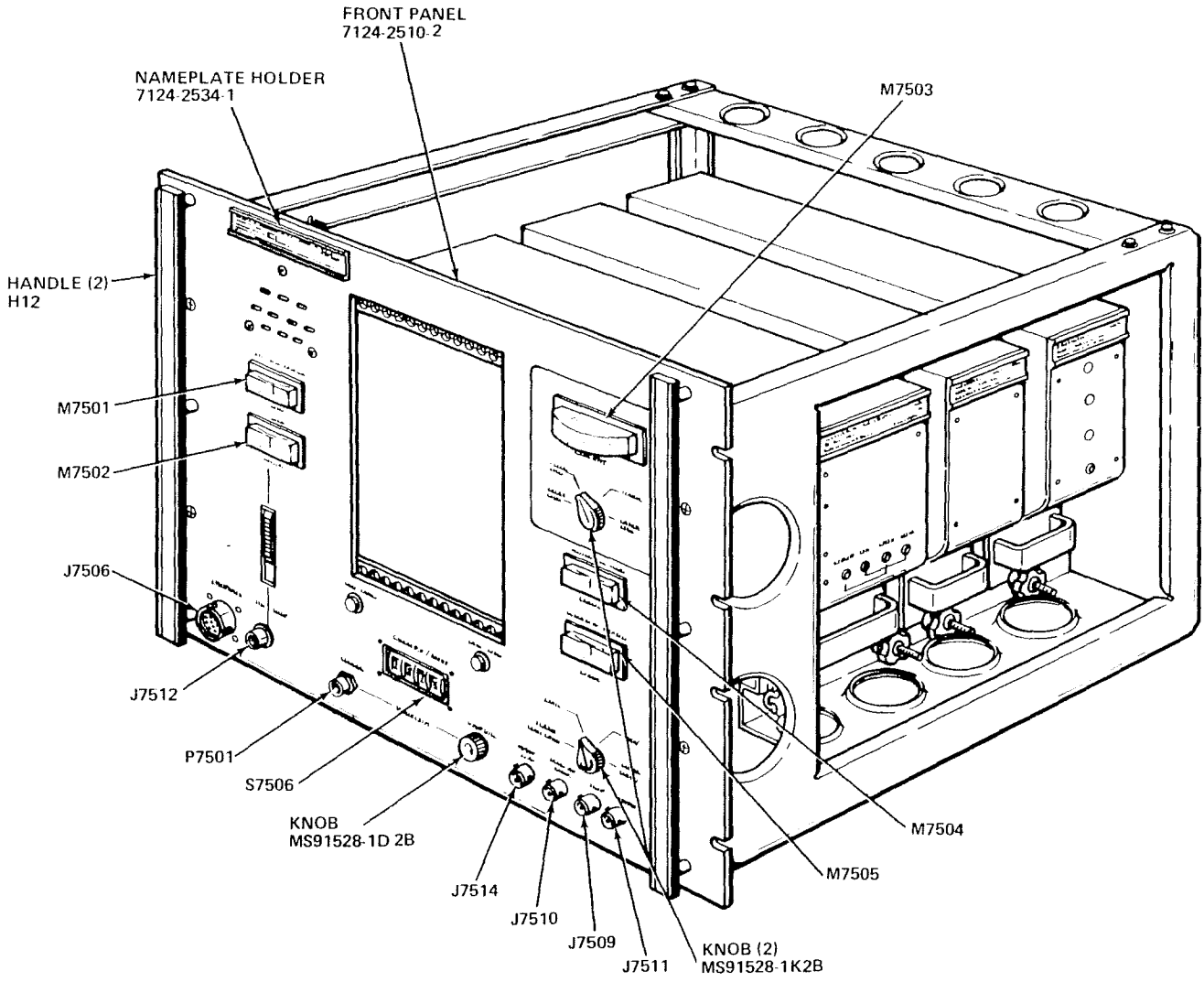


Figure 1201. Panel and Chassis Assembly (Sheet 1 of 2)

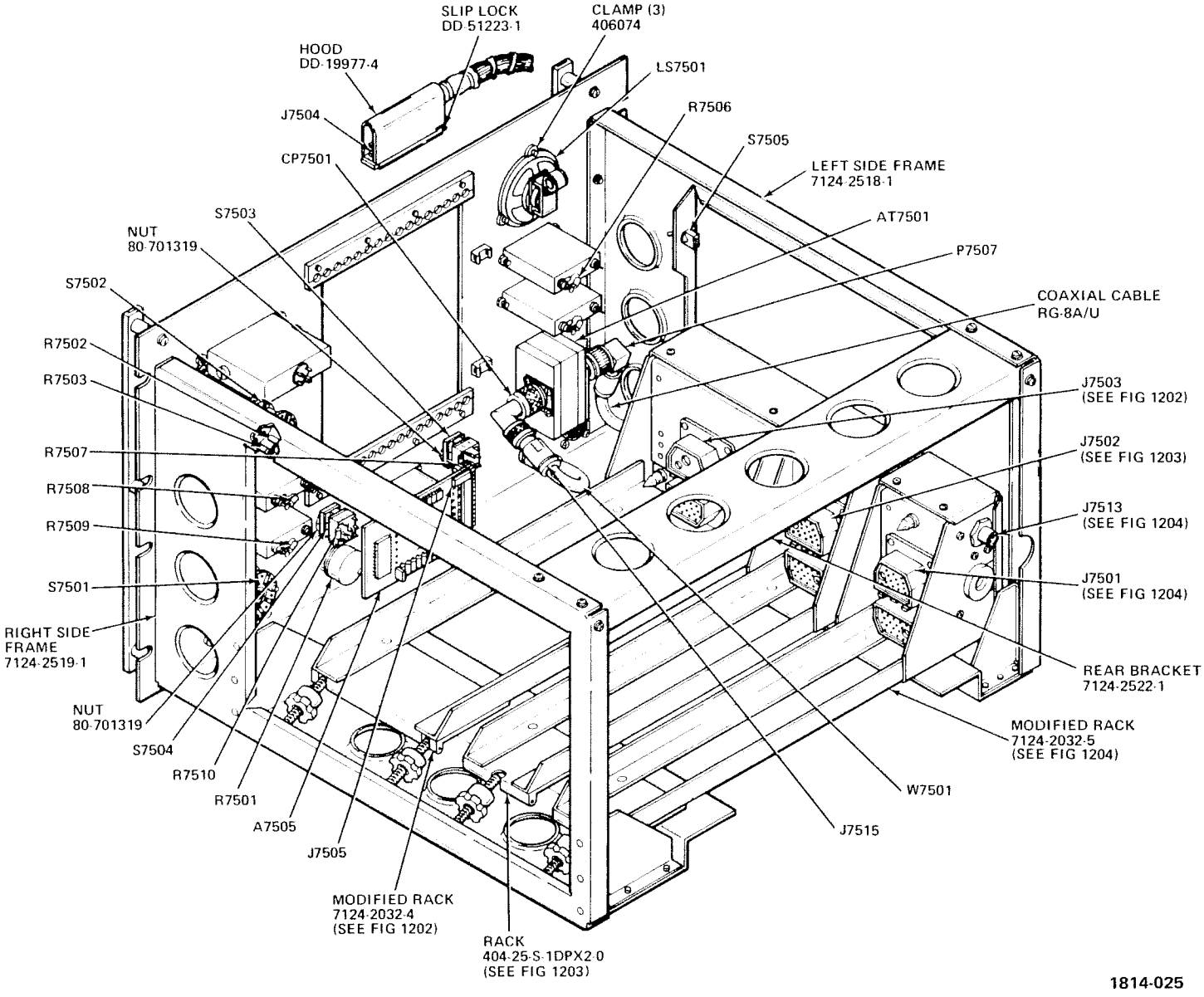


Figure 1201. Panel and Chassis Assembly (Sheet 2 of 2)

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1202-	7124-2032-4	RACK, MODIFIED, DME V-12115		1
J7503	DPX2MA-AC3S-67S-33B-0019	CONNECTOR V-71468 (SEE FIG. 1205 FOR KEYING INFORMATION)		2
	404-.50-S-1/DPX2-0	RACK V-81860		3
	MS21266-1N	PLASTIC EDGING GROMMET		4

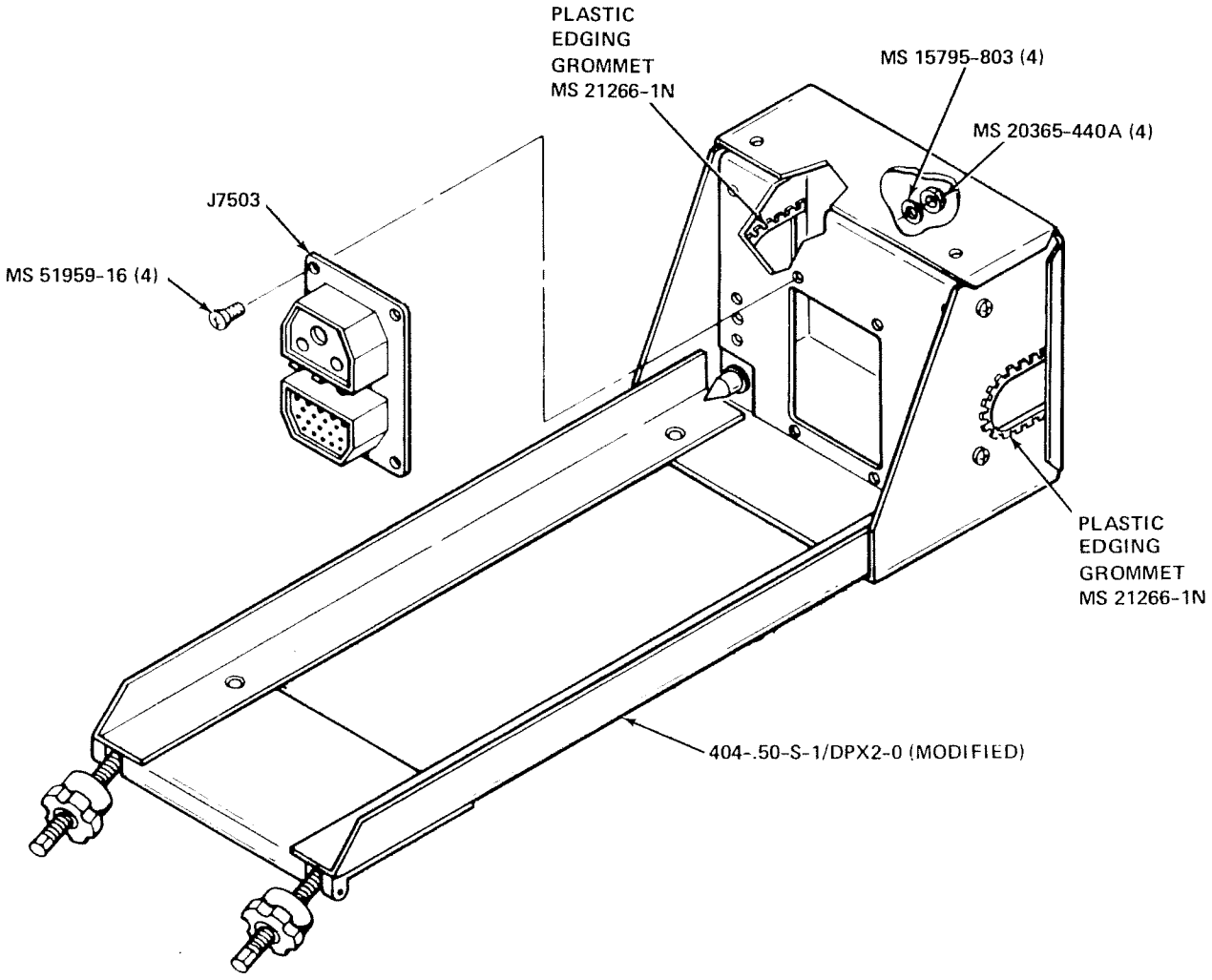


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Figure 1202. Distance Measuring Equipment Mounting Rack Assembly

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1203-	404-.25-S-1DPX2-0	RACK, SAU V-81860		1
J7502	DPX2MA-40W1- 40W1S-33B-0004	CONNECTOR V-71468 (SEE FIG. 1205 FOR KEYING INFORMATION)		2
	MS21266-1N	PLASTIC EDGING GROMMET		3

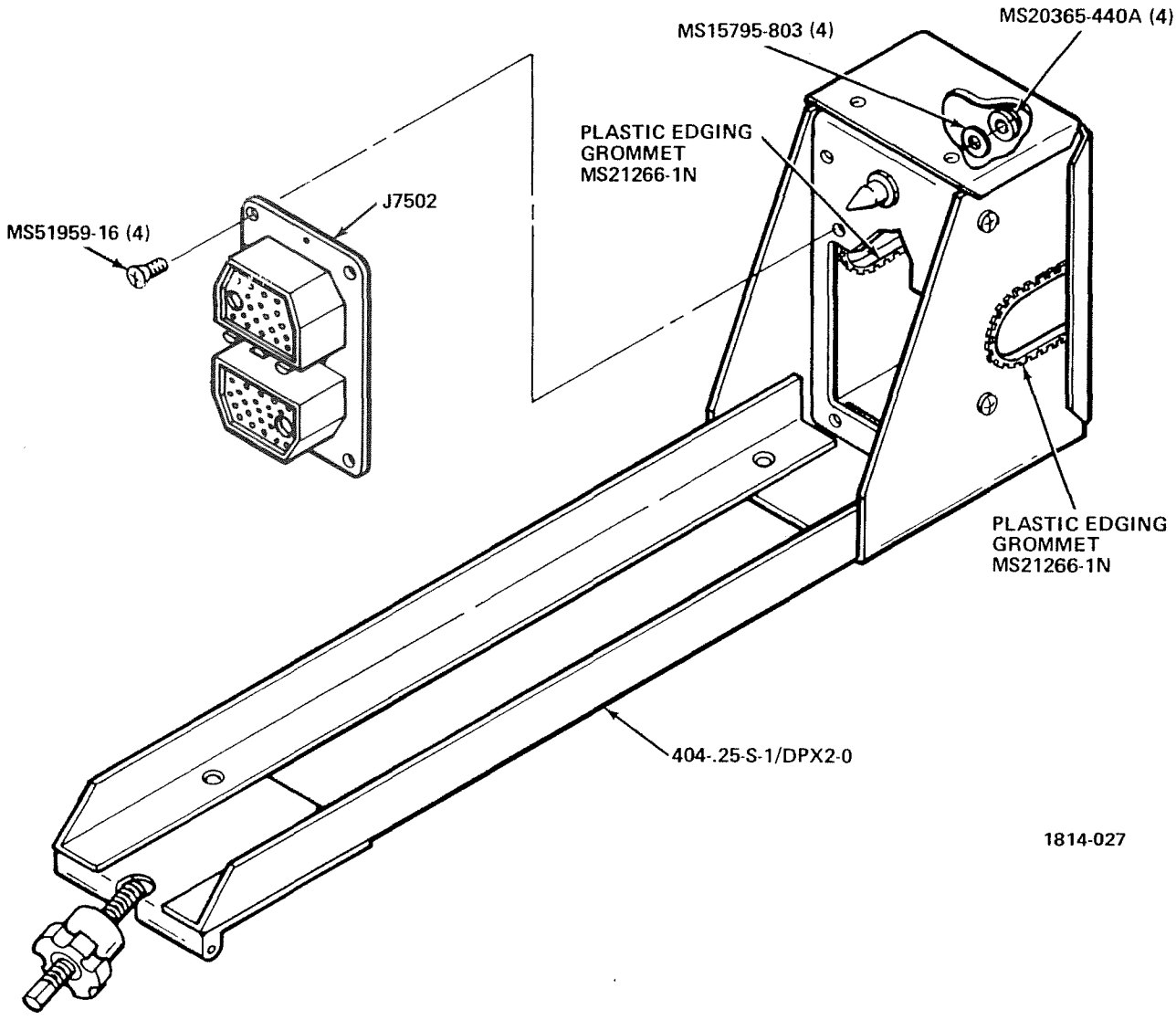


Figure 1203. Signal Analyzer Unit Mounting Rack Assembly

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1204-	7124-2032-5	RACK, MODIFIED, DBU V-12115		1
J7501	DPX2MA-40W1-40W1S-33B-0022	CONNECTOR V-71468 (SEE FIG. 1205 FOR KEYING INFORMATION)		2
J7513	MS3114E8-4P	CONNECTOR		3
	MS21266-1N	PLASTIC EDGING GROMMET		4
	249-1400-000	COAXIAL CONTACT V-71468		5

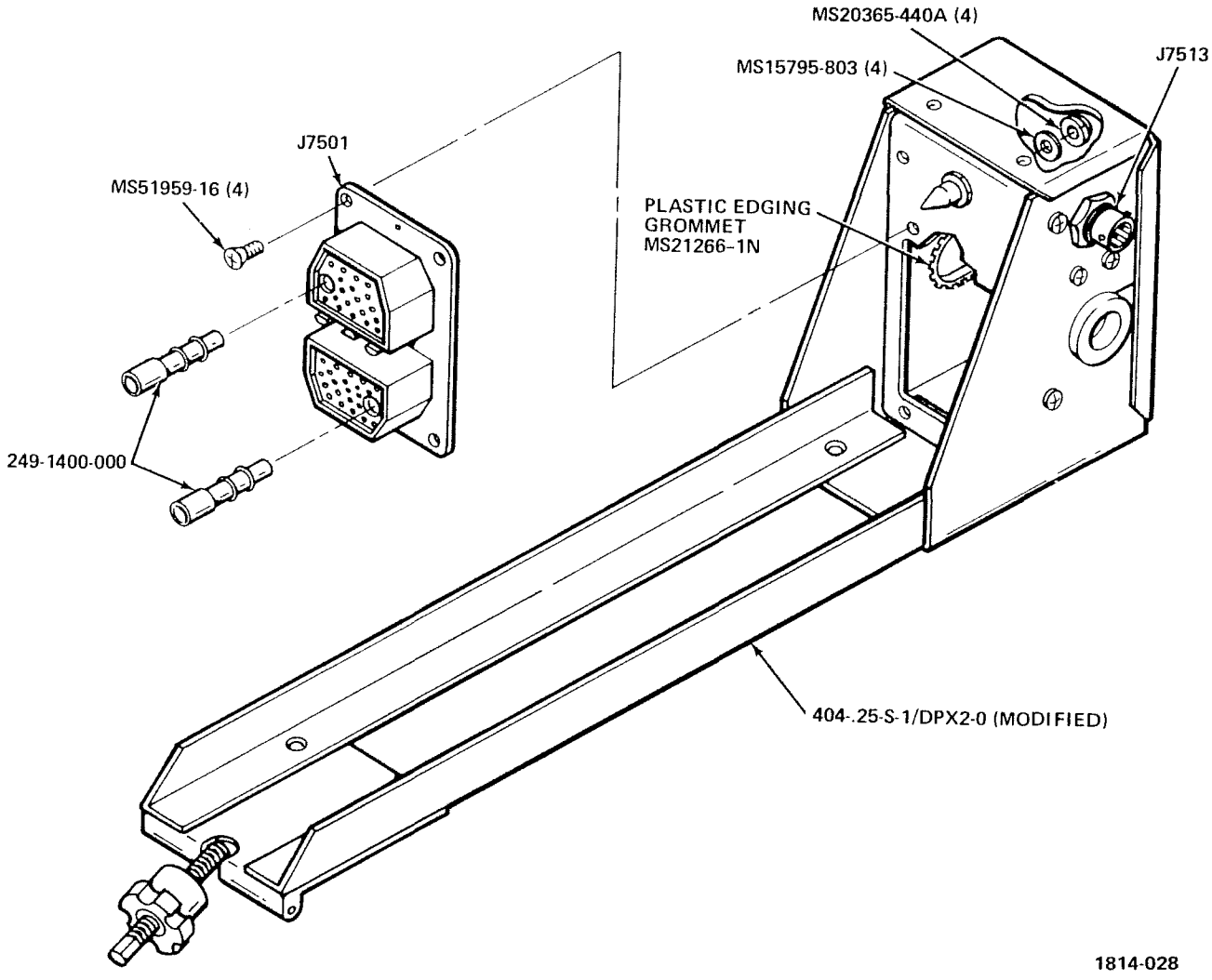


Figure 1204. Digital Bearing Unit Mounting Rack Assembly

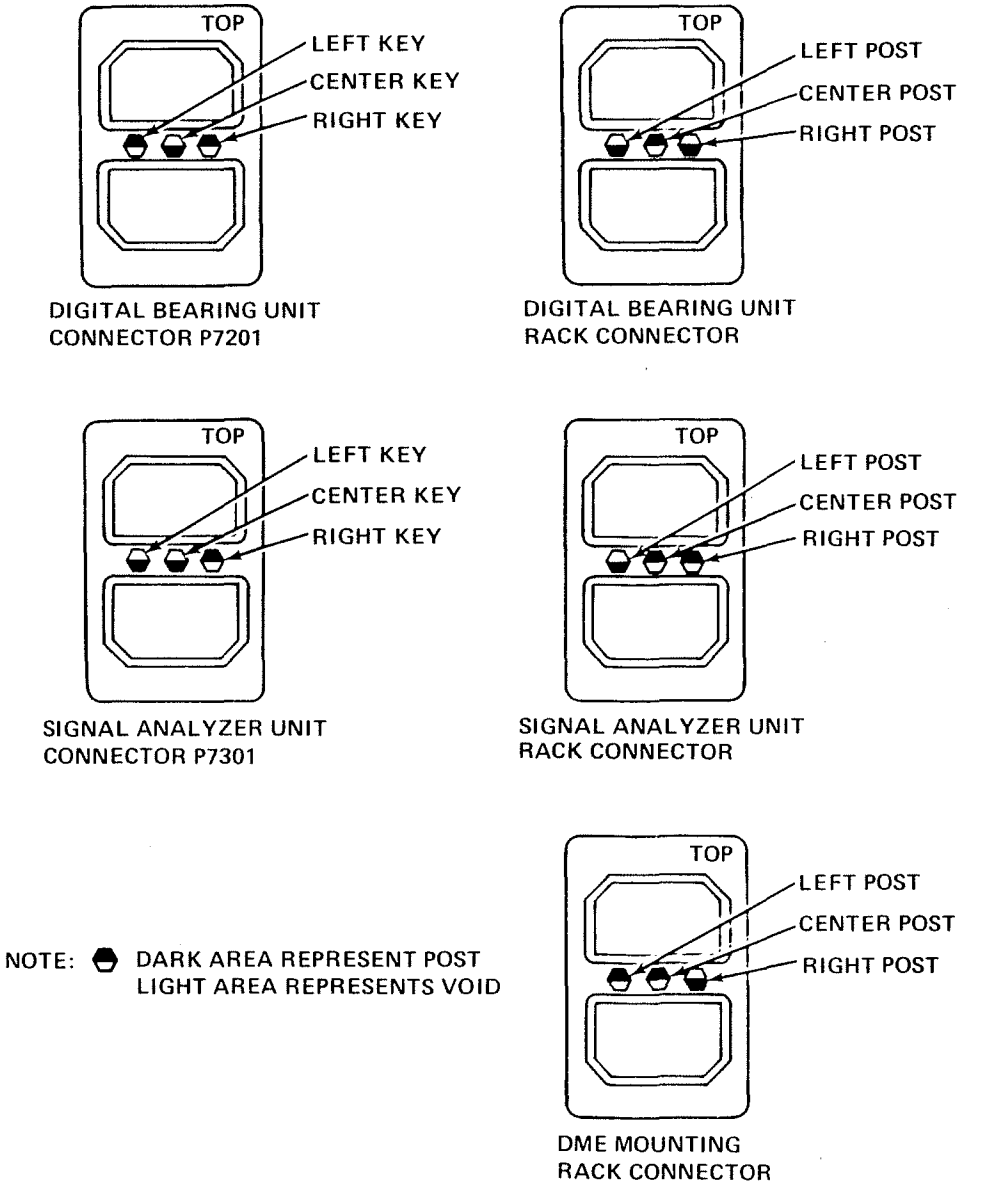


Figure 1205. Connector Keying Information

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1206-	7006-0530-1	CHANNEL SELECT PRINTED WIRING ASSEMBLY V-12115		1
C2001	CK06BX104K	CAPACITOR		2
J2001	2VH6/1AK5	CONNECTOR V-05574		3
J2002	2VH6/1AK5	CONNECTOR V-05574		4
J2003	2VH6/1AK5	CONNECTOR V-05574		5
J2004	2VH6/1AV8	CONNECTOR V-05574		6
P2001	00-7022-017-000-001	CONNECTOR V-91662		7
R2001	RCR07G103JS	RESISTOR		8
R2002	RCR07G103JS	RESISTOR		9
R2003	RCR07G103JS	RESISTOR		10
R2004	RCR07G103JS	RESISTOR		11
R2005	RCR07G103JS	RESISTOR		12
R2006	RCR07G103JS	RESISTOR		13
R2007	RCR07G103JS	RESISTOR		14
R2008	RCR07G103JS	RESISTOR		15
R2009	RCR07G103JS	RESISTOR		16
R2010	RCR07G103JS	RESISTOR		17
R2011	RCR07G103JS	RESISTOR		18
U2001	SC5962-0070-1	INTEGRATED CIRCUIT, PROGRAMMED V-12115		19
U2002	SN5406N	INTEGRATED CIRCUIT V-01295		20
U2003	SN5406N	INTEGRATED CIRCUIT V-01295		21

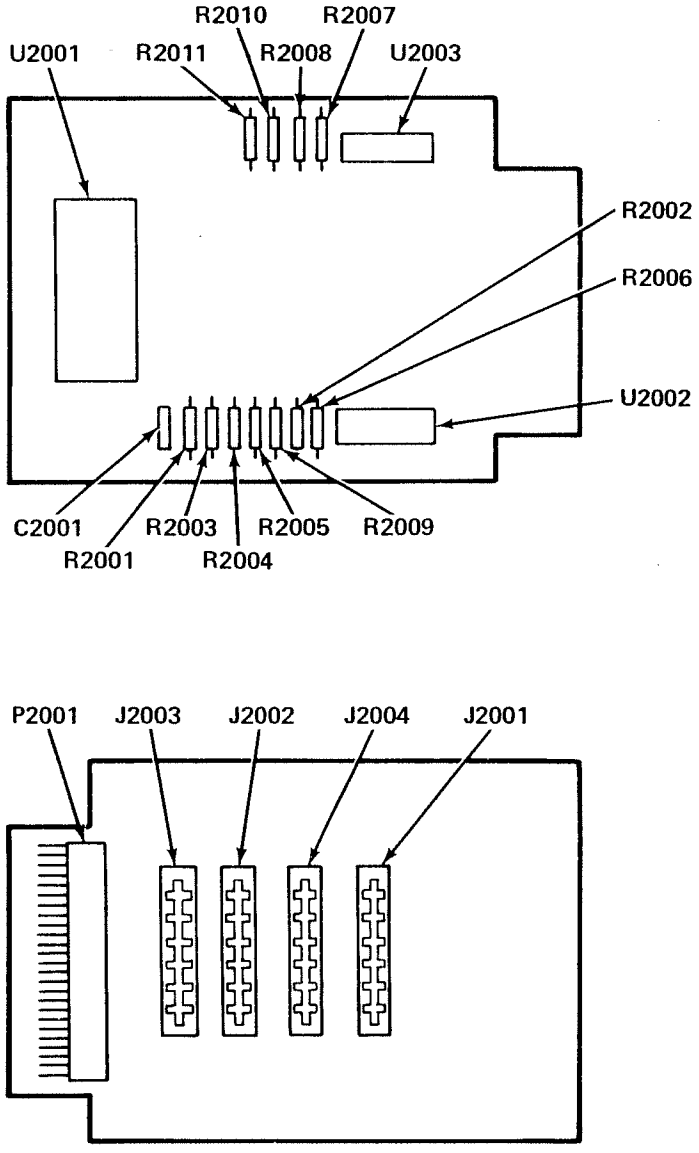


Figure 1206. Channel Select Printed Wiring Assembly

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1207-	7124-2523-1	REAR PANEL ASSEMBLY V-12115		1
B7501	SPA2A	FAN V-82877		2
C7501	602D129A1	CAPACITOR V-56289		3
CB7501	7274-2-2-1/2	CIRCUIT BREAKER V-83803		4
CB7502	7274-2-2	CIRCUIT BREAKER V-83803		5
CB7503	7274-2-7-1/2	CIRCUIT BREAKER V-83803		6
CR7501	680-1	RECTIFIER V-12969		7
P7513	MS3114E8-4S	CONNECTOR		8
J1	MS3112E12-10P	CONNECTOR		9
	MS3106B18-9S	CONNECTOR (SUPPLIED AS PART OF STATIC INVERTER)		10
T7501	24-0297-00	TRANSFORMER V-11402		11
	PC-15B	STATIC INVERTER V-07181		12
	20049	GUARD V-82877		13
	7124-2524-1	PANEL, REAR V-12115		14
	7124-2525-1	CAPACITOR BRACKET V-12115		15
	6179-1A	CRADLE (2) V-91506		16

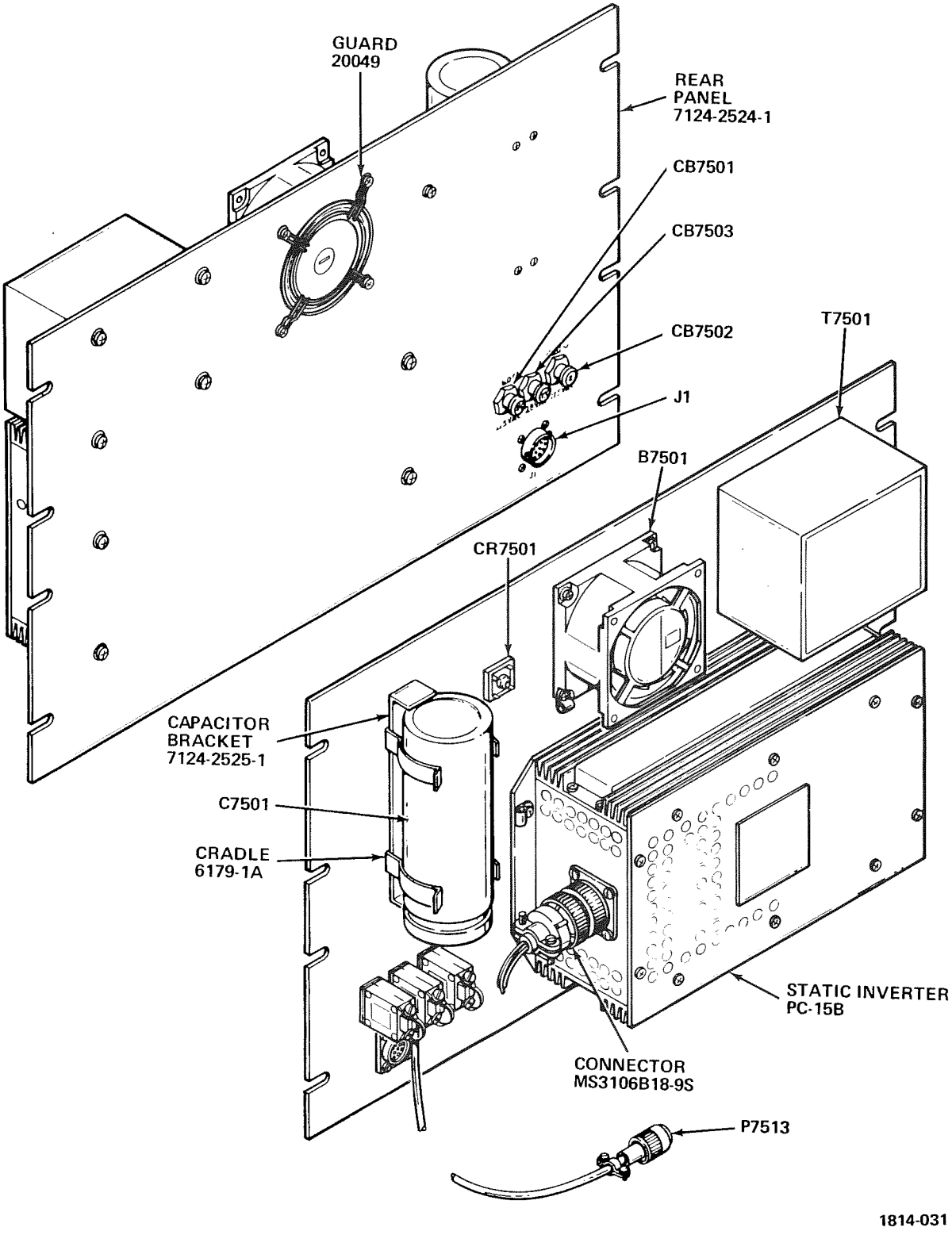


Figure 1207. Rear Panel Assembly

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1208-	7124-4000-2	DIGITAL BEARING UNIT V-12115		1
A100	7109-3020-1	POWER SUPPLY REGULATOR V-12115		2
A200	7124-4300-1	MEMORY COUNTER V-12115		3
A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115		4
A400	7124-4310-1	REFERENCE COUNTER V-12115		5
A500	7124-4320-2	PULSE GROUP DECODER V-12115		6
A600	7124-4305-1 OR 7124-4305-2	DIGITAL BEARING UNIT MONITOR V-12115		7
C7201	602D40-G015-AA2A	CAPACITOR, 4000 μF, 15 VDC V-56289		8
CR7201	680-1	DIODE, RECTIFIER V-12969		9
J101	00-7008-017-163-001	CONNECTOR V-91662		10
J201	00-7008-029-163-001	CONNECTOR V-91662		11
J301	00-7008-041-163-001	CONNECTOR V-91662		12
J401	00-7008-041-163-001	CONNECTOR V-91662		13
J501	00-7008-029-163-001	CONNECTOR V-91662		14
J601	00-7008-017-163-001	CONNECTOR V-91662		15
P7201	DPX2J-42226-26	CONNECTOR (SEE FIG. 1205 FOR KEYING INFORMATION) V-71468		16
Q7201	2N4231	TRANSISTOR V-07263		17
T7201	SC5950-0041-2	TRANSFORMER V-12115		18

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1208-	7124-4000-2	DIGITAL BEARING UNIT V-12115 (Cont)		
	PK-11-66-M	INSULATOR KIT V-08289		19
	60-5006-34-14	POLARIZING KEY V-91662		20
	1488-4	SOLDER LUG V-83330		21
	1410-6	SOLDER LUG V-83330		22
	1410-10	SOLDER LUG V-83330		23
	2175	GROMMET V-83330		24
	MS21266-1N	GROMMET		25

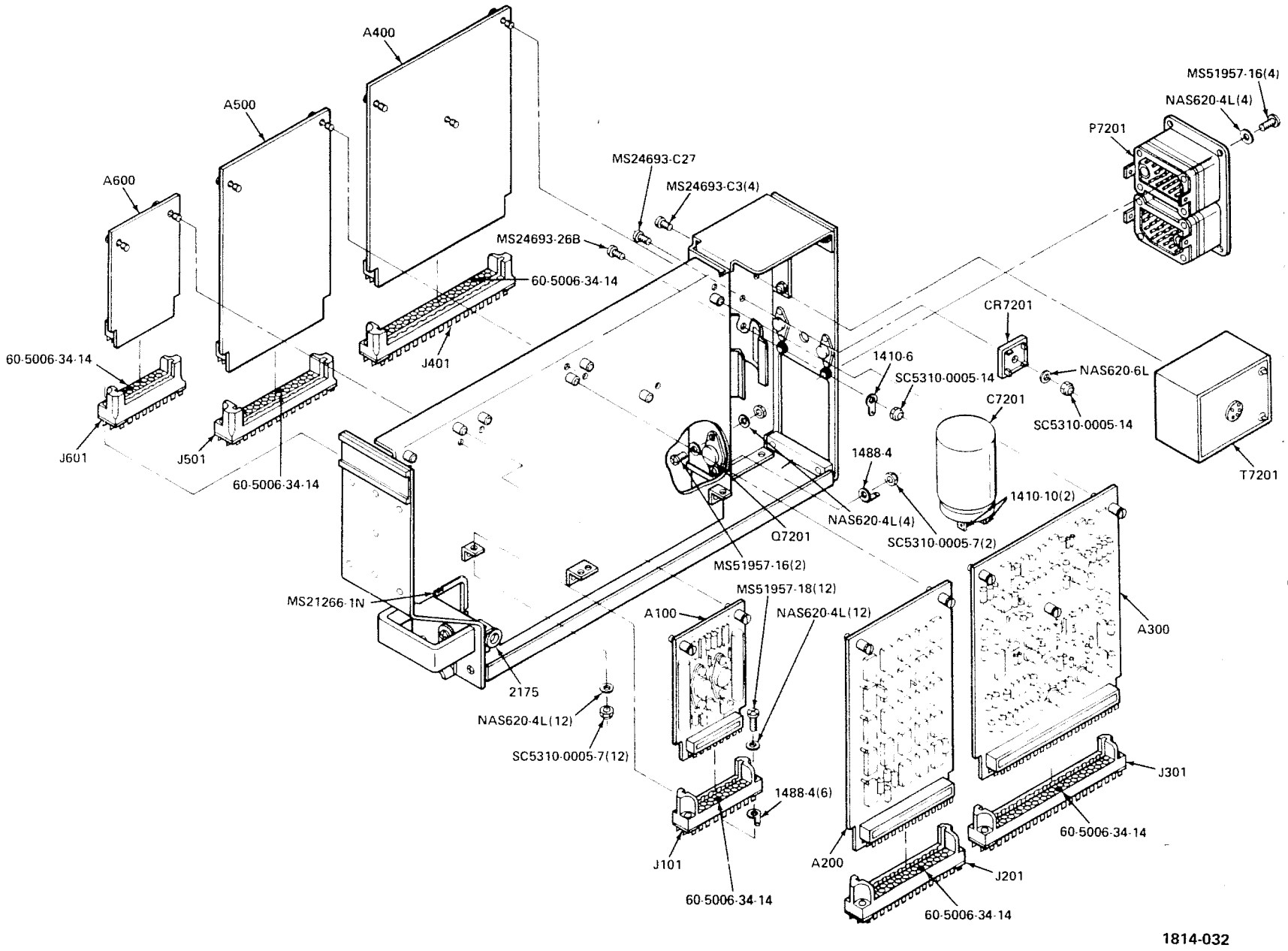


Figure 1208. Digital Bearing Unit

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1209-	7006-0739-2	COVER, DBU V-12115		1
	7124-4011-1	MAIN FRAME V-12115		2
	7006-0732-3	FRONT PANEL V-12115		3
	7006-0733-2	REAR PANEL V-12115		4
	7006-0734-1	BOTTOM PLATE V-12115		5
	7124-3008-3	NAMEPLATE V-12115		6
	7006-0738-1	NAMEPLATE HOLDER V-12115		7
	7006-0737-1	MOUNTING BAR V-12115		8
	FCA9	HANDLE V-08730		9
	HDH-4	RETAINER HOOK V-94867		10

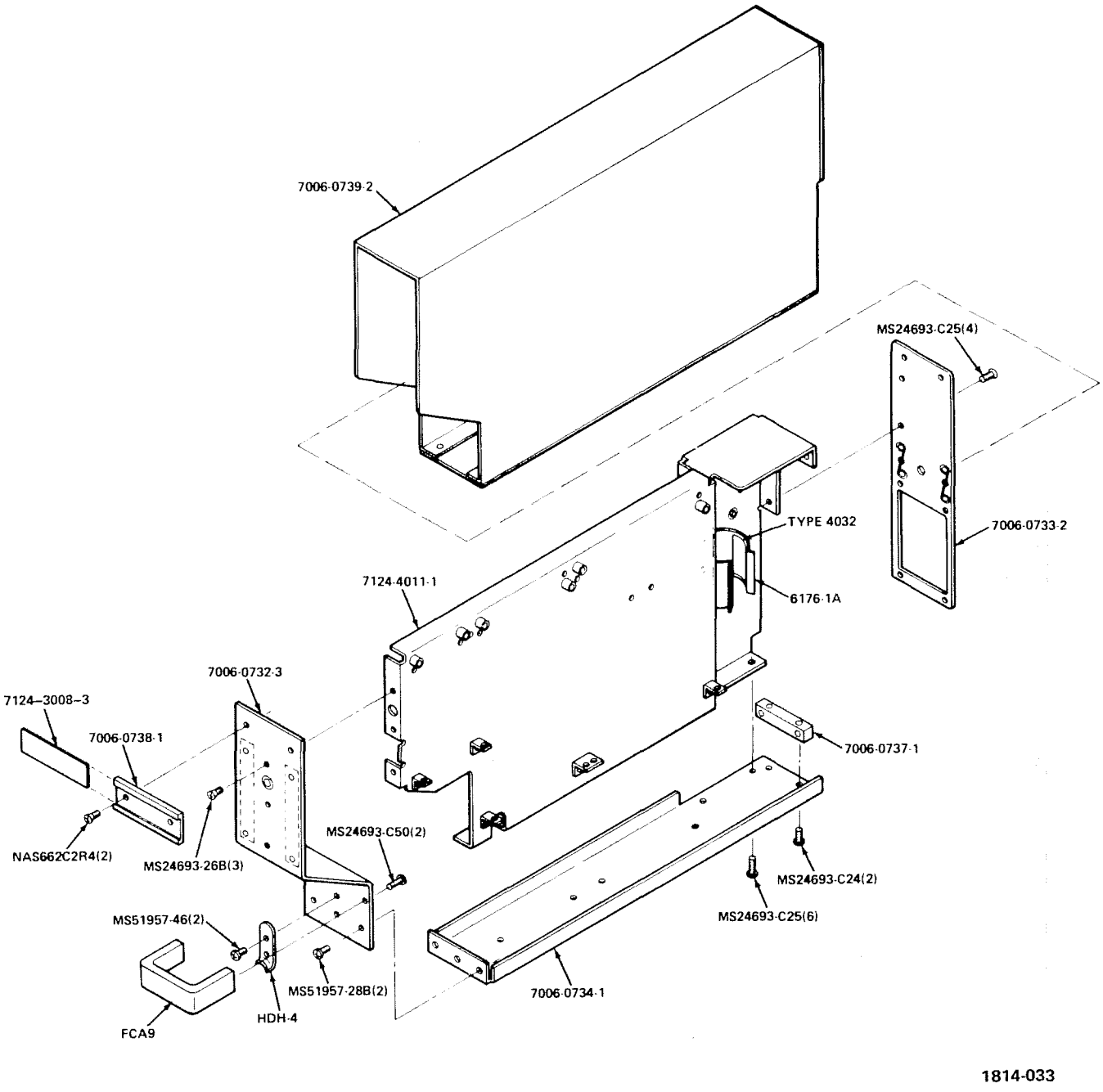


Figure 1209. Digital Bearing Unit Cover and Main Frame

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1210-A100	7109-3020-1	POWER SUPPLY REGULATOR V-12115		1
C101	CK05BX102K	CAPACITOR, 0.001μF		2
C102	CK06BX104K	CAPACITOR, 0.1μF		3
C103	S106R-20	CAPACITOR, 10μF V-06751		4
C104	600D337-G030-DL4	CAPACITOR, 330μF V-56289		5
C105	600D337-G030-DL4	CAPACITOR, 330μF V-56289		6
C106	CK05BX102K	CAPACITOR, 0.001μF		7
C107	CK06BX104K	CAPACITOR, 0.1μF		8
C108	S106R-20	CAPACITOR, 10μF V-06751		9
CR101	1N4002	DIODE		10
CR102	1N4002	DIODE		11
CR103	1N4002	DIODE		12
CR104	1N4002	DIODE		13
CR105	1N4002	DIODE		14
P101	00-7022-017-000-001	CONNECTOR V-91662		15
Q101	2N2222A	TRANSISTOR		16
R101	RS1A	RESISTOR, 1.5 OHMS, ±3%, V-91637		17
R102	RN60C1692F	RESISTOR		18
R103	3099P-1-501	RESISTOR, VARIABLE, 500 OHMS V-80294		19
R104	RCR32G101JS	RESISTOR		20
R105	RN60C6811F	RESISTOR		21
R106	RS1A	RESISTOR, 2 OHMS, ±3% V-91637		22
R107	RN60C1692F	RESISTOR		23
R108	3099P-1-501	RESISTOR, VARIABLE, 500 OHMS V-80294		24
R109	RN60C6811F	RESISTOR		25
TP101	016-4005-BRN	TEST POINT V-98291		26

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1210-A100	7109-3020-1	POWER SUPPLY REGULATOR V-12115 (Cont)		
TP102	016-4005-RED	TEST POINT V-98291		27
TP103	016-4005-ORN	TEST POINT V-98291		28
TP104	016-4005-YEL	TEST POINT V-98291		29
TP105	016-4005-GRN	TEST POINT V-98291		30
U101	MC1569R	INTEGRATED CIRCUIT V-04713		31
U102	MC1563R	INTEGRATED CIRCUIT V-04713		32
VR101	1N4733	DIODE		33
	10034N	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		34
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		35
	68-1660-26	NUT, HEX, MINIATURE V-11117, V-12115 SPEC CONT DWG SC5310-0005-9		36

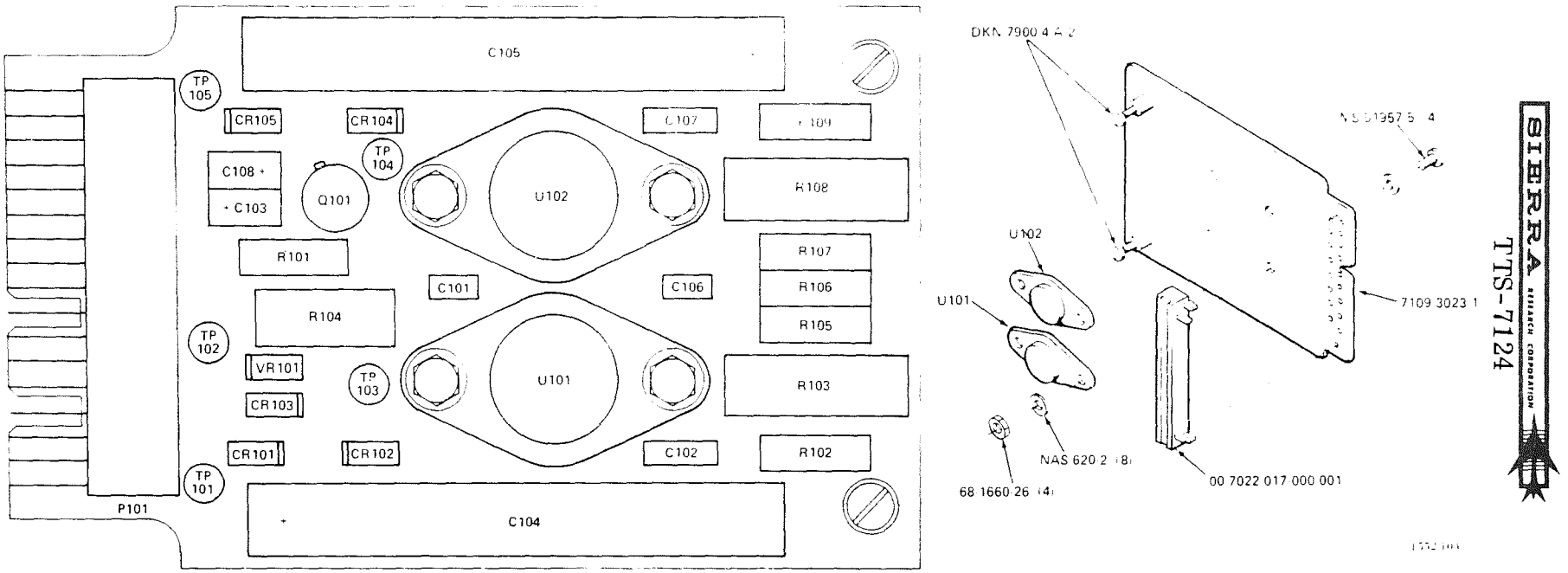


Figure 1210. Digital Bearing Unit Power Supply Regulator

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1211-A200	7124-4300-1	MEMORY COUNTER V-12115		1
C201	CK06BX105K	CAPACITOR, 1μF		2
C202	CK05BX102K	CAPACITOR, 0.001μF		3
C203	CK05BX102K	CAPACITOR, 0.001μF		4
P201	00-7022-029-000-001	CONNECTOR V-91622		5
R201	RCR07G102JS	RESISTOR		6
R202	RCR07G103JS	RESISTOR		7
R203	RCR07G103JS	RESISTOR		8
R204	RCR07G332JS	RESISTOR		9
TP201	016-4005-BRN	TEST POINT V-98291		10
TP202	016-4005-RED	TEST POINT V-98291		11
TP203	016-4005-ORN	TEST POINT V-98291		12
TP204	016-4005-YEL	TEST POINT V-98291		13
TP205	016-4005-GRN	TEST POINT V-98291		14
TP206	016-4005-BLU	TEST POINT V-98291		15
TP207	016-4005-VIO	TEST POINT V-98291		16
TP208	016-4005-GRA	TEST POINT V-98291		17
TP209	016-4005-WHT	TEST POINT V-98291		18
TP210	016-4005-BLK	TEST POINT V-98291		19
U201	S5400A	INTEGRATED CIRCUIT V-18324		20
U202	S54193B	INTEGRATED CIRCUIT V-18324		21
U203	S54193B	INTEGRATED CIRCUIT V-18324		22

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1211-A200	7124-4300-1	MEMORY COUNTER V-12115 (Cont)		
U204	S5474A	INTEGRATED CIRCUIT V-18324		23
U205	S5474A	INTEGRATED CIRCUIT V-18324		24
U206	S5474A	INTEGRATED CIRCUIT V-18324		25
U207	S5404A	INTEGRATED CIRCUIT V-18324		26
U208	S5400A	INTEGRATED CIRCUIT V-18324		27
U209	S54193B	INTEGRATED CIRCUIT V-18324		28
U210	S5402A	INTEGRATED CIRCUIT V-18324		29
U211	S5410A	INTEGRATED CIRCUIT V-18324		30
U212	S5474A	INTEGRATED CIRCUIT V-18324		31
U213	S5474A	INTEGRATED CIRCUIT V-18324		32
U214	S5486A	INTEGRATED CIRCUIT V-18324		33
U215	S5400A	INTEGRATED CIRCUIT V-18324		34
U216	S5490A	INTEGRATED CIRCUIT V-18324		35
U217	S5490A	INTEGRATED CIRCUIT V-18324		36
U218	S5492A	INTEGRATED CIRCUIT V-18324		37
U219	S5492A	INTEGRATED CIRCUIT V-18324		38
U220	S54123B	INTEGRATED CIRCUIT V-18324		39
U221	SN54174J	INTEGRATED CIRCUIT V-01295		40

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1211-A200	7124-4300-1	MEMORY COUNTER V-12115 (Cont)		
U222	SN54174J	INTEGRATED CIRCUIT V-01295		41
U223	SN5432J	INTEGRATED CIRCUIT V-01295		42
U224	S5410A	INTEGRATED CIRCUIT V-18324		43
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		44

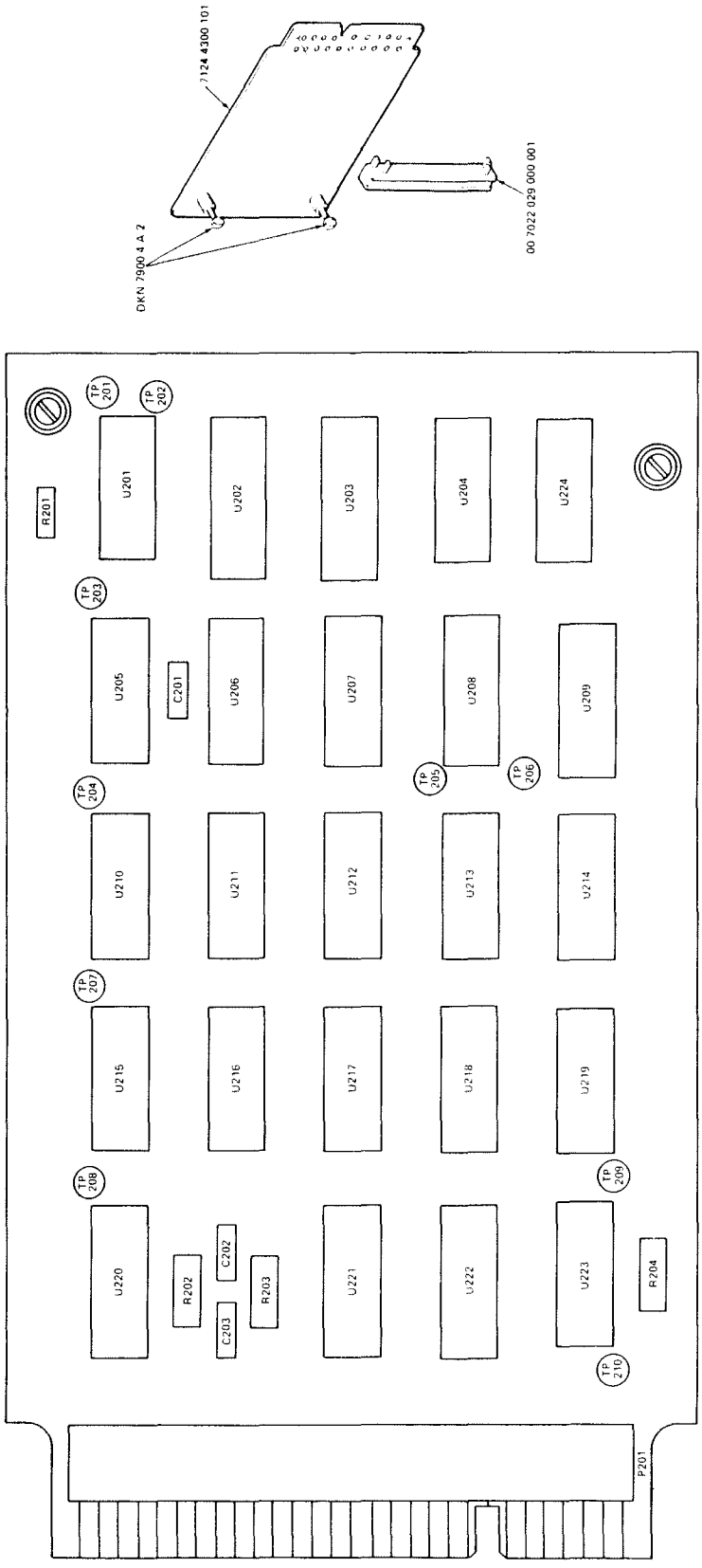


Figure 1211. Memory Counter

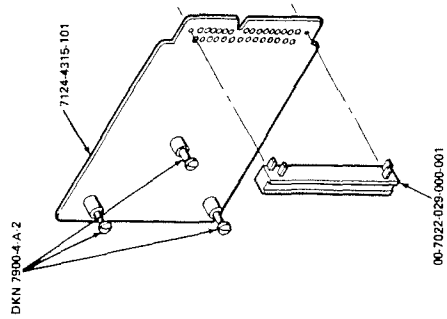
FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1212-A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115		1
C301	F330D1003F050	CAPACITOR, 0.1μF V-05397		2
C302	F330D1003F050	CAPACITOR, 0.1μF V-05397		3
C303	F330D1003F050	CAPACITOR, 0.1μF V-05397		4
C304	CK06BX104K	CAPACITOR, 0.1μF		5
C305	CK06BX104K	CAPACITOR, 0.1μF		6
C306	F330D1003F050	CAPACITOR, 0.1μF V-05397		7
C307	CK06BX104K	CAPACITOR, 0.1μF		8
C308	CK06BX104K	CAPACITOR, 0.1μF		9
C309	CK06BX104K	CAPACITOR, 0.1μF		10
C310	CK06BX104K	CAPACITOR, 0.1μF		11
C311	S106R-20	CAPACITOR, 10μF V-06751		12
C312	CK06BX103K	CAPACITOR, 0.01μF		13
C313	CK06BX105K	CAPACITOR, 1μF		14
C314	S226R-20	CAPACITOR, 22μF V-06751		15
C315	CD7-FA102J03	CAPACITOR, 0.001μF V-09023		16
C316	CD7-FA102J03	CAPACITOR, 0.001μF V-09023		17
C317	NG335R-10	CAPACITOR, 3.3μF V-06751		18
C318	NG335R-10	CAPACITOR, 3.3μF V-06751		19
C319	F330D1003F050	CAPACITOR, 0.1μF V-05397		20
C320	CD7-FA511J03	CAPACITOR, 510PF V-09023		21
C321	F330D1003F050	CAPACITOR, 0.1μF V-05397		22
C322	150D335X9035B2 or CS13BF335R (SPRAGUE ONLY)	CAPACITOR, 3.3μF V-56289		23

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1212-A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115 (Cont)		
C323	CK05BX100K	CAPACITOR, 10PF		24
C324	CK06BX104K	CAPACITOR, 0.1μF		25
C325	CK06BX104K	CAPACITOR, 0.1μF		26
C326	CK06BX682K	CAPACITOR, 0.0068μF		27
CR301	HP2800	DIODE V-28480		28
CR302	1N4148	DIODE		29
CR303	HP2800	DIODE V-28480		30
CR304	HP2800	DIODE V-28480		31
CR305	HP2800	DIODE V-28480		32
CR306	HP2800	DIODE V-28480		33
P301	00-7022-041-000-001	CONNECTOR V-91662		34
Q301	2N2907A	TRANSISTOR		35
Q302	2N930	TRANSISTOR		36
Q303	2N2222A	TRANSISTOR		37
R301	RCR07G100JS	RESISTOR		38
R302	RCR07G155JS	RESISTOR		39
R303	RCR07G274JS	RESISTOR		40
R304	3099P-1-102	RESISTOR, VARIABLE 1K V-80294		41
R305	RN60C1182F	RESISTOR		42
R306	RN60C1243F	RESISTOR		43
R307	RCR07G334JS	RESISTOR		44
R308	RCR07G334JS	RESISTOR		45
R309	RN60C2942F	RESISTOR		46
R310	3099P-1-500	RESISTOR, VARIABLE 50 OHMS V-80294		47
R311	RN60C5620F	RESISTOR		48
R312	RCR07G183JS	RESISTOR		49
R313	RCR07G183JS	RESISTOR		50

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1212-A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115 (Cont)		
R314	3099P-1-503	RESISTOR, VARIABLE 50K V-80294		51
R315	RN60C2263F	RESISTOR		52
R316	3099P-1-503	RESISTOR, VARIABLE 50K V-80294		53
R317	RCR07G104JS	RESISTOR		54
R318	RN60C1004F	RESISTOR		55
R319	RCR07G244JS	RESISTOR		56
R320	RCR07G105JS	RESISTOR		57
R321	RN60C2323F	RESISTOR		58
R322	RN60C4992F	RESISTOR		59
R323	RCR07G364JS	RESISTOR		60
R324	RN60C7502F	RESISTOR		61
R325	RN60C3323F	RESISTOR		62
R326	RCR07G244JS	RESISTOR		63
R327	RCR07G332JS	RESISTOR		64
R328	RN60C2492F	RESISTOR		65
R329	RCR07G682JS	RESISTOR		66
R330	RCR07G103JS	RESISTOR		67
R331	RCR07G332JS	RESISTOR		68
R332	RCR07G102JS	RESISTOR		69
R333	RCR07G103JS	RESISTOR		70
R334	RCR07G684JS	RESISTOR		71
R335	RN60C2103F	RESISTOR		72
R336	RN60C1073F	RESISTOR		73
R337	RN60C1073F	RESISTOR		74
R338	RCR07G564JS	RESISTOR		75
R339	RCR07G155JS	RESISTOR		76
R340	RCR07G224JS	RESISTOR		77
R341	RCR07G152JS	RESISTOR		78
R342	RCR07G683JS	RESISTOR		79
R343	RN60C2672F	RESISTOR		80
R344	RN60C4992F	RESISTOR		81
R345	RN60C2492F	RESISTOR		82
R346	RCR07G682JS	RESISTOR		83
R347	RN60C1651F	RESISTOR		84
R348	RN60C1432F	RESISTOR		85

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1212-A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115 (Cont)		
R349	RN60C5901F	RESISTOR		86
R350	RCR07G101JS	RESISTOR		87
R351	RCR07G101JS	RESISTOR		88
R352	RN60C4421F	RESISTOR		89
R353	RN60C2152F	RESISTOR		90
R354	RN60C4021F	RESISTOR		91
R355	RN60C2672F	RESISTOR		92
R356	RCR07G101JS	RESISTOR		93
R357	RCR07G244JS	RESISTOR		94
R358	RN60C7502F	RESISTOR		95
R359	RCR07G104JS	RESISTOR		96
TP301	016-4005-BRN	TEST POINT V-98291		97
TP302	016-4005-RED	TEST POINT V-98291		98
TP303	016-4005-ORN	TEST POINT V-98291		99
TP304	016-4005-YEL	TEST POINT V-98291		100
TP305	016-4005-GRN	TEST POINT V-98291		101
TP306	016-4005-BLU	TEST POINT V-98291		102
TP307	016-4005-VIO	TEST POINT V-98291		103
TP308	016-4005-GRA	TEST POINT V-98291		104
TP309	016-4005-WHT	TEST POINT V-98291		105
TP310	016-4005-BLK	TEST POINT		106
U301	U6W7747312	INTEGRATED CIRCUIT V-34335		107
U302	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		108
U303	LM106H	INTEGRATED CIRCUIT V-27014		109

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1212-A300	7124-4315-1	DIGITAL VIDEO SIGNAL PROCESSOR V-12115 (Cont)		
U304	LM106H	INTEGRATED CIRCUIT V-27014		110
U305	U6W7747312	INTEGRATED CIRCUIT V-34335		111
U306	U6W7747312	INTEGRATED CIRCUIT V-34335		112
U307	AH0014D	INTEGRATED CIRCUIT V-27014		113
U308	S54123B	INTEGRATED CIRCUIT V-18324		114
U309	AH0015D	INTEGRATED CIRCUIT V-27014		115
U310	U6W7747312	INTEGRATED CIRCUIT V-34335		116
U311	U6W7747312	INTEGRATED CIRCUIT V-34335		117
U312	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		118
U313	U6W7747312	INTEGRATED CIRCUIT V-34335		119
U314	NH0005	INTEGRATED CIRCUIT V-27014		120
U315	LM106H	INTEGRATED CIRCUIT V-27014		121
U316	S54H04A	INTEGRATED CIRCUIT V-18324		122
	10034N	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		123
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		124



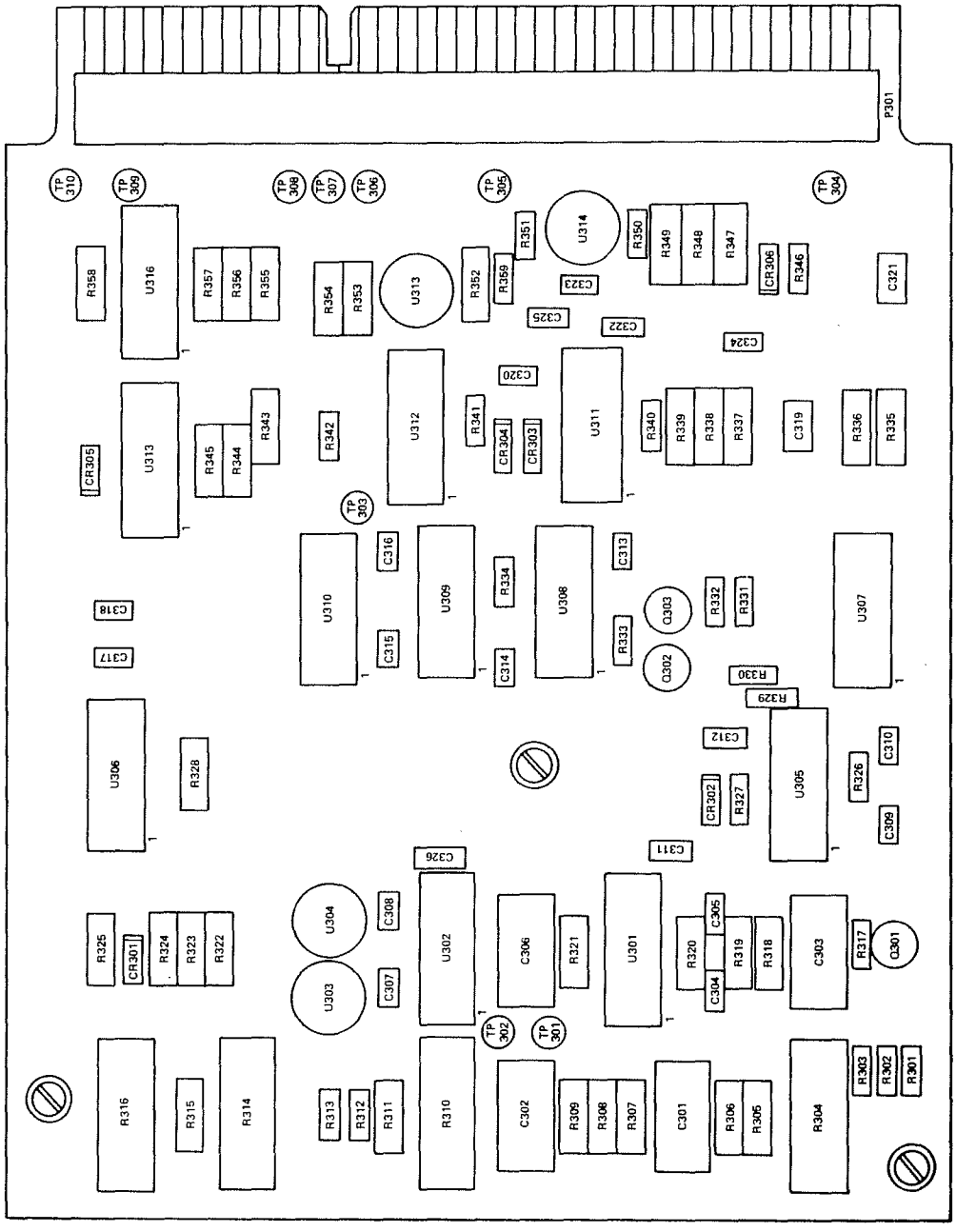


Figure 1212. Digital Video Signal Processor

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1213-A400	7124-4310-1	REFERENCE COUNTER V-12115		1
C401	CK06BX104K	CAPACITOR, 0.1μF		2
C402	CK06BX104K	CAPACITOR, 0.1μF		3
C403	S685R-20	CAPACITOR, 6.8μF V-56289		4
C404	CK06BX104K	CAPACITOR, 0.1μF		5
C405	CK06BX105K	CAPACITOR, 1μF		6
C406	F330A1002F050	CAPACITOR, 0.01μF V-05397		7
C407	CK06BX104K	CAPACITOR, 0.1μF		8
CR401	1N4148	DIODE		9
P401	00-7022-041-000-001	CONNECTOR V-91662		10
R401	RCR07G103JS	RESISTOR		11
R402	RN60C3011F	RESISTOR		12
R403	RN60C1001F	RESISTOR		13
R404	RCR07G335JS	RESISTOR		14
R405	RCR07G104JS	RESISTOR		15
R406	RCR07G335JS	RESISTOR		16
R407	RN60C4752F	RESISTOR		17
R408	RN60C4752F	RESISTOR		18
R409	RCR07G332JS	RESISTOR		19
R410	RCR07G102JS	RESISTOR		20
TP401	016-4005-BRN	TEST POINT V-98291		21
TP402	016-4005-RED	TEST POINT V-98291		22
TP403	016-4005-ORN	TEST POINT V-98291		23
TP404	016-4005-YEL	TEST POINT V-98291		24
TP405	016-4005-GRN	TEST POINT V-98291		25
TP406	016-4005-BLU	TEST POINT V-98291		26

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1213-A400	7124-4310-1	REFERENCE COUNTER V-12115 (Cont)		
TP407	016-4005-VIO	TEST POINT V-98291		27
TP408	016-4005-GRA	TEST POINT V-98291		28
TP409	016-4005-WHT	TEST POINT V-98291		29
TP410	016-4005-BLK	TEST POINT V-98291		30
U401	LM9100	INTEGRATED CIRCUIT V-90634		31
U402	U6A7741312	INTEGRATED CIRCUIT V-07263		32
U403	LM9103	INTEGRATED CIRCUIT V-90634		33
U404	S5474A	INTEGRATED CIRCUIT V-18324		34
U405	S5410A	INTEGRATED CIRCUIT V-18324		35
U406	S5402A	INTEGRATED CIRCUIT V-18324		36
U407	S5493A	INTEGRATED CIRCUIT V-18324		37
U408	S5400A	INTEGRATED CIRCUIT V-18324		38
U409	S5474A	INTEGRATED CIRCUIT V-18324		39
U410	S5486A	INTEGRATED CIRCUIT V-18324		40
U411	S5474A	INTEGRATED CIRCUIT V-18324		41
U412	S5490A	INTEGRATED CIRCUIT V-18324		42
U413	S5490A	INTEGRATED CIRCUIT V-18324		43
U414	S5490A	INTEGRATED CIRCUIT V-18324		44

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1213 A400	7124-4310-1	REFERENCE COUNTER V-12115 (Cont)		
U415	S5490A	INTEGRATED CIRCUIT V-18324		45
U416	S5490A	INTEGRATED CIRCUIT V-18324		46
U417	S8242A	INTEGRATED CIRCUIT V-18324		47
U418	SN54174J	INTEGRATED CIRCUIT V-01295		48
U419	S8242A	INTEGRATED CIRCUIT V-18324		49
U420	SN54174J	INTEGRATED CIRCUIT V-01295		50
U421	S8242A	INTEGRATED CIRCUIT V-18324		51
U422	S5404A	INTEGRATED CIRCUIT V-18324		52
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		53

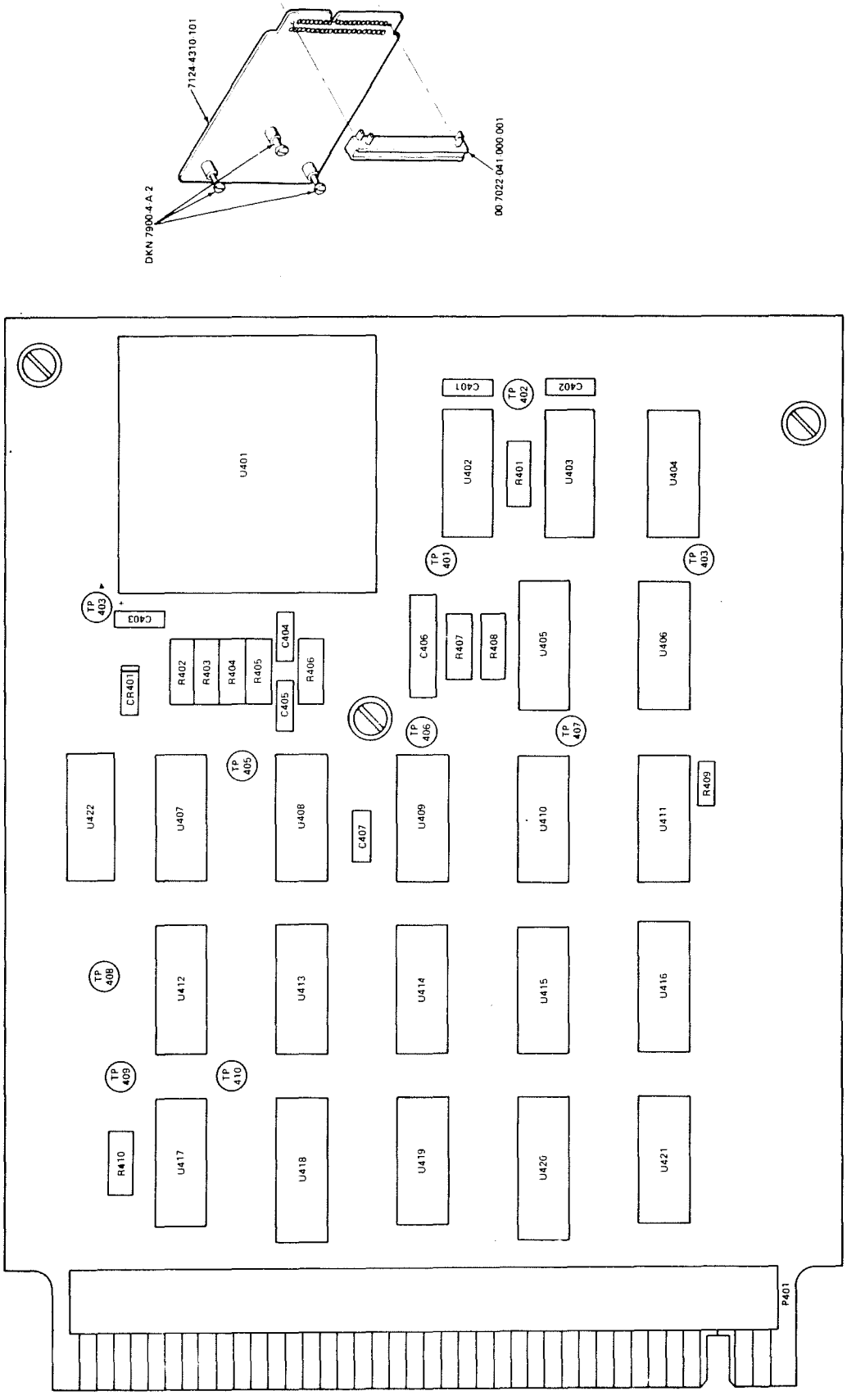


Figure 1213. Reference Counter

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1214				
A500	7124-4320-2	PULSE GROUP DECODER V-12115		1
C501	CK06BX105K	CAPACITOR		2
C502	CK06BX153K	CAPACITOR		3
C503	CK06BX153K	CAPACITOR		4
P501	00-7022-029-000-001	CONNECTOR V-91662		5
R501	RCR07G223JS	RESISTOR		6
R502	RCR07G223JS	RESISTOR		7
R503	RCR07G682JS	RESISTOR		8
R504	RCR07G332JS	RESISTOR		9
R505	RCR07G103JS	RESISTOR		10
R506	RCR07G223JS	RESISTOR		11
TP501	016-4005-BRN	TEST POINT V-98291		12
TP502	016-4005-RED	TEST POINT V-98291		13
TP503	016-4005-ORG	TEST POINT V-98291		14
TP504	016-4005-YEL	TEST POINT V-98291		15
TP505	016-4005-GRN	TEST POINT V-98291		16
TP506	016-4005-BLU	TEST POINT V-98291		17
TP507	016-4005-VIO	TEST POINT V-98291		18
TP508	016-4005-GRA	TEST POINT V-98291		19
TP509	016-4005-WHT	TEST POINT V-98291		20
TP510	016-4005-BLK	TEST POINT V-98291		21
U501	S5400A	INTEGRATED CIRCUIT V-18324		22
U502	S5402A	INTEGRATED CIRCUIT V-18324		23

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1214-A500	7124-4320-2	PULSE GROUP DECODER V-12115 (Cont)		
U503	S54157B	INTEGRATED CIRCUIT V-18324		24
U504	S54H08	INTEGRATED CIRCUIT V-18324		25
U505	S5474A	INTEGRATED CIRCUIT V-18324		26
U506	S54164A	INTEGRATED CIRCUIT V-18324		27
U507	S54164A	INTEGRATED CIRCUIT V-18324		28
U508	S54164A	INTEGRATED CIRCUIT V-18324		29
U509	S54164A	INTEGRATED CIRCUIT V-18324		30
U510	S5493A	INTEGRATED CIRCUIT V-18324		31
U511	S5493A	INTEGRATED CIRCUIT V-18324		32
U512	S5402A	INTEGRATED CIRCUIT V-18324		33
U513	S5410A	INTEGRATED CIRCUIT V-18324		34
U514	S5402A	INTEGRATED CIRCUIT V-18324		35
U515	S5474A	INTEGRATED CIRCUIT V-18324		36
U516	S5474A	INTEGRATED CIRCUIT V-18324		37
U517	S5400A	INTEGRATED CIRCUIT V-18324		38
U518	S5490A	INTEGRATED CIRCUIT V-18324		39
U519	S5474A	INTEGRATED CIRCUIT V-18324		40
U520	S5400A	INTEGRATED CIRCUIT V-18324		41

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1214-A500	7124-4320-2	PULSE GROUP DECODER V-12115 (Cont)		
U521	S54123B	INTEGRATED CIRCUIT V-18324		42
U522	C0-238A-1	INTEGRATED CIRCUIT, 4.0 MHZ V-27802		43
U523	S5474A	INTEGRATED CIRCUIT V-18324		44
U524	S54123B	INTEGRATED CIRCUIT V-18324		45
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		46

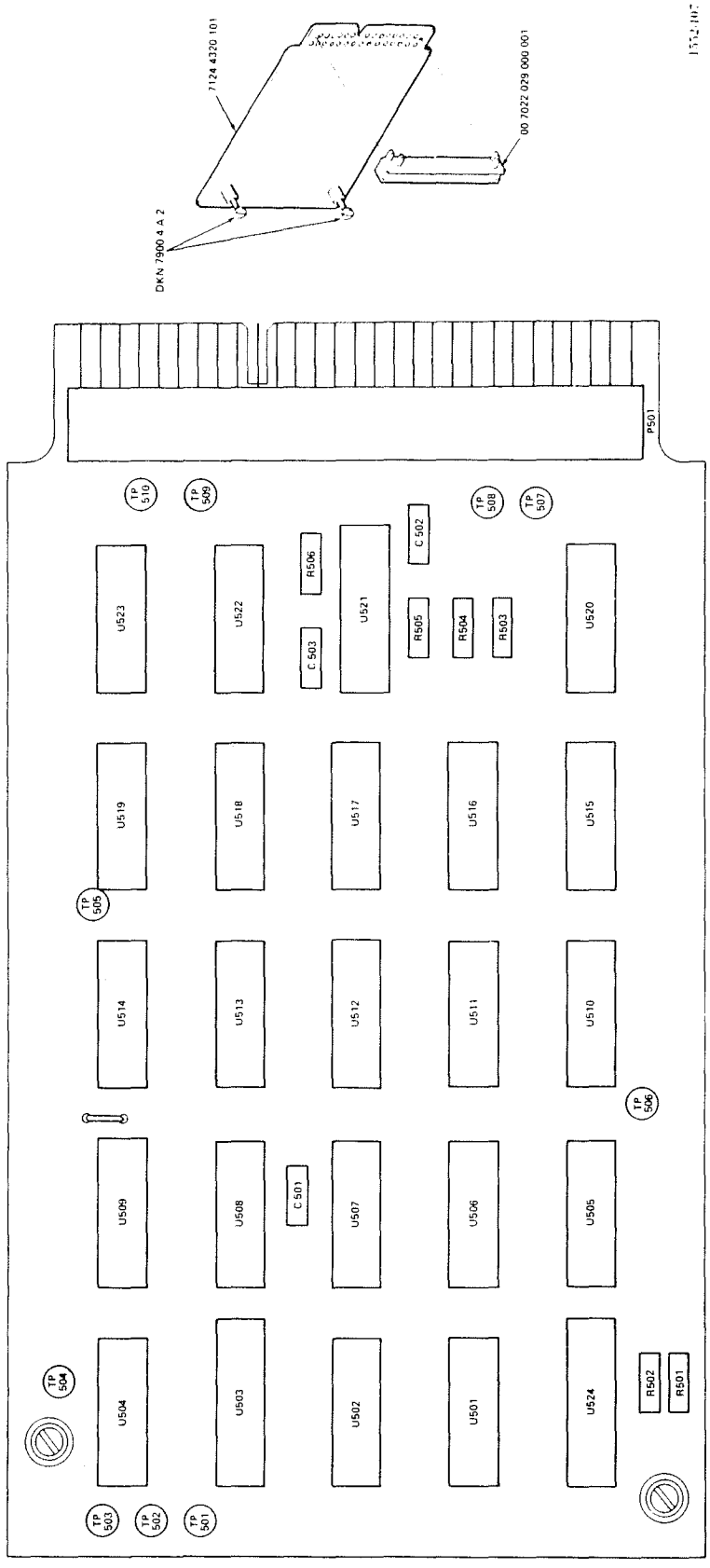


Figure 1214. Pulse Group Decoder

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1215-A600	7124-4305-1	DIGITAL BEARING UNIT MONITOR V-12115		1
C601	S226R-20	CAPACITOR, 22μF V-06751		2
C602	S226R-20	CAPACITOR, 22μF V-06751		3
C603	S226R-20	CAPACITOR, 22μF V-06751		4
C604	CK06BX105K	CAPACITOR, 1μF		5
C605	CK06BX104K	CAPACITOR, 0.1μF		6
C606	CK06BX105K	CAPACITOR, 1μF		7
C607	CK06BX104K	CAPACITOR, 0.1μF		8
C608	CK06BX104K	CAPACITOR, 0.1μF		9
C609	CK06BX104K	CAPACITOR, 0.1μF		10
C610	CK06BX104K	CAPACITOR, 0.1μF		11
C611	NS106R-10	CAPACITOR, 10μF V-06751		12
CR601	1N4148	DIODE		13
CR602	1N4148	DIODE		14
CR603	1N4148	DIODE		15
CR604	1N4148	DIODE		16
CR605	1N4148	DIODE		17
CR606	1N4148	DIODE		18
CR607	1N4148	DIODE		19
CR608	1N4148	DIODE		20
CR609	HP2800	DIODE V-28480		21
CR610	HP2800	DIODE V-28480		22
CR611	1N4148	DIODE		23
CR612	1N4148	DIODE		24
CR613	1N4148	DIODE		25
CR614	1N4148	DIODE		26
CR615	1N4148	DIODE		27
P601	00-7022-017-000-001	CONNECTOR V-91662		28
Q601	MPS-A13	TRANSISTOR V-04713		29

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1215-A600	7124-4305-1	DIGITAL BEARING UNIT MONITOR V-12115 (Cont)		
R601	RCR07G122JS	RESISTOR		30
R602	RCR07G332JS	RESISTOR		31
R603	RCR07G223JS	RESISTOR		32
R604	RCR07G223JS	RESISTOR		33
R605	RCR07G223JS	RESISTOR		34
R606	RCR07G331JS	RESISTOR		35
R607	RCR07G332JS	RESISTOR		36
R608	RN55E5901B	RESISTOR		37
R609	RN55E4121B	RESISTOR		38
R610	RN55E1002B	RESISTOR		39
R611	RCR07G332JS	RESISTOR		40
R612	RCR07G334JS	RESISTOR		41
R613	RCR07G223JS	RESISTOR		42
R614	RN55C2001F	RESISTOR		43
R615	RCR07G101JS	RESISTOR		44
R616	RN55C2001F	RESISTOR		45
R617	RN55C1000F	RESISTOR		46
R618	RCR07G103JS	RESISTOR		47
R619	RCR07G105JS	RESISTOR		48
U601	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		49
U602	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		50
U603	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		51
U604	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		52
U605	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		53
U606	S54123B	INTEGRATED CIRCUIT V-18324		54
U607	S54123B	INTEGRATED CIRCUIT V-18324		55
U608	U6A7749312	INTEGRATED CIRCUIT V-28584		56

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1215-A600	7124-4305-1	DIGITAL BEARING UNIT MONITOR V-12115 (Cont)		
U609	U6W7747312	INTEGRATED CIRCUIT V-34335		57
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		58

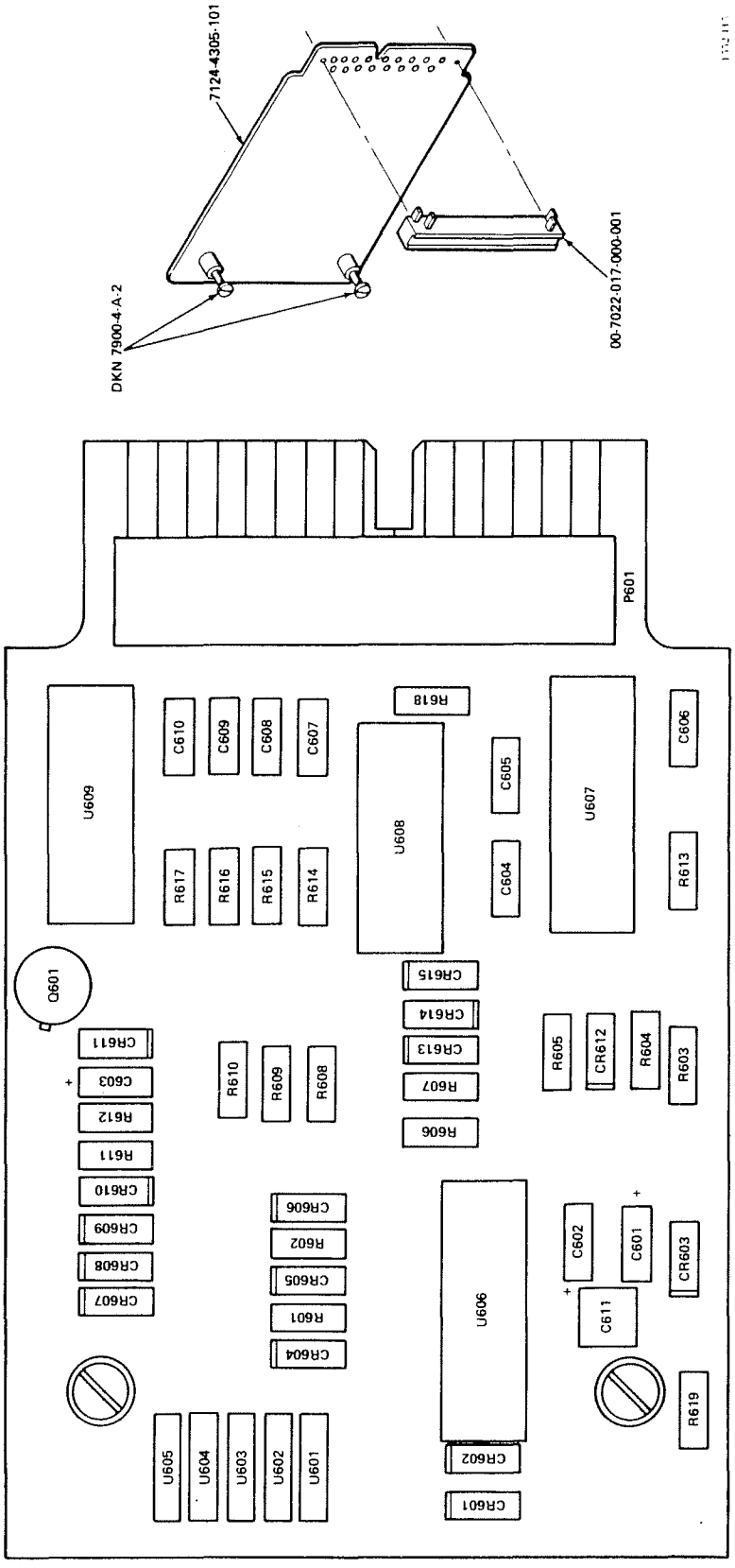


Figure 1215. Digital Bearing Unit Monitor (7124-4305-1)

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1216-A600	7124-4305-2	DIGITAL BEARING UNIT MONITOR V-12115		1
P601	00-7022-017-000-001	CONNECTOR V-91662		2
Q601	MPS-A13	TRANSISTOR V-04713		3
Q602	2N2222	TRANSISTOR		4
R601	RCR07G122JS	RESISTOR		5
R602	RCR07G332JS	RESISTOR		6
R603	RCR07G223JS	RESISTOR		7
R604	RCR07G223JS	RESISTOR		8
R605	RCR07G223JS	RESISTOR		9
R606	RCR07G331JS	RESISTOR		10
R607	RCR07G332JS	RESISTOR		11
R608	RN55E5901B	RESISTOR		12
R609	RN55E4121B	RESISTOR		13
R610	RN55E1002B	RESISTOR		14
R611	RCR07G332JS	RESISTOR		15
R612	RCR07G334JS	RESISTOR		16
R613	RCR07G223JS	RESISTOR		17
R614	RN55C2001F	RESISTOR		18
R615	RCR07G101JS	RESISTOR		19
R616	RN55C2001F	RESISTOR		20
R617	RN55C1000F	RESISTOR		21
R618	RCR07G103JS	RESISTOR		22
R619	RCR07G105JS	RESISTOR		23
R620	RCR07G103JS	RESISTOR		24
U601	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		25
U602	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		26
U603	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		27
U604	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		28
U605	SC6250-0021-1	DIODE, LIGHT EMITTING V-12115		29

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1216-A600	7124-4305-2	DIGITAL BEARING UNIT MONITOR V-12115 (Cont)		
U606	S54123B	INTEGRATED CIRCUIT V-18324		30
U607	S54123B	INTEGRATED CIRCUIT V-18324		31
U608	U6W7747312	INTEGRATED CIRCUIT V-34335		32
U609	U6W7747312	INTEGRATED CIRCUIT V-34335		33
	10034N	PAD, TRANSISTOR V-07047 V-12115 SPEC CONT DWG SC5975-0018-1		34

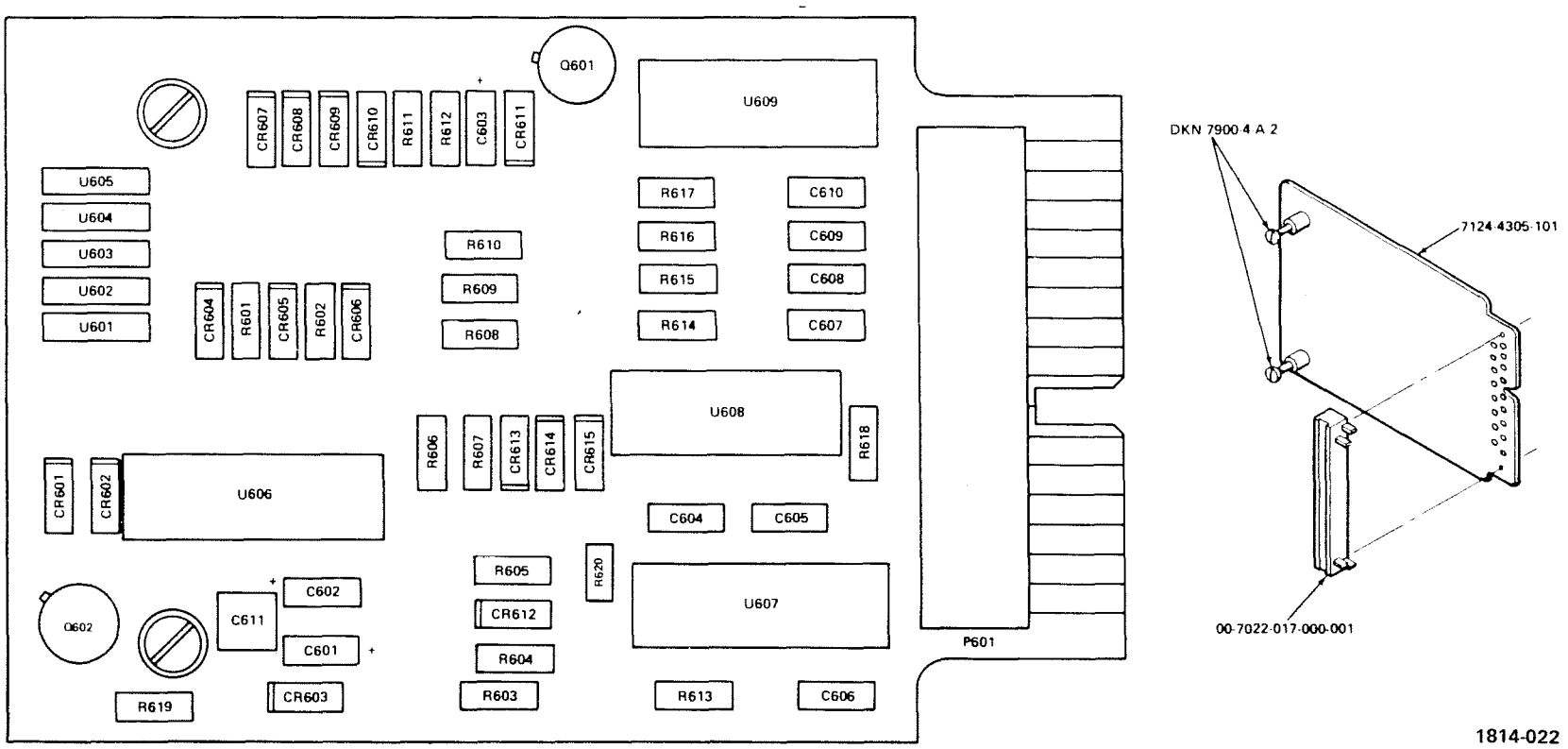


Figure 1216. Digital Bearing Unit Monitor (7124-4305-2)

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1217-	7124-0140-2	SIGNAL ANALYZER UNIT V-12115		1
A100	7109-3020-2	POWER SUPPLY REGULATOR, V-12115		2
A200	7124-1110-1 or 7124-1110-2	LIMIT DETECTOR V-12115		3
A300	7124-1105-1	SIGNAL PROCESSOR V-12115		4
C7301	602D402G015-AA2A	CAPACITOR, 4000 μF, 15VDC, V-56289		5
CR7301	680-1	DIODE, RECTIFIER V-12969		6
J101	00-7008-017-163-001	CONNECTOR V-91662		7
J201	00-7008-041-163-001	CONNECTOR V-91662		8
J301	00-7008-041-163-001	CONNECTOR V-91662		9
P7301	DPX2J-42226-26	CONNECTOR (See Figure 1205 for keying information) V-71468		10
Q7301	2N4231	TRANSISTOR V-07263		11
T7301	SC5950-0041-3	TRANSFORMER V-12115		12
	PK-11-66-M	INSULATOR KIT V-08289		13
	60-5006-34-14	POLARIZING KEY V-91662		14
	1488-4	SOLDER LUG V-83330		15
	1410-6	SOLDER LUG V-83330		16
	1410-10	SOLDER LUG V-83330		17
	MS21266-IN	GROMMET		18

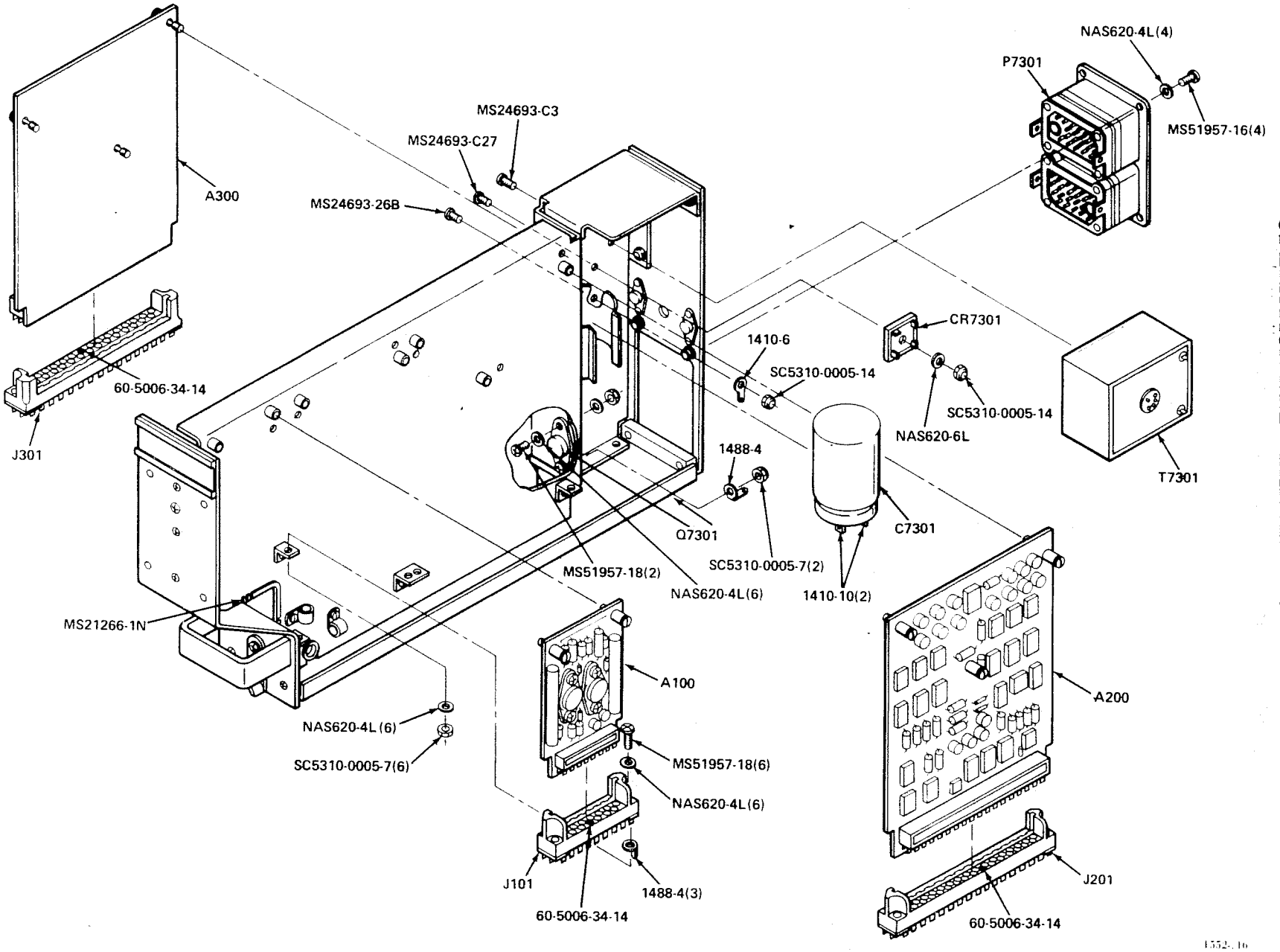


Figure 1217. Signal Analyzer Unit

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1218-	7006-0739-2	COVER, SAU V-12115		1
	7124-1011-1	MAIN FRAME V-12115		2
	7006-0732-3	FRONT PANEL V-12115		3
	7006-0733-3	REAR PANEL V-12115		4
	7006-0734-1	BOTTOM PLATE V-12115		5
	7124-3008-4	NAMEPLATE V-12115		6
	7006-0738-1	NAMEPLATE HOLDER V-12115		7
	7006-0737-1	MOUNTING BAR V-12115		8
	FCA9	HANDLE V-08730		9
	HDH-4	RETAINER HOOK V-94867		10
	3/16-4	CABLE LAMP, NYLON V-95987, V-12115 SPEC CONT DWG SC5325-0038-4		11
	D4-140	WASHER "D" CLAMP V-95987, V-12115 SPEC CONT DWG SC5325-0037-1		12
	92-1660-40	MINIATURE HEX NUT V-11117, V-12115 SPEC CONT DWG SC5310-0005-7		13
	97NM107-62	MINIATURE HEX NUT V-11117, V-12115 SPEC CONT DWG SC5310-0005-14		14

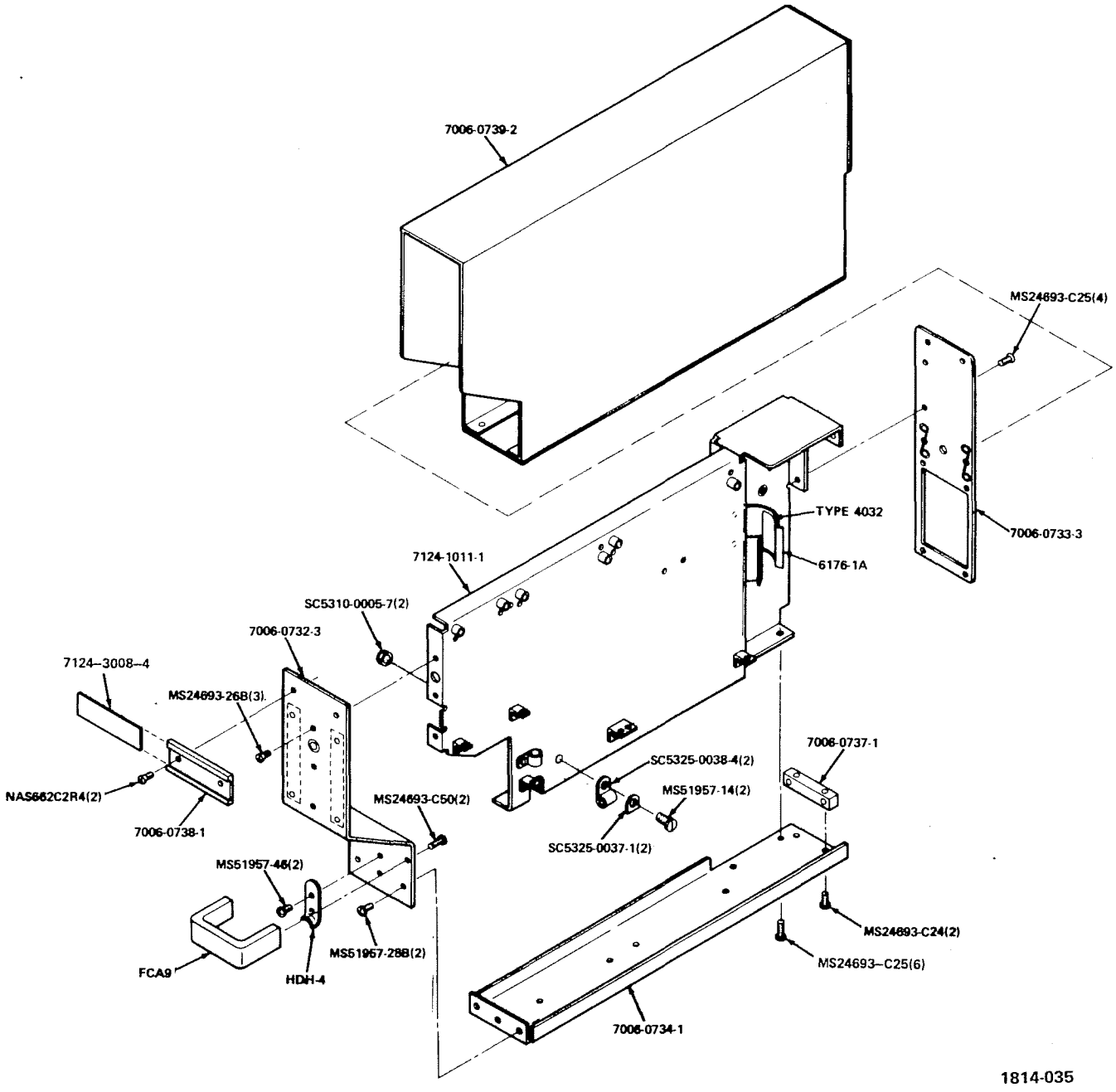


Figure 1218. Signal Analyzer Unit Cover and Main Frame

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1219-A100	7109-3020-2	POWER SUPPLY REGULATOR V-12115		1
C101	CK05BX102K	CAPACITOR, 0.001μF		2
C102	CK06BX104K	CAPACITOR, 0.1μF		3
C103	S106R-20	CAPACITOR, 10μF V-06751		4
C104	600D337-G030-DL4	CAPACITOR, 330μF V-56289		5
C105	600D337-G030-DL4	CAPACITOR, 330μF V-56289		6
C106	CK05BX102K	CAPACITOR, 0.001μF		7
C107	CK06BX104K	CAPACITOR, 0.1μF		8
C108	S106R-20	CAPACITOR, 10μF V-06751		9
CR101	1N4002	DIODE		10
CR102	1N4002	DIODE		11
CR103	1N4002	DIODE		12
CR104	1N4002	DIODE		13
CR105	1N4002	DIODE		14
P101	00-7022-017-000-001	CONNECTOR V-91662		15
Q101	2N2222A	TRANSISTOR		16
R101	RS1A	RESISTOR, 1.5 OHMS, ±3%, V-91637		17
R102	RN60C2322F	RESISTOR		18
R103	3099P-1-501	RESISTOR, VARIABLE, 500 OHMS V-80294		19
R104	RCR32G221JS	RESISTOR		20
R105	RN60C6811F	RESISTOR		21
R106	RS1A	RESISTOR, 2 OHMS, ±3% V-91637		22
R107	RN60C2322F	RESISTOR		23
R108	3099P-1-501	RESISTOR, VARIABLE, 500 OHMS V-80294		24
R109	RN60C6811F	RESISTOR		25
TP101	016-4005-BRN	TEST POINT V-98291		26

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1219-A100	7109-3020-2	POWER SUPPLY REGULATOR V-12115 (Cont)		
TP102	016-4005-RED	TEST POINT V-98291		27
TP103	016-4005-ORN	TEST POINT V-98291		28
TP104	016-4005-YEL	TEST POINT V-98291		29
TP105	016-4005-GRN	TEST POINT V-98291		30
U101	MC1569R	INTEGRATED CIRCUIT V-04713		31
U102	MC1563R	INTEGRATED CIRCUIT V-04713		32
VR101	1N4733	DIODE		33
	10034N	PAD, TRANSISTOR V-07047 V-12115 SPEC CONT DWG SC5975-0018-1		34
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		35
	68-1660-26	NUT, HEX, MINIATURE V-11117 V-12115 SPEC CONT DWG SC5310-0005-9		36

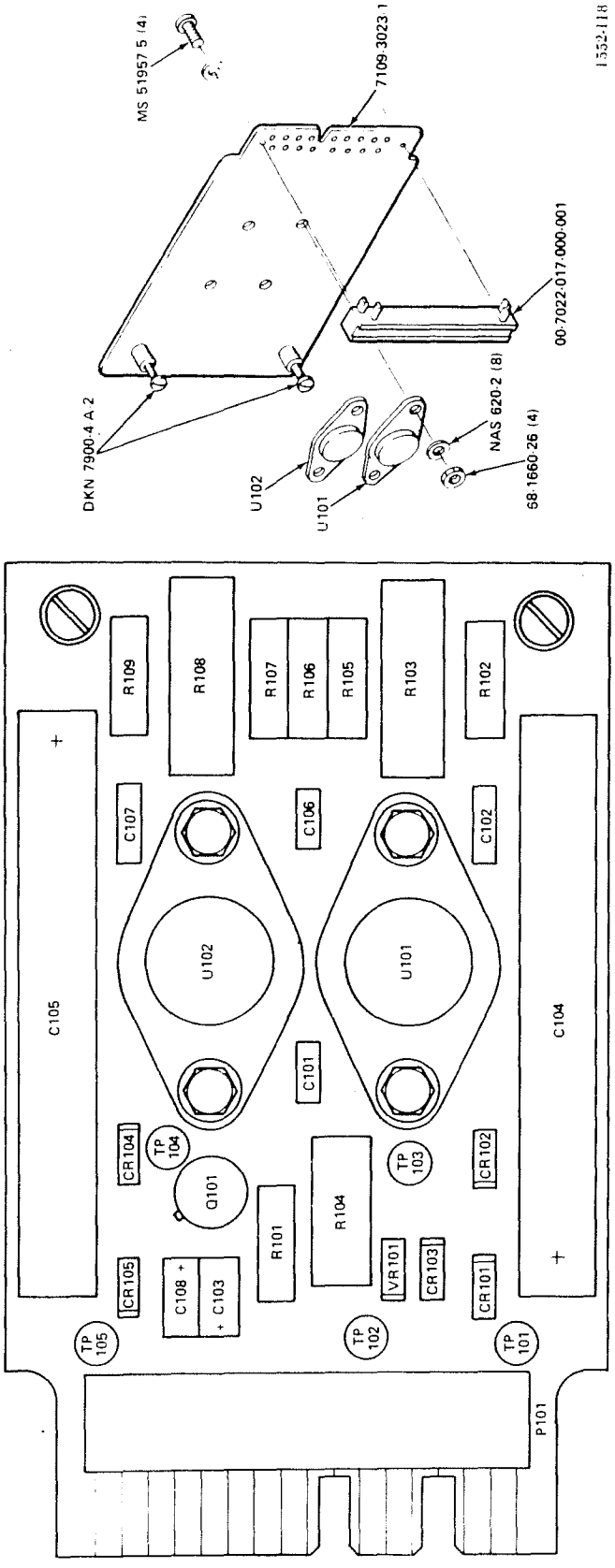


Figure 1219. Signal Analyzer Unit Power Supply Regulator

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1220-A200	7124-1110-1	LIMIT DETECTOR V-12115		1
C201	NG335R-10	CAPACITOR, 3.3μF V-06751		2
C202	NS106R-10	CAPACITOR, 10μF V-06751		3
C203	NG335R-10	CAPACITOR, 3.3μF V-06751		4
C204	NG335R-10	CAPACITOR, 3.3μF V-06751		5
C205	NG335R-10	CAPACITOR, 3.3μF V-06751		6
C206	NG335R-10	CAPACITOR, 3.3μF V-06751		7
C207	NS106R-10	CAPACITOR, 10μF V-06751		8
C208	CK06BX104K	CAPACITOR, 0.1μF		9
C209	CK06BX104K	CAPACITOR, 0.1μF		10
C210	CK06BX104K	CAPACITOR, 0.1μF		11
P201	00-7022-041-000-001	CONNECTOR V-91662		12
Q201	2N2222A	TRANSISTOR		13
Q202	2N2222A	TRANSISTOR		14
Q203	2N2222A	TRANSISTOR		15
Q204	2N2222A	TRANSISTOR		16
Q205	2N2222A	TRANSISTOR		17
Q206	2N2222A	TRANSISTOR		18
Q207	2N2222A	TRANSISTOR		19
Q208	2N2222A	TRANSISTOR		20
Q209	2N2222A	TRANSISTOR		21
Q210	2N2222A	TRANSISTOR		22
Q211	2N2222A	TRANSISTOR		23
Q212	2N2222A	TRANSISTOR		24
Q213	2N2222A	TRANSISTOR		25
Q214	2N2222A	TRANSISTOR		26
Q215	2N2907A	TRANSISTOR		27
Q216	2N2907A	TRANSISTOR		28
R201	3099P-1-203	RESISTOR, VARIABLE 20K V-80294		29

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1220-A200	7124-1110-1	LIMIT DETECTOR V-12115 (Cont)		
R202	RN60C6041F	RESISTOR		30
R203	RN60C4021F	RESISTOR		31
R204	RN60C8871F	RESISTOR		32
R205	RN60C2002F	RESISTOR		33
R206	RN60C1001F	RESISTOR		34
R207	RN60C3013F	RESISTOR		35
R208	RN60C3741F	RESISTOR		36
R209	RN60C4221F	RESISTOR		37
R210	RN60C1102F	RESISTOR		38
R211	RN60C8063F	RESISTOR		39
R212	RN60C1102F	RESISTOR		40
R213	RCR07G304JS	RESISTOR		41
R214	RN60C1302B	RESISTOR		42
R215	RN60C1301F	RESISTOR		43
R216	RN60C1302B	RESISTOR		44
R217	RN60C1821F	RESISTOR		45
R218	RN60C3013F	RESISTOR		46
R219	RCR07G304JS	RESISTOR		47
R220	RCR07G472JS	RESISTOR		48
R221	RCR07G472JS	RESISTOR		49
R222	RCR07G472JS	RESISTOR		50
R223	RCR07G472JS	RESISTOR		51
R224	RN60C4222F	RESISTOR		52
R225	RCR07G334JS	RESISTOR		53
R226	RCR07G334JS	RESISTOR		54
R227	RCR07G334JS	RESISTOR		55
R228	RCR07G334JS	RESISTOR		56
R229	RN60C1302B	RESISTOR		57
R230	RN60C6041F	RESISTOR		58
R231	RN60C4021F	RESISTOR		59
R232	RN60C1302B	RESISTOR		60
R233	RCR07G561JS	RESISTOR		61
R234	RCR07G561JS	RESISTOR		62
R235	RCR07G561JS	RESISTOR		63
R236	RCR07G561JS	RESISTOR		64
R237	RN60C4021F	RESISTOR		65
R238	RN60C6041F	RESISTOR		66
R239	RCR07G332JS	RESISTOR		67

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1220-A200	7124-1110-1	LIMIT DETECTOR V-12115 (Cont)		
TP201	016-4005-BRN	TEST POINT V-98291		68
TP202	016-4005-RED	TEST POINT V-98291		69
TP203	016-4005-ORN	TEST POINT V-98291		70
TP204	016-4005-YEL	TEST POINT V-98291		71
TP205	016-4005-GRN	TEST POINT V-98291		72
TP206	016-4005-BLU	TEST POINT V-98291		73
TP207	016-4005-VIO	TEST POINT V-98291		74
TP208	016-4005-GRA	TEST POINT V-98291		75
TP209	016-4005-WHT	TEST POINT V-98291		76
U201	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		77
U202	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		78
U203	U6A7749312	INTEGRATED CIRCUIT V-28584		79
U204	U6A7749312	INTEGRATED CIRCUIT V-28584		80
U205	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		81
U206	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		82
U207	U6A7749312	INTEGRATED CIRCUIT V-28584		83
U208	U6A7749312	INTEGRATED CIRCUIT V-28584		84
U209	U6W7747312	INTEGRATED CIRCUIT V-34335		85
U210	U6A7749312	INTEGRATED CIRCUIT V-28584		86

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1220-A200	7124-1110-1	LIMIT DETECTOR V-12115 (Cont)		
U211	U6A7749312	INTEGRATED CIRCUIT V-28584		87
U212	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		88
U213	S5474A	INTEGRATED CIRCUIT V-18324		89
U214	S5400A	INTEGRATED CIRCUIT V-18324		90
U215	SN5485	INTEGRATED CIRCUIT V-01295		91
U216	S5493A	INTEGRATED CIRCUIT V-18324		92
U217	SN5485	INTEGRATED CIRCUIT V-01295		93
U218	S5493A	INTEGRATED CIRCUIT V-18324		94
	10034	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		95
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		96

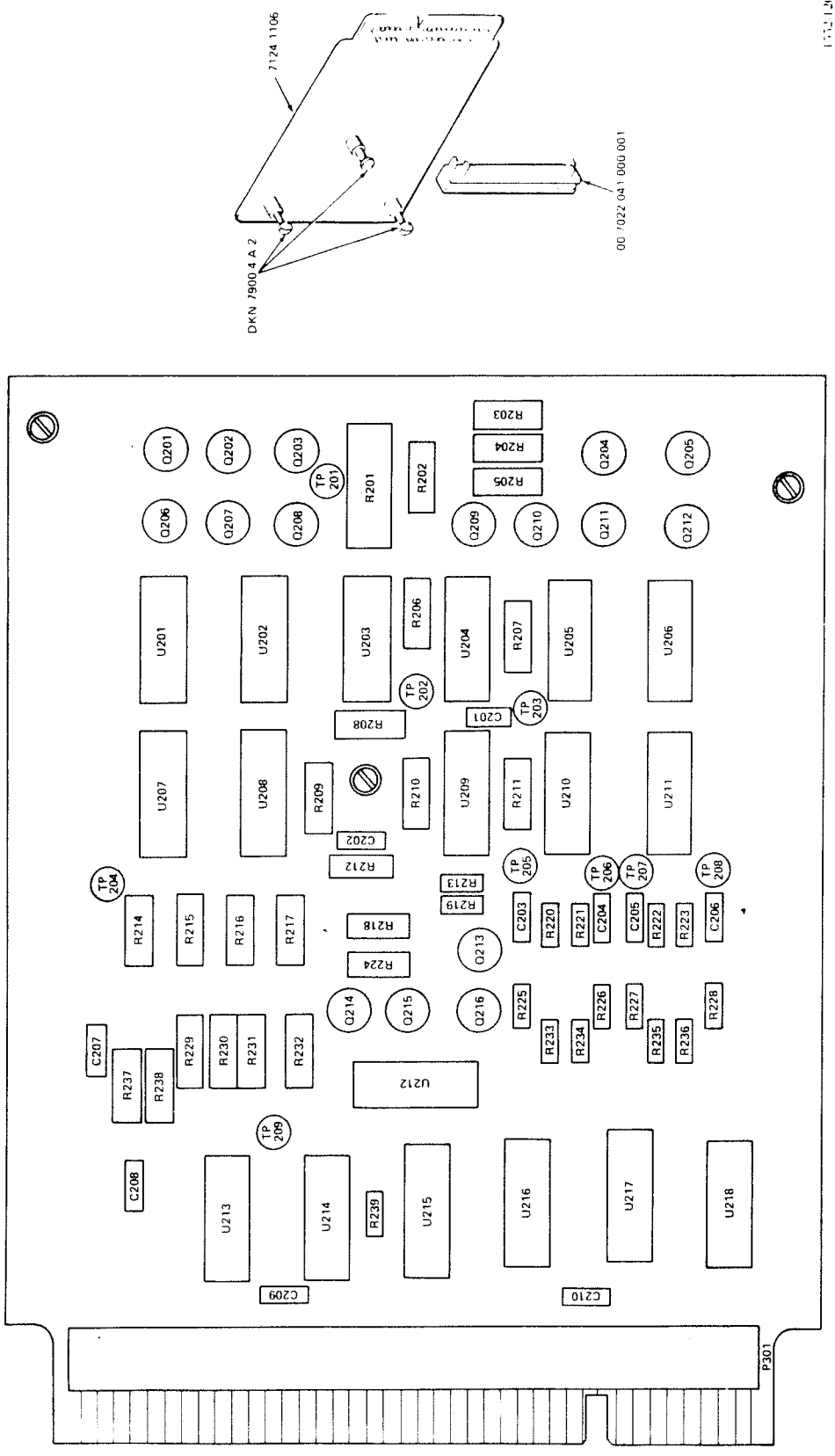


Figure 1220. Limit Detector (7124-1110-1)

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1221-A200	7124-1110-2	LIMIT DETECTOR V-12115		1
C201	NG335R-10	CAPACITOR, 3.3μF V-06751		2
C202	NS106R-10	CAPACITOR, 10μF V-06751		3
C203	NG335R-10	CAPACITOR, 3.3μF V-06751		4
C204	NG335R-10	CAPACITOR, 3.3μF V-06751		5
C205	NG335R-10	CAPACITOR, 3.3μF V-06751		6
C206	NG335R-10	CAPACITOR, 3.3μF V-06751		7
C207	NS106R-10	CAPACITOR, 10μF V-06751		8
C208	CK06BX104K	CAPACITOR, 0.1μF		9
C209	CK06BX104K	CAPACITOR, 0.1μF		10
C210	CK06BX104K	CAPACITOR, 0.1μF		11
P201	00-7022-041-000-001	CONNECTOR V-91662		12
Q201	2N2222A	TRANSISTOR		13
Q202	2N2222A	TRANSISTOR		14
Q203	2N2222A	TRANSISTOR		15
Q204	2N2222A	TRANSISTOR		16
Q205	2N2222A	TRANSISTOR		17
Q206	2N2222A	TRANSISTOR		18
Q207	2N2222A	TRANSISTOR		19
Q208	2N2222A	TRANSISTOR		20
Q209	2N2222A	TRANSISTOR		21
Q210	2N2222A	TRANSISTOR		22
Q211	2N2222A	TRANSISTOR		23
Q212	2N2222A	TRANSISTOR		24
Q213	2N2222A	TRANSISTOR		25
Q214	2N2222A	TRANSISTOR		26
Q215	2N2907A	TRANSISTOR		27
Q216	2N2907A	TRANSISTOR		28
R201	3099P-1-203	RESISTOR, VARIABLE 20K V-80294		29

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1221-A200	7124-1110-2	LIMIT DETECTOR V-12115 (Cont)		
R204	RN60C8871F	RESISTOR		30
R205	RN60C2002F	RESISTOR		31
R206	RN60C1501F	RESISTOR		32
R207	RN60C3013F	RESISTOR		33
R208	RN60C1102F	RESISTOR		34
R209	RN60C1102F	RESISTOR		35
R210	RN60C6341F	RESISTOR		36
R211	RN60C8063F	RESISTOR		37
R212	RN60C4751F	RESISTOR		38
R213	RCR07G304JS	RESISTOR		39
R214	RN60C1302B	RESISTOR		40
R215	RN60C3831F	RESISTOR		41
R216	RN60C1302B	RESISTOR		42
R217	RN60C5231F	RESISTOR		43
R218	RN60C3013F	RESISTOR		44
R219	RCR07G304JS	RESISTOR		45
R220	RCR07G472JS	RESISTOR		46
R221	RCR07G472JS	RESISTOR		47
R222	RCR07G472JS	RESISTOR		48
R223	RCR07G472JS	RESISTOR		49
R224	RN60C4222F	RESISTOR		50
R225	RCR07G334JS	RESISTOR		51
R226	RCR07G334JS	RESISTOR		52
R227	RCR07G334JS	RESISTOR		53
R228	RCR07G334JS	RESISTOR		54
R229	RN60C1302B	RESISTOR		55
R232	RN60C1302B	RESISTOR		56
R233	RCR07G561JS	RESISTOR		57
R234	RCR07G561JS	RESISTOR		58
R235	RCR07G561JS	RESISTOR		59
R236	RCR07G561JS	RESISTOR		60
R239	RCR07G332JS	RESISTOR		61

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1221-A200	7124-1110-2	LIMIT DETECTOR V-12115 (Cont)		
TP201	016-4005-BRN	TEST POINT V-98291		62
TP202	016-4005-RED	TEST POINT V-98291		63
TP203	016-4005-ORN	TEST POINT V-98291		64
TP204	016-4005-YEL	TEST POINT V-98291		65
TP205	016-4005-GRN	TEST POINT V-98291		66
TP206	016-4005-BLU	TEST POINT V-98291		67
TP207	016-4005-VIO	TEST POINT V-98291		68
TP208	016-4005-GRA	TEST POINT V-98291		69
TP209	016-4005-WHT	TEST POINT V-98291		70
U201	899-3-R2.2K	INTEGRATED CIRCUIT V-80740		71
U202	899-3-R4.7K	INTEGRATED CIRCUIT V-80740		72
U203	U6W7747312	INTEGRATED CIRCUIT V-28584		73
U204	U6W7747312	INTEGRATED CIRCUIT V-28584		74
U205	899-3-R2.2K	INTEGRATED CIRCUIT V-80740		75
U206	899-3-R4.7K	INTEGRATED CIRCUIT V-80740		76
U207	U6W7747312	INTEGRATED CIRCUIT V-28584		77
U208	U6W7747312	INTEGRATED CIRCUIT V-28584		78
U209	U6W7747312	INTEGRATED CIRCUIT V-34335		79
U210	U6W7747312	INTEGRATED CIRCUIT V-28584		80

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1221-A200	7124-1110-2	LIMIT DETECTOR V-12115 (Cont)		
U211	U6W7747312	INTEGRATED CIRCUIT V-28584		81
U212	899-3-R3.3K	INTEGRATED CIRCUIT V-80740		82
U213	S5474A	INTEGRATED CIRCUIT V-18324		83
U214	S5400A	INTEGRATED CIRCUIT V-18324		84
U215	SN5485	INTEGRATED CIRCUIT V-01295		85
U216	S5493A	INTEGRATED CIRCUIT V-18324		86
U217	SN5485	INTEGRATED CIRCUIT V-01295		87
U218	S5493A	INTEGRATED CIRCUIT V-18324		88
	10034	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		89
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		90

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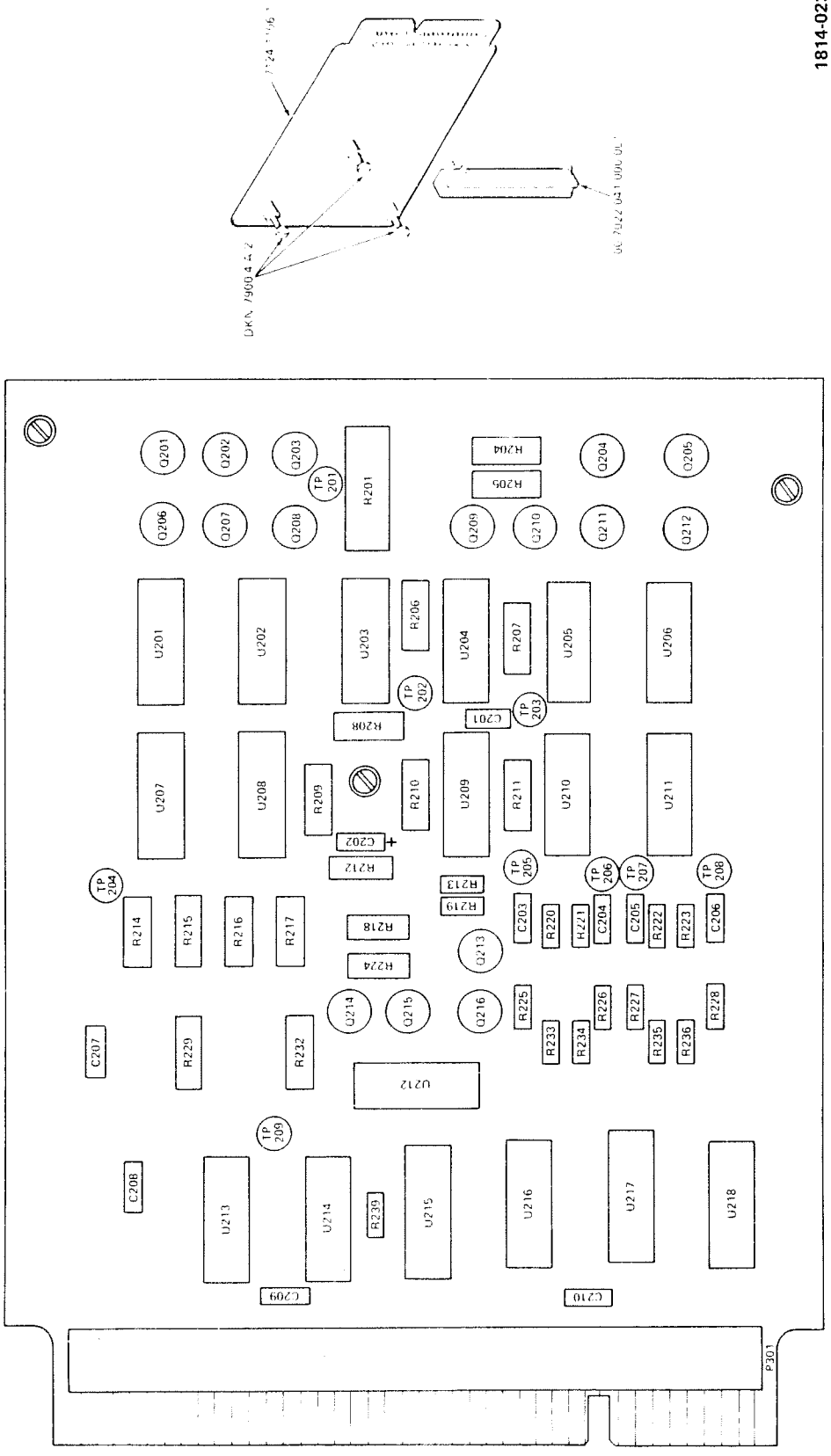


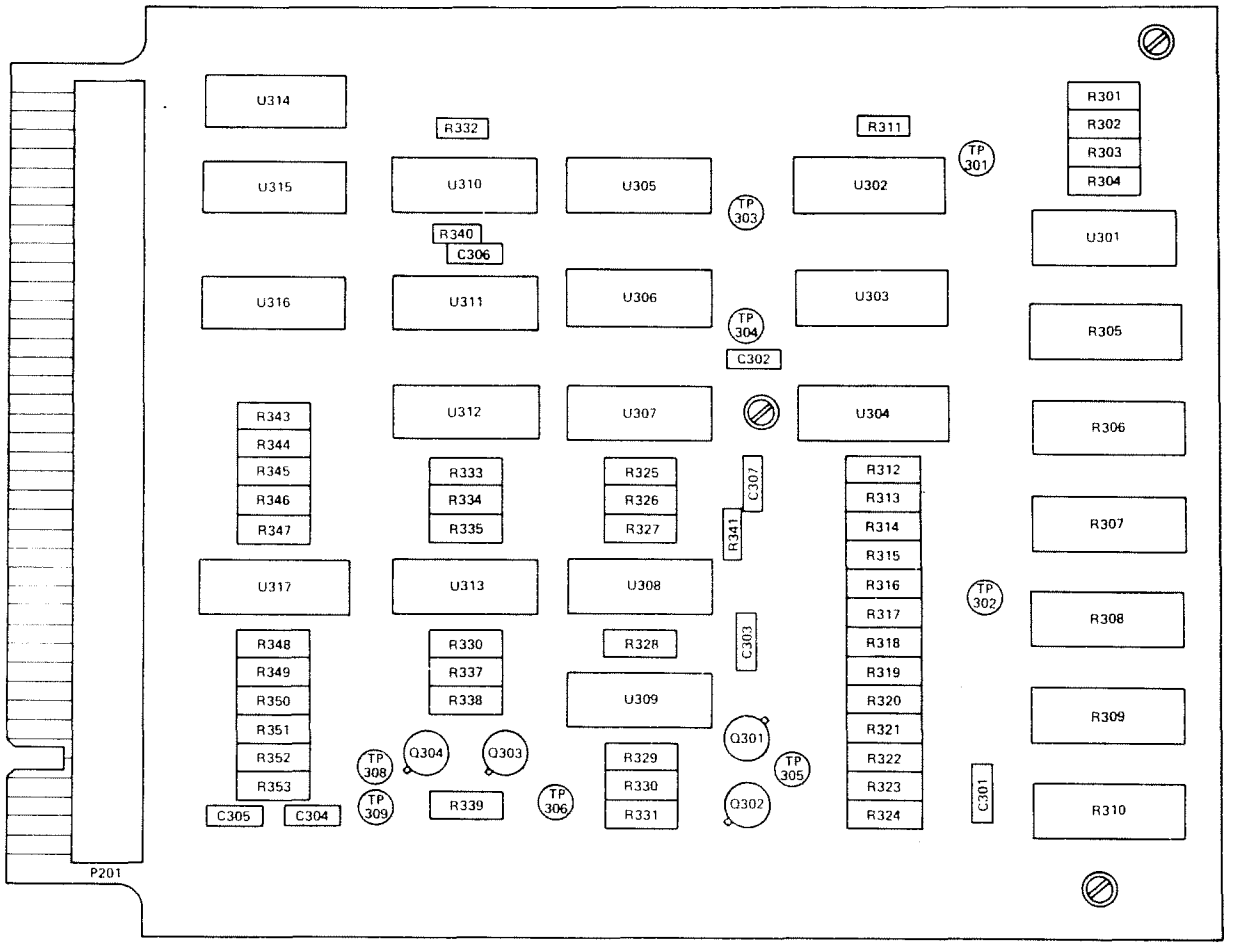
Figure 1221. Limit Detector (7124-1110-2)

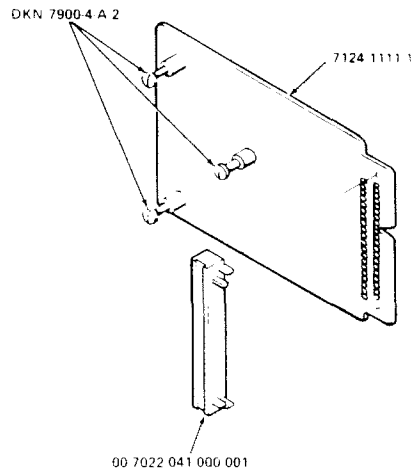
FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1222-A300	7124-1105-1	SIGNAL PROCESSOR V-12115		1
C301	NS335R-10	CAPACITOR, 3.3μF V-06751		2
C302	CK06BX104K	CAPACITOR, 0.1μF		3
C303	CK06BX104K	CAPACITOR, 0.1μF		4
C304	CK06BX104K	CAPACITOR, 0.1μF		5
C305	CK06BX104K	CAPACITOR, 0.1μF		6
C306	CK06BX103K	CAPACITOR, 0.01μF		7
C307	NG335R-10	CAPACITOR, 3.3μF V-06751		8
P301	00-7022-041-000-001	CONNECTOR V-91662		9
Q301	2N2222A	TRANSISTOR		10
Q302	2N2907A	TRANSISTOR		11
Q303	2N4392	TRANSISTOR		12
Q304	2N2907A	TRANSISTOR		13
R301	RN60C4993F	RESISTOR		14
R302	RN60C1821F	RESISTOR		15
R303	RN60C1243F	RESISTOR		16
R304	RN60C2493F	RESISTOR		17
R305	3099P-1-201	RESISTOR, VARIABLE, 200 OHM, V-80294		18
R306	3099P-1-201	RESISTOR, VARIABLE, 200 OHM, V-80294		19
R307	3099P-1-102	RESISTOR, VARIABLE, 1K, V-80294		20
R308	3099P-1-102	RESISTOR, VARIABLE, 1K, V-80294		21
R309	3099P-1-203	RESISTOR, VARIABLE, 20K, V-80294		22
R310	3099P-1-102	RESISTOR, VARIABLE, 1K, V-80294		23
R311	RCR07G332JS	RESISTOR		24
R312	RN60C1002B	RESISTOR		25
R313	RN60C8062F	RESISTOR		26
R314	RN60C1623F	RESISTOR		27
R315	RN60C3243F	RESISTOR		28
R316	RN60C6343F	RESISTOR		29

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1222-A300	7124-1105-1	SIGNAL PROCESSOR V-12115 (Cont)		
R317	RN60C4022F	RESISTOR		30
R318	RN60C1002B	RESISTOR		31
R319	RN60C1002B	RESISTOR		32
R320	RN60C1002B	RESISTOR		33
R321	RN60C1002B	RESISTOR		34
R322	RN60C1501F	RESISTOR		35
R323	RN60C3013F	RESISTOR		36
R324	RN60C1501F	RESISTOR		37
R325	RN60C1002F	RESISTOR		38
R326	RN60C4991F	RESISTOR		39
R327	RN60C5901F	RESISTOR		40
R328	RCR07G304JS	RESISTOR		41
R329	RN60C4643F	RESISTOR		42
R330	RCR07G332JS	RESISTOR		43
R331	RCR07G332JS	RESISTOR		44
R332	RCR07G332JS	RESISTOR		45
R333	RN60C1002F	RESISTOR		46
R334	RN60C4991F	RESISTOR		47
R335	RN60C9091F	RESISTOR		48
R336	RN60C1003B	RESISTOR		49
R337	RN60C1003B	RESISTOR		50
R338	RN60C1003B	RESISTOR		51
R339	RN60C6492F	RESISTOR		52
R340	RCR07G101JS	RESISTOR		53
R341	RCR07G304JS	RESISTOR		54
R343	RCR07G100JS	RESISTOR		55
R344	RN60C2492F	RESISTOR		56
R345	RN60C1002B	RESISTOR		57
R346	RN60C1002B	RESISTOR		58
R347	RN60C1002B	RESISTOR		59
R348	RN60C4992F	RESISTOR		60
R349	RN60C1003F	RESISTOR		61
R350	RN60C1002B	RESISTOR		62
R351	RN60C2491F	RESISTOR		63
R352	RCR07G104JS	RESISTOR		64
R353	RCR07G103JS	RESISTOR		65

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1222-A300	7124-1105-1	SIGNAL PROCESSOR V-12115 (Cont)		
TP301	016-4005-BRN	TEST POINT V-98291		66
TP302	016-4005-RED	TEST POINT V-98291		67
TP303	016-4005-ORN	TEST POINT V-98291		68
TP304	016-4005-YEL	TEST POINT V-98291		69
TP305	016-4005-GRN	TEST POINT V-98291		70
TP306	016-4005-BLU	TEST POINT V-98291		71
TP308	016-4005-GRA	TEST POINT V-98291		72
TP309	016-4005-WHT	TEST POINT V-98291		73
U301	S5406A	INTEGRATED CIRCUIT V-18324		74
U302	S5475B	INTEGRATED CIRCUIT V-18324		75
U303	S5475B	INTEGRATED CIRCUIT V-18324		76
U304	S5406A	INTEGRATED CIRCUIT V-18324		77
U305	S5493A	INTEGRATED CIRCUIT V-18324		78
U306	S5493A	INTEGRATED CIRCUIT V-18324		79
U307	S5474A	INTEGRATED CIRCUIT V-18324		80
U308	U6W7747312	INTEGRATED CIRCUIT V-34335		81
U309	U6W7747312	INTEGRATED CIRCUIT V-34335		82
U310	S5400A	INTEGRATED CIRCUIT V-18324		83
U311	S5404A	INTEGRATED CIRCUIT V-18324		84

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1222-A300	7124-1105-1	SIGNAL PROCESSOR V-12115 (Cont)		
U312	S5400A	INTEGRATED CIRCUIT V-18324		85
U313	U6W7747312	INTEGRATED CIRCUIT V-34335		86
U314	S5400A	INTEGRATED CIRCUIT V-18324		87
U315	S5474A	INTEGRATED CIRCUIT V-18324		88
U316	S5404A	INTEGRATED CIRCUIT V-18324		89
U317	S5406A	INTEGRATED CIRCUIT V-18324		90
	10034N	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		91
	DKN7900-4-A-2	SCREW, CAPTIVE V-08524		92





SIERRA RESEARCH CORPORATION

TTS-7124

Figure 1222. Signal Processor

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1223-	7124-0130-2	CONSOLE DISPLAY AND CONTROL PANEL UNIT V-12115		1
A100	7124-1600-1	LED DISPLAY V-12115		2
A200	7124-1605-1	LED LOGIC V-12115		3
A300	7124-1610-1	COURSE SELECT V-12115		4
C7401	602D402-G015-AA2A	CAPACITOR, 4000 μF 15VDC, V-56289		5
C7402	600D107-G030-DE4	CAPACITOR, 100 μF 30VDC, V-56289		6
C7403	CK06BX105K	CAPACITOR, 1 μF		7
CR7401	680-1	DIODE, RECTIFIER V-12969		8
CR7402	680-1	DIODE, RECTIFIER V-12969		9
J7401	2DD100S	CONNECTOR V-71468		10
P301	00-7008-017-163-001	CONNECTOR V-91662		11
Q7401	SG109K	TRANSISTOR V-34333		12
S7401	MS24656-231	SWITCH, DPDT		13
S7402	MS24656-231	SWITCH, DPDT		14
S7403	MS24656-231	SWITCH, DPDT		15
S7404	MS24656-231	SWITCH, DPDT		16
S7405	MS24656-231	SWITCH, DPDT		17
S7406	MS24656-231	SWITCH, DPDT		18
T7401	SC5950-0041-4	TRANSFORMER V-12115		19
	49-4159	TOGGLE COVER V-27193		20
	8-S-634	SWITCH, THUMBWHEEL V-07126		21

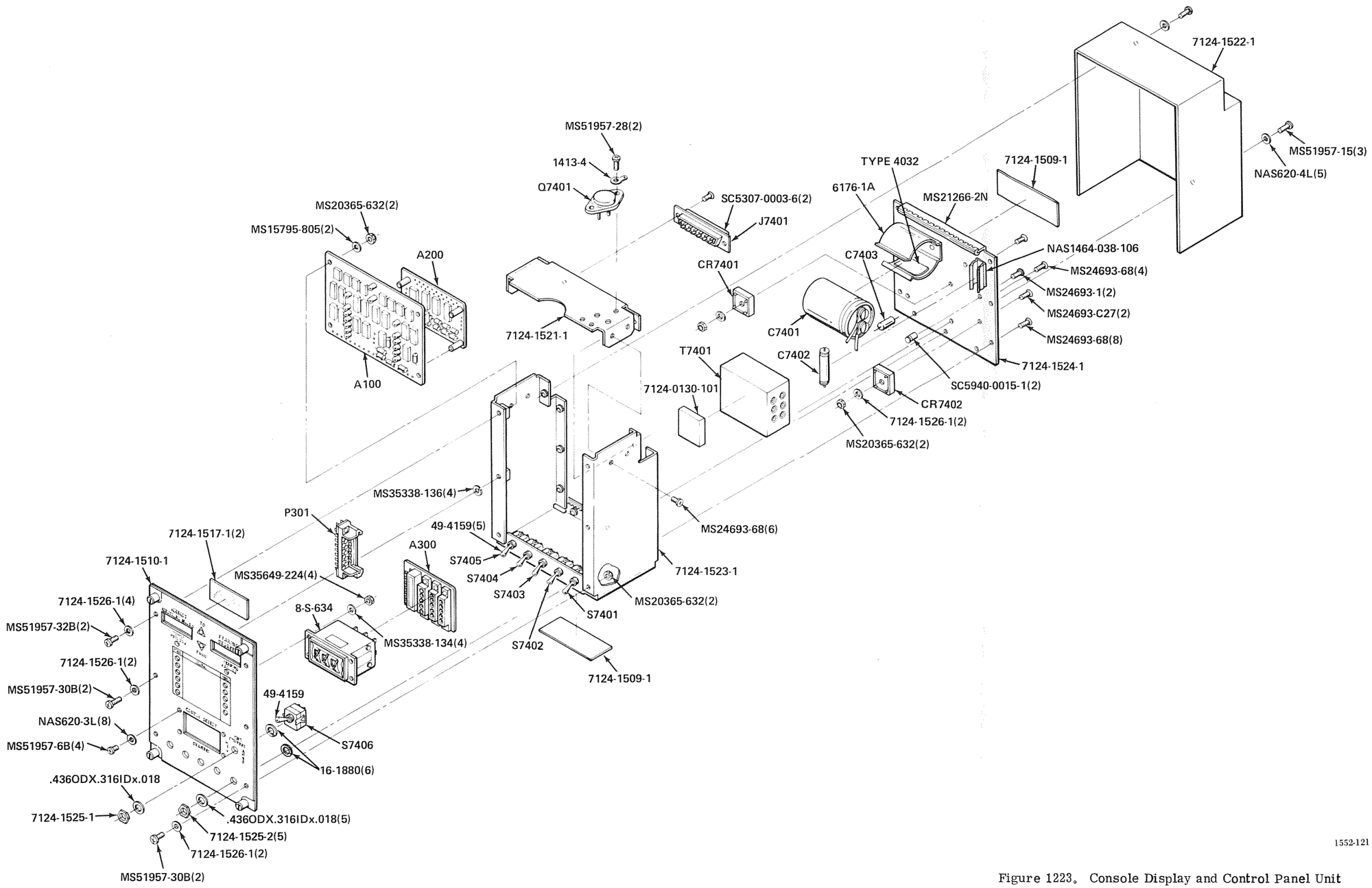


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Figure 1223. Console Display and Control Panel Unit

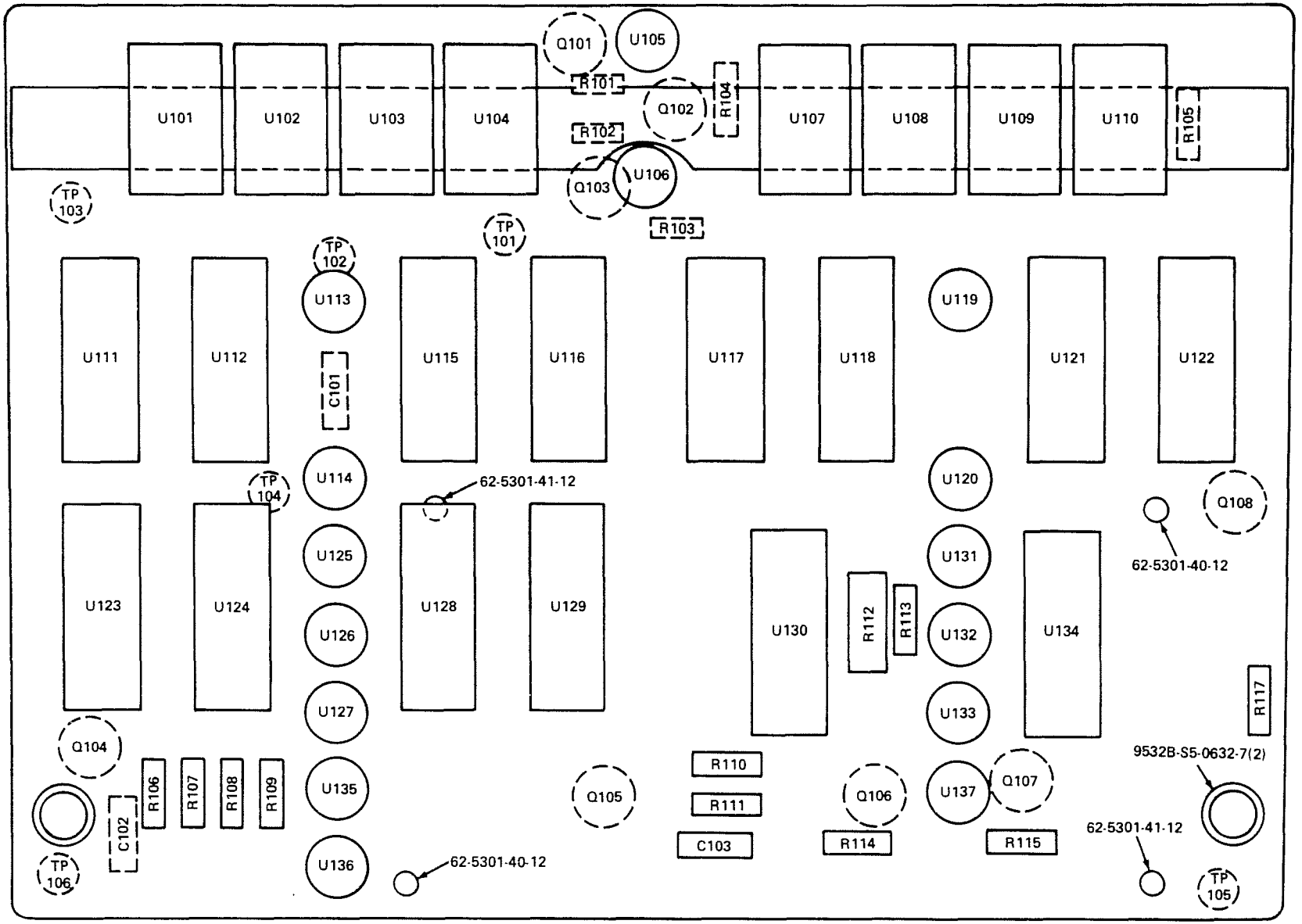
FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1223-	7124-0130-2	CONSOLE DISPLAY AND CONTROL PANEL UNIT V-12115 (Cont)		
	1413-4	TERMINAL LUG V-83330		22
	MS21266-1N	GROMMET		23
	7124-1522-1	COVER, DUST V-12115		24
	7124-1524-1	PLATE, TRANSFORMER, MTG V-12115		25
	7124-1508-1	PLATE, IDENTIFICATION V-12115		26
	7124-1521-1	PLATE, CONNECTOR, MTG V-12115		27
	7124-1510-1	PANEL, FRONT V-12115		28
	7124-1517-1	WINDOW V-12115		29
	7124-1523-1	CHASSIS, MAIN V-12115		30
	7124-0130-101	PAD V-12115		31
	D53018	RETAINER, ELECTRICAL CONNECTOR V-71468, V-12115 SPEC CONT DWG SC5307-0003-6		32
	4838-1-0516	TERMINAL, INSULATED V-71279, V-12115 SPEC CONT DWG SC5940-0015-1		33

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1224-A100	7124-1600-1	LED DISPLAY V-12115		1
C101	CK06BX104K	CAPACITOR, 0.1μF		2
C102	S-226R-20	CAPACITOR, 22μF V-06751		3
C103	CK06BX104K	CAPACITOR, 0.1μF		4
Q101	2N2222A	TRANSISTOR		5
Q102	2N2222A	TRANSISTOR		6
Q103	2N2222A	TRANSISTOR		7
Q104	2N2222A	TRANSISTOR		8
Q105	2N2907A	TRANSISTOR		9
Q106	2N2907A	TRANSISTOR		10
Q107	2N2907A	TRANSISTOR		11
Q108	2N2907A	TRANSISTOR		12
R101	RC05G102JS	RESISTOR		13
R102	RC05G222JS	RESISTOR		14
R103	RC05G202JS	RESISTOR		15
R104	RCR07G101JS	RESISTOR		16
R105	RCR07G101JS	RESISTOR		17
R106	RC07G682JS	RESISTOR		18
R107	RN55C6042F	RESISTOR		19
R108	RC07G512JS	RESISTOR		20
R109	RCR07G202JS	RESISTOR		21
R110	RCR07G103JS	RESISTOR		22
R111	RCR07G103JS	RESISTOR		23
R112	RCR20G221JS	RESISTOR		24
R113	RCR07G202JS	RESISTOR		25
R114	RC07G512JS	RESISTOR		26
R115	RC07G272JS	RESISTOR		27
R117	RCR07G102JS	RESISTOR		28
TP101	016-4005-BRN	TEST POINT V-98291		29
TP102	016-4005-RED	TEST POINT V-98291		30
TP103	016-4005-ORN	TEST POINT V-98291		31
TP104	016-4005-YEL	TEST POINT V-98291		32

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1224-A100	7124-1600-1	LED DISPLAY V-12115 (Cont)		
TP105	016-4005-GRN	TEST POINT V-98291		33
TP106	016-4005-BLU	TEST POINT V-98291		34
U101	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		35
U102	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		36
U103	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		37
U104	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		38
U105	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		39
U106	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		40
U107	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		41
U108	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		42
U109	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		43
U110	5082-7302	LIGHT EMITTING DIODE DISPLAY V-28480		44
U111	S54157B	INTEGRATED CIRCUIT V-18324		45
U112	S54157B	INTEGRATED CIRCUIT V-18324		46

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1224-A100	7124-1600-1	LED DISPLAY V-12115 (Cont)		
U113	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		47
U114	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		48
U115	S54157B	INTEGRATED CIRCUIT V-18324		49
U116	S54157B	INTEGRATED CIRCUIT V-18324		50
U117	S54157B	INTEGRATED CIRCUIT V-18324		51
U118	S54157B	INTEGRATED CIRCUIT V-18324		52
U119	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		53
U120	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		54
U121	S54157B	INTEGRATED CIRCUIT V-18324		55
U122	S54157B	INTEGRATED CIRCUIT V-18324		56
U123	S54164	INTEGRATED CIRCUIT V-18324		57
U124	SN54122J	INTEGRATED CIRCUIT V-01295		58
U125	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		59
U126	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		60
U127	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		61
U128	899-3-R100	INTEGRATED CIRCUIT V-80740		62
U129	S54164	INTEGRATED CIRCUIT V-18324		63
U130	S5474A	INTEGRATED CIRCUIT V-18324		64

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1224-A100	7124-1600-1	LED DISPLAY V-12115 (Cont)		
U131	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		65
U132	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		66
U133	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		67
U134	899-3-R100	INTEGRATED CIRCUIT V-80740		68
U135	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		69
U136	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		70
U137	5082-4882	LIGHT EMITTING DIODE INDICATOR V-28480		71
	7124-1520-1	HEAT SINK V-12115		72
	10034N	PAD, TRANSISTOR V-07047, V-12115 SPEC CONT DWG SC5975-0018-1		73
	02-048-113-6-125	CONTACTS V-91662		74
	9532B-SS-0632-7	STANDOFF V-06540		75
	62-5301-41-12	PIN, GUIDE V-91662		76
	62-5301-40-12	SOCKET, GUIDE V-91662		77
	8060-1G7	SOCKET V-91506		78



NOTE: COMPONENTS SHOWN AS BROKEN LINES ARE MOUNTED ON FARSIDE OF P.C. BOARD

Figure 1224. Light Emitting Diode (LED) Display

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1225-A200	7124-1605-1	LED LOGIC V-12115		1
CR202	HP5082-2800	DIODE V-28480		2
R201	RC05G272JS	RESISTOR		3
R202	RC05G102JS	RESISTOR		4
R203	RC05G202JS	RESISTOR		5
R204	RC05G822JS	RESISTOR		6
R205	RC05G103JS	RESISTOR		7
R206	RC05G272JS	RESISTOR		8
R207	RC05G272JS	RESISTOR		9
R208	RC05G272JS	RESISTOR		10
TP201	016-4005-BRN	TEST POINT V-98291		11
TP202	016-4005-RED	TEST POINT V-98291		12
TP203	016-4005-ORN	TEST POINT V-98291		13
TP204	016-4005-YEL	TEST POINT V-98291		14
TP205	016-4005-GRN	TEST POINT V-98291		15
TP206	016-4005-BLU	TEST POINT V-98291		16
TP207	016-4005-VIO	TEST POINT V-98291		17
TP208	016-4005-GRA	TEST POINT V-98291		18
TP209	016-4005-WHT	TEST POINT V-98291		19
TP210	016-4005-BLK	TEST POINT V-98291		20
U201	S5474A	INTEGRATED CIRCUIT V-18324		21
U202	S5402A	INTEGRATED CIRCUIT V-18324		22
U203	S5404A	INTEGRATED CIRCUIT V-18324		23

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1225-A200	7124-1605-1	LED LOGIC V-12115 (Cont)		
U204	S5400A	INTEGRATED CIRCUIT V-18234		24
	02-048-113-6-125	CONTACTS V-91662		25
	62-5301-41-12	PIN, GUIDE V-91662		26
	62-5301-40-12	SOCKET, GUIDE V-91662		27
	SC6145-0010-9	WIRE, #26 AWG INSULATED V-12115		28

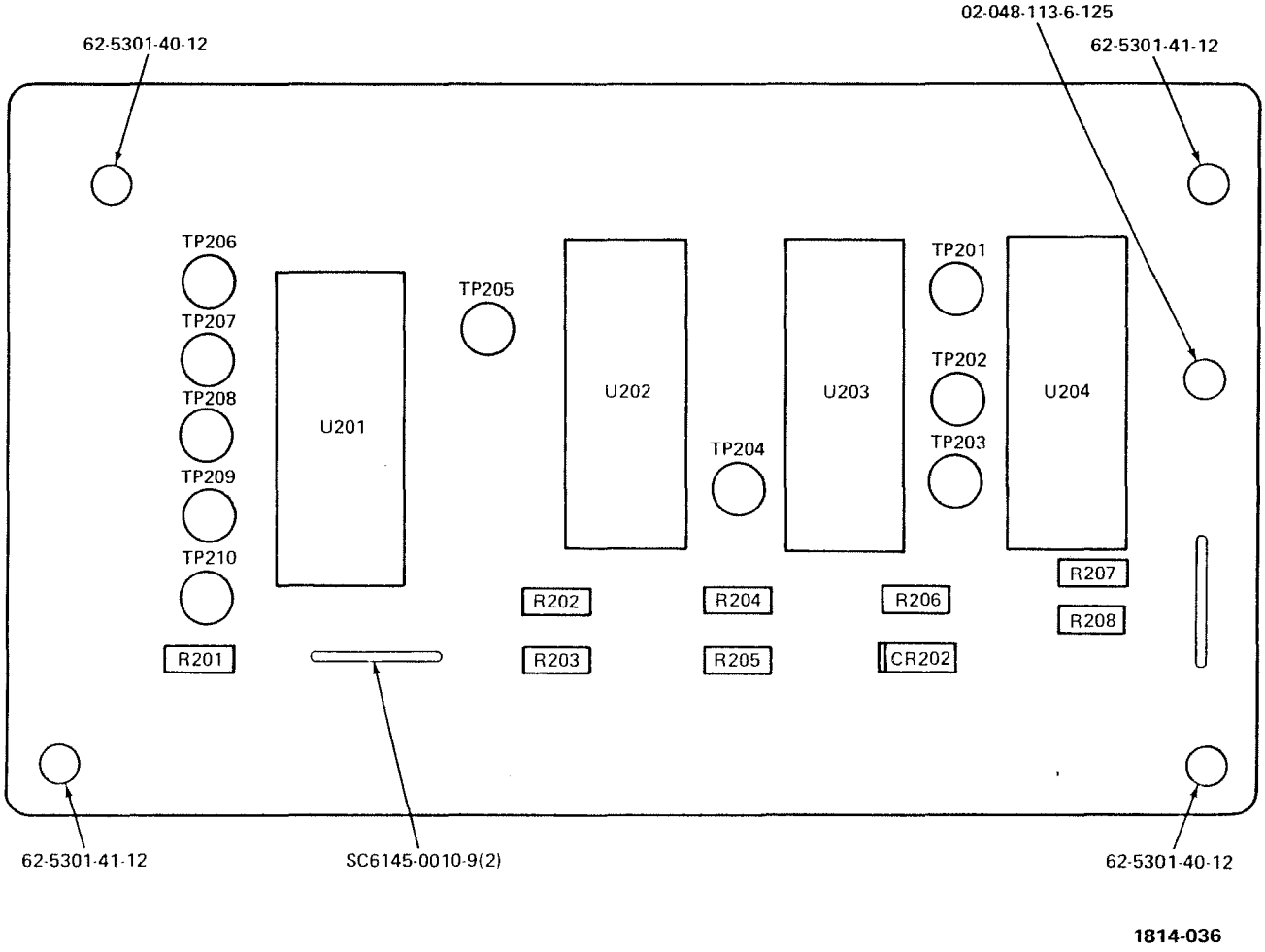


Figure 1225. Light Emitting Diode (LED) Logic

FIG. & INDEX NO.	PART NO.	NOMENCLATURE	AIRLINE PART NO.	ITEM NO.
1226-A300	7124-1610-1	COURSE SELECT V-12115		1
J301	2VH6/1AK5	CONNECTOR V-05574		2
J302	2VH6/1AK5	CONNECTOR V-05574		3
J303	2VH6/1AK5	CONNECTOR V-05574		4
P301	00-7022-017-000-001	CONNECTOR V-91662		5
R301	RC07G102JS	RESISTOR		6

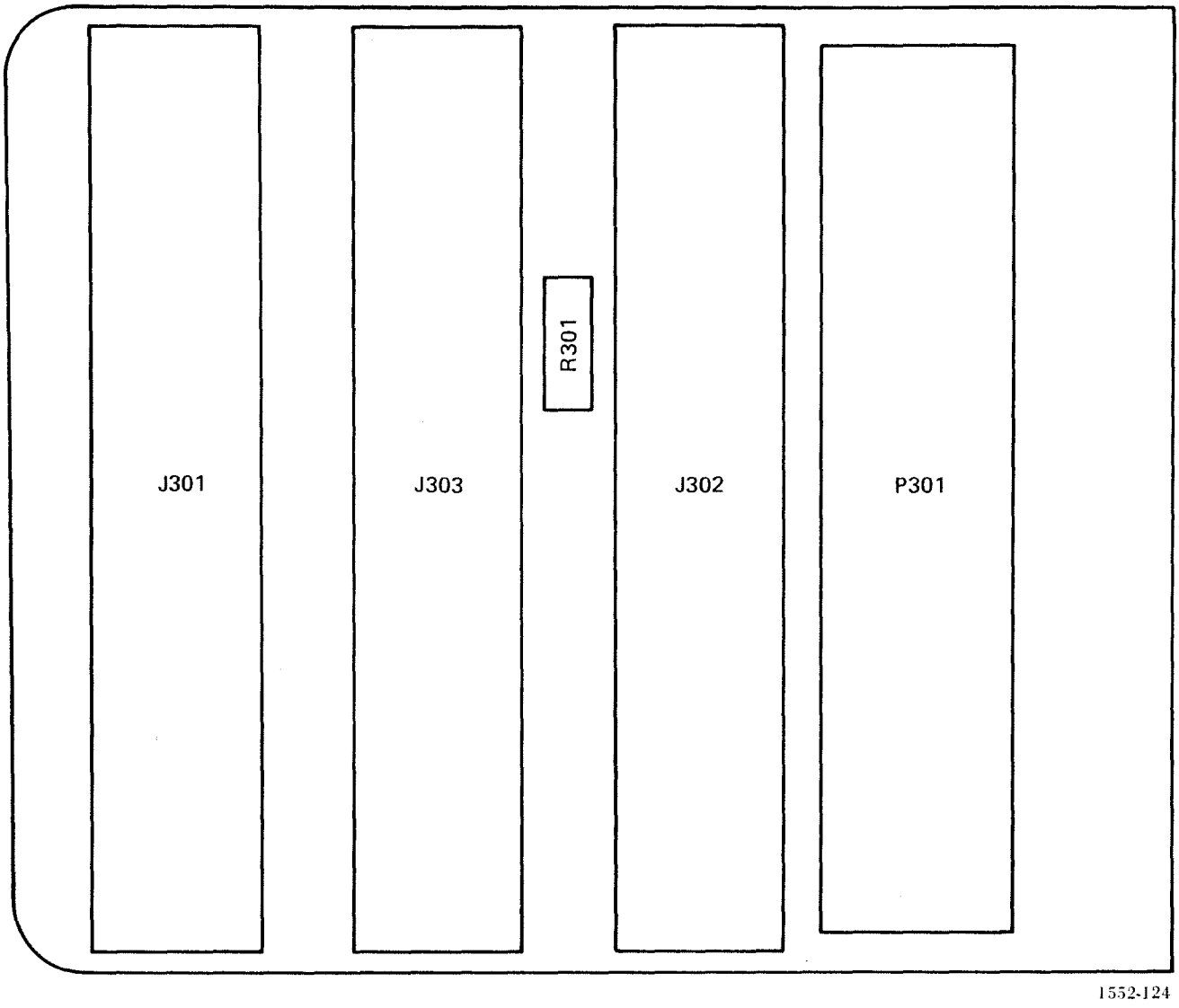


Figure 1226. Course Select

CODE	MANUFACTURER'S NAME	ADDRESS
01295	Texas Instrument Inc Components Group	PO Box 5012 13500 N Central Expressway Dallas, Tx 75222
02768	Illinois Tool Works Inc Fastex Division	195 Algonquin Road Des Plaines Il 60016
04426	Illinois Tool Works Inc Licon Division	6615 W Irving Park Rd Chicago, Il 60634
04713	Motorola Inc Semiconductor Products Div	5005 E McDowell Rd Phoenix, Az 85008
05397	Union Carbide Corp Materials Systems Div	11901 Madison Ave Cleveland, Oh 44101
05574	Viking Industries Inc	21001 Nordhoff Chatsworth, Ca 91311
06540	Amatom Electronic Hardware Div of White Corp	81 Rockdale Ave New Rochelle, NY 10802
06751	Components Inc Semcor Division	3540 W Osborn Rd Phoenix, Az 85019
06773	Timber Top Inc	199 N Main St Freeport, NY 11520
07047	Ross Milton Co, The	511 Second Street Pike Southampton, Pa 18966
07126	Digitran Co, The	855 South Arroya Parkway Pasadena, Ca 91109
07181	Flite-Tronics Co Inc	3314 Burtn Burbank, Ca 91502
07263	Fairchild Semiconductor A Division of Fairchild Camera and Instrument Co	464 Ellis St Mountain View, Ca 94040
08289	Blinn Delbert Co Inc, The	1678 E Mission Blvd PO Box 2007 Pomona. Ca 91766

CODE	MANUFACTURER'S NAME	ADDRESS
08524	Deutsch Fastener Corp	PO Box 90925 7001 W Imperial Hwy Los Angeles, Ca 90009
08730	Venaline Product Co Inc	PO Box 3455 West Main St Wyckoff, NJ 07481
09023	Cornell-Dubilier Electronics	2652 Dalrymple St Sanford, NC 27330
10110	Scientific-Atlanta Inc	PO Box 13654 Atlanta, Ga 30324
11117	Elastimold Division of Amerance Esna Corp	1 Esna Park Hackettstown, NJ 07340
11402	Hisonic Inc	249 N Troost Olathe, Kans 66061
12115	Sierra Research Corp	PO Box 222 Buffalo, NY 14225
12969	Unitrode Corp	580 Pleasant St Watertown, Ma 02172
18324	Signetics Corp	811 East Argues Ave Sunnyvale, Ca 94086
27014	National Semi-Conductor Corp	2950 San Ysidro Way Santa Clara, Ca 95051
27193	Cutler-Hammer Inc Specialty Products Division	420/N 27th St Milwaukee, Wi 53216
27802	Vectron Laboratories Inc	121 Water St Norwalk, Ct 06854
28480	Hewlett-Packard Co	1501 Page Mill Rd Palo Alto, Ca 94304
28584	Data Products Core Memories Inc	2525 Charleston Rd Mountain View, Ca 94040
34333	Silicon General Inc	7382 Bolsa Ave Westminister, Ca 92683
34335	Advanced Micro Devices	901 Thompson Pl Sunnyvale, Ca 94086

CODE	MANUFACTURER'S NAME	ADDRESS
56289	Sprague Electronic Co	North Adams, Ma 01247
71279	Cambridge Thermionic Corp	445 Concord Ave Cambridge, Ma 02138
71468	ITT Cannon Electric	666 E Dyer Rd Santa Ana, Ca 92702
71590	Globe-Union Inc Centralab Electronic Div	5757 N Green Bay Ave Milwaukee, Wi 53201
74199	Quam Nichols Co	218 E Marquette Rd Chicago, Il 60637
79963	Zierick Mfg Co	Radio Circle Mt Kisco, NY 10549
80294	Bourns Inc	1200 Columbia Ave Riverside, Ca 92507
80740	Beckman Instruments Inc	2500 Harbor Blvd Fullerton, Ca 92634
81860	Barry Controls Division of Barry Wright Corp	700 Pleasant St Watertown, Ma 02172
82389	Switchcraft Inc	5555 N Elston Ave Chicago, Il 60630
82877	Rotron Inc	7-9 Hasbrouck Lane Woodstock, NY 12498
83330	Herman H Smith Inc	812 Sinediker Ave Brooklyn, NY 11207
83803	Peerless Radio Corp	19 Wilbur St Lynbrook, NY 11563
90634	Gulton Industries Inc	Gulton St Metucken, NJ 08840
91506	Augat Inc	33 Percy Ave Attleboro, Ma 02703
91637	Dale Electronics Inc	PO Box 609 Columbus, Nb 68601
91662	Elco Corp	Maryland Rd and Computer Ave Willow Grove, Pa 19090

CODE	MANUFACTURER'S NAME	ADDRESS
94867	Churchill Corp	344 Franklin St Melrose, Ma 02176
95146	Alco Electronics Products Inc	PO Box 1348 3 Walcott Ave Lawrence, Ma 01843
95712	Bendix Corp The Microwave Devices Div	Hurricane Rd Franklin, Ia 46131
95987	Weckesser Co Inc	4444 W Irving Park Rd Chicago, Il 60641
98291	Selectro Corp	225 Hoyt Mamaroneck, NY 10544

AIRCRAFT STATIC INVERTER

INSTRUCTION MANUAL

FOR

MODEL PC-15( )

AND

MODEL PC-15B( ) SERIES

TSO-C73

FLITE-TRONICS CO., INC.
3314 BURTON AVENUE
BURBANK, CALIFORNIA

AIRCRAFT STATIC INVERTER

INSTRUCTION MANUAL

FOR

MODEL PC-15( )

AND

MODEL PC-15B( ) SERIES

TSO-C73

FLITE-TRONICS CO., INC.
3314 BURTON AVENUE
BURBANK, CALIFORNIA

FLITE-TRONICS STATIC INVERTERS
UNDER MODEL PC-15( ) and
MODEL PC-15B( ) SERIES

MODEL SERIES	DESCRIPTION
PC-15	Basic 250VA, 400HZ, 115VAC output inverter 5 pin or 7 pin connectors This model series superseded by Model PC-15B
PC-15A	250VA, 400HZ, 115V & 26VAC outputs, Osc. Sync. output. 7 pin connector This model series superseded by Model PC-15B.
PC-15A with M1 after Serial No.	PC-15A with field modification per Flite-Tronic's Service Bulletin No.1/PC-15A. This model series superseded by Model PC-15B
PC-15A with A after Serial No.	PC-15A with increased fuse-rupture capability per Flite-Tronic's Service Bulletin No.2/PC-15A. This model series superseded by Model PC-15B.
* PC-15B or PC-15A with B after Serial No.	Currently available basic 250VA, 400HZ Static Inverter 115V & 26VAC outputs, Osc. Sync. output. 7 pin connector Refer to Section VII of this Manual for detail
PC-15C	Not Assigned.
* PC-15D	PC15B with 150VA from 26VAC output 100VA from 115VAC output Osc. Sync. output 7 pin connector Refer to Section VII of this Manual for detail.
* PC-15E	PC-15B with remote on & off feature added 9 pin connector. Refer to Section VII of this Manual for detail.
* PC-15F	PC-15B with DC return isolated from chassis Refer to Section VII of this Manual for detail.
* PC-15G	PC-15F with a MS3102A22-15P connector and 115VAC output only. Refer to Section VII of this Manual for detail.

* Refer to Page ii for Model identification changes.

Model identification change has been made as listed below. This is an identification change of the inverters of current manufacture. Interchangeability of the PC-15B( ) with the PC-15B, effective Serial Number 3178, is not affected and the electrical and mechanical specifications are the same.

The electrical and mechanical specifications of the PC-15B( ) are equal to or superior than the PC-15( ) manufactured previously. PC-15B( ) Serial Number effectivity is 3700. *

NEW IDENTIFICATION		PREVIOUS IDENTIFICATION	
MODEL	SERIAL NUMBER EFFECTIVITY	MODEL	SERIAL NUMBER
PC-15B( )	3700	PC-15B	3178 & Up
PC-15B(D)	25	PC-15D	1 & Up
PC-15B(E)	27	PC-15E	9 & Up
PC-15B(F)	3700	PC-15F	3178 & Up
PC-15B(G)	3700	PC-15G	3178 & Up

* Refer to Revision No. 7 for details.

REVISION NUMBERS

TO

INSTRUCTION MANUAL

REVISION NUMBERS	DATE	SERIAL NUMBER EFFECTIVITY
Original Publication	November 1966	Not Applicable
Revision No. 1	March 1968	See Revision No.1
Revision No. 1-5 Pin	March 1968	See Rev. No. 1-5 Pin
Revision No. 2	January 1969	No. 1471 and up
Revision No. 3	September 1969	No. 1934
5th Printing (No change)	September 1970	None
Revision No. 4	April 1971	No. 2779
Revision No. 5	May 1971	None
Revision No. 6	November 1971	No. 3174, 3175, 3178, and up.
Revision No. 7	August 1972	No. 3700 and up
8th Printing	November 1972	None

NOTE:
This manual includes original publication information and all revisions to date.
The original publication is kept intact and all changes with serial number effectivity when applicable are compiled under revision section as they occurred.

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6.7	Revision No. 6 - November 1971	58
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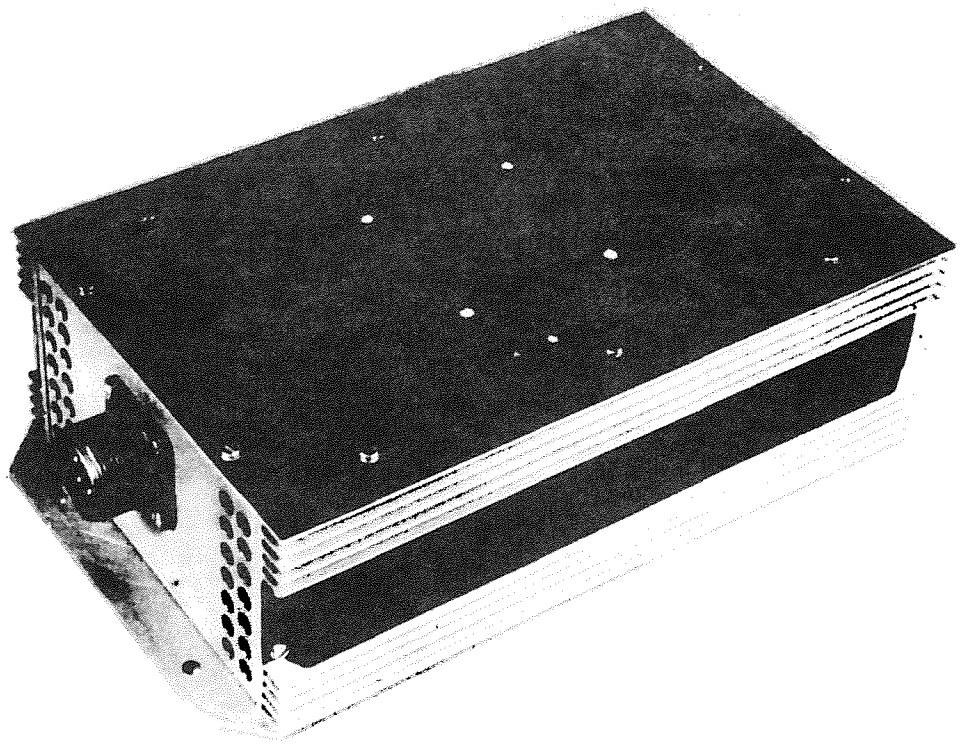


Figure 1.1 Flite-Tronics Model PC-15 and PC-15A

Section I

General Information

1.1 Introduction

This instruction manual has been prepared to provide information in installation, performance, operation, identification of parts, and maintenance of the Flite-Tronics' Model PC-15 and PC-15A Transistorized Power Inverter. PC-15A is identical to PC-15, except it has a 26.0 VAC 400 HZ output.

1.2 Purpose of Equipment

The PC-15 and PC-15A, shown in Figure 1.1, is a transistorized inverter designed to supply AC power at 400 cycles per second.

The unit is capable of delivering a current overload of 150% for a minimum duration of 5 minutes at full rated output. This permits the PC-15 and PC-15A to power equipment that requires momentary surges of power during turn on. When the 26 VAC output from the PC-15A is not used, the PC-15A is identical in performance to the PC-15.

1.3 Specifications for PC-15 and PC-15A

Input Voltage..... 28.0 VDC

Input Current:

a) 14.2 amperes for PC-15s delivering 250 VA.

b) .75 amperes typical no load.

Input Voltage Range:

22 to 30 VDC
Operate down to 20 VDC

Input Overvoltage:

Withstands 130% input overvoltage for 5 minutes, while supplying full rated 250 VA output power. Output voltage under this condition, +5%, -7%.

Output Voltage:
(PC-15 and PC-15A)
115 VAC rms +5%, -7% 22 to 30 VDC. Greater than 100 VAC down to input of 20 VDC

Pin E Output @ 20 VDC input:
115 VAC @ 90% load.

Output Voltage: (PC-15A only)

26.0 VAC rms +5%, -7%

Output Frequency: 400 HZ ± 1%

Total Maximum Continuous Output Power..... 250 VA

Output Power, PC-15A 26.0 VAC..... 75 VA

Output Waveform:
Sine Wave, Single Phase

For Higher Power Output:

Units may be paralleled for higher power output. (Refer to installation section.)

Amplitude Distortion
Both output..... 7% Max.
26-30 VDC input (Typ. 3%)

Overload Capacity:

Withstands 150% output current overload for at least 5 minutes.

Power Factor..... .8 to 1.0

Input Voltage Protection:

Unit withstands transient of 88 volts lasting 1 millisecond on the 28.0 VDC input line.

Excessive Overload and Output Short Circuit:

Withstands without damage or degradation loads exceeding 150% nominal to an output short circuit. Unit delivers rated output on removal of above condition.

Altitude..... 45,000 feet

Efficiency..... 70% typical

Temperature: -65° F. to 160° F.

Emission RFI:

Radiated & Conducted... 90 KC to 1000 MC

Far below levels specified in Appendix A of RTCA Paper 120-61/DO-108 Category "A", see pages 4 and 5.

Weight..... 8.2 lbs.

Size:

Width	6"
Length	9-3/8" (not incl. mounting flange)
Height	3-3/16"

1.3 Specifications for PC-15B

Input Voltage..... 28.0 VDC

Input Current:

a) 14.2 amperes for PC-15s delivering 250 VA.

b) .75 amperes typical no load.

Input Voltage Range:

22 to 30 VDC
Operate down to 20 VDC

Input Overvoltage:

Withstands 130% input overvoltage for 5 minutes, while supplying full rated 250 VA output power. Output voltage under this condition, +5%, -7%.

Output Voltage:

115 VAC rms +5%, -7% 22 to 30 VDC. Greater than 100 VAC down to input of 20 VDC

Output Voltage:
26.0 VAC rms +5%, -7%

Pin E Output @ 20 VDC Input:
115 VAC +5%, -7% @ 90% load

Output Frequency: 400 HZ ± 1%

Total Maximum Continuous Output Power..... 250 VA
(Sum of 115 VAC and 26 VAC outputs)

Output Waveform:
Sine Wave, Single Phase

For Higher Power Output:

Units may be paralleled for higher power output. (Refer to installation section.)

Amplitude Distortion
Both output..... 7% Max.
26-30 VDC input (Typ. 3%)

Overload Capacity:

Withstands 150% output current overload for at least 5 minutes.

Power Factor..... .8 to 1.0

Input Voltage Protection:

Unit withstands transient of 88 volts lasting 1 millisecond on the 28.0 VDC input line.

*Excessive Overload and Output Short Circuit:

Withstands without damage or degradation loads exceeding 150% nominal to an output short circuit. Unit delivers rated output on removal of above condition.

Altitude..... 45,000 feet

Efficiency..... 70% typical

Temperature: -65° F. to 160° F.

Emission RFI:

Radiated & Conducted... 90 KC to 1000 MC

Far below levels specified in Appendix A of RTCA Paper 120-61/DO-108 Category "A", see pages 4 and 5.

Weight..... 8.2 lbs.

Size:

Width	6"
Length	9-3/8" (not incl. mounting flange)
Height	3-3/16"

*See Page A0 for output fault clearance capability

Humidity:

Greater than 95% for ten days, temperature cycled between 75° F. to 160° F.

Vibration:

To withstand in three directions

.08 DA	5-15 HZ
.036 DA	15-70 HZ
10 G's	70-500 HZ

Shock:

To withstand at least 10 G's for 11 milliseconds in three directions.

1.4 Description

The PC-15 and PC-15A is a transistorized airborne static power inverter. The unit operates from 28.0 VDC aircraft power source and delivers 115 VAC at 400 HZ. The Model PC-15A has a 26.0 VAC output. The total continuous power drawn from the two outputs should not exceed 250 VA for the PC-15A.

An L/C tuned 400 HZ oscillator operating in a class B push-pull mode is used to generate the 400 HZ signal.

This signal is amplified by 4 stages of class B push-pull emitter follower amplifiers. Protective circuits for output overload, thermal runaway and input voltage transient are incorporated to make the PC-15s an extremely reliable equipment.

Frequency and output voltage are adjustable. However, once set at the factory, they should not require readjusting for the life of the equipment.

TEST CONDITION: Broadband Radiated
TEST MODE: Steady State Mode
LEGEND: SPECIFICATION
MEASURED LEVEL
AMBIENT LEVEL
No narrow band C.W. detected.

TEST SPECIMEN: Flite-Tronics Co. Static Inverter M/N PC-15, S/N 100
SPECIFICATION: R.T.C.A. Paper 120-61/ DO-108, Appendix A
DATE: 12 June '66

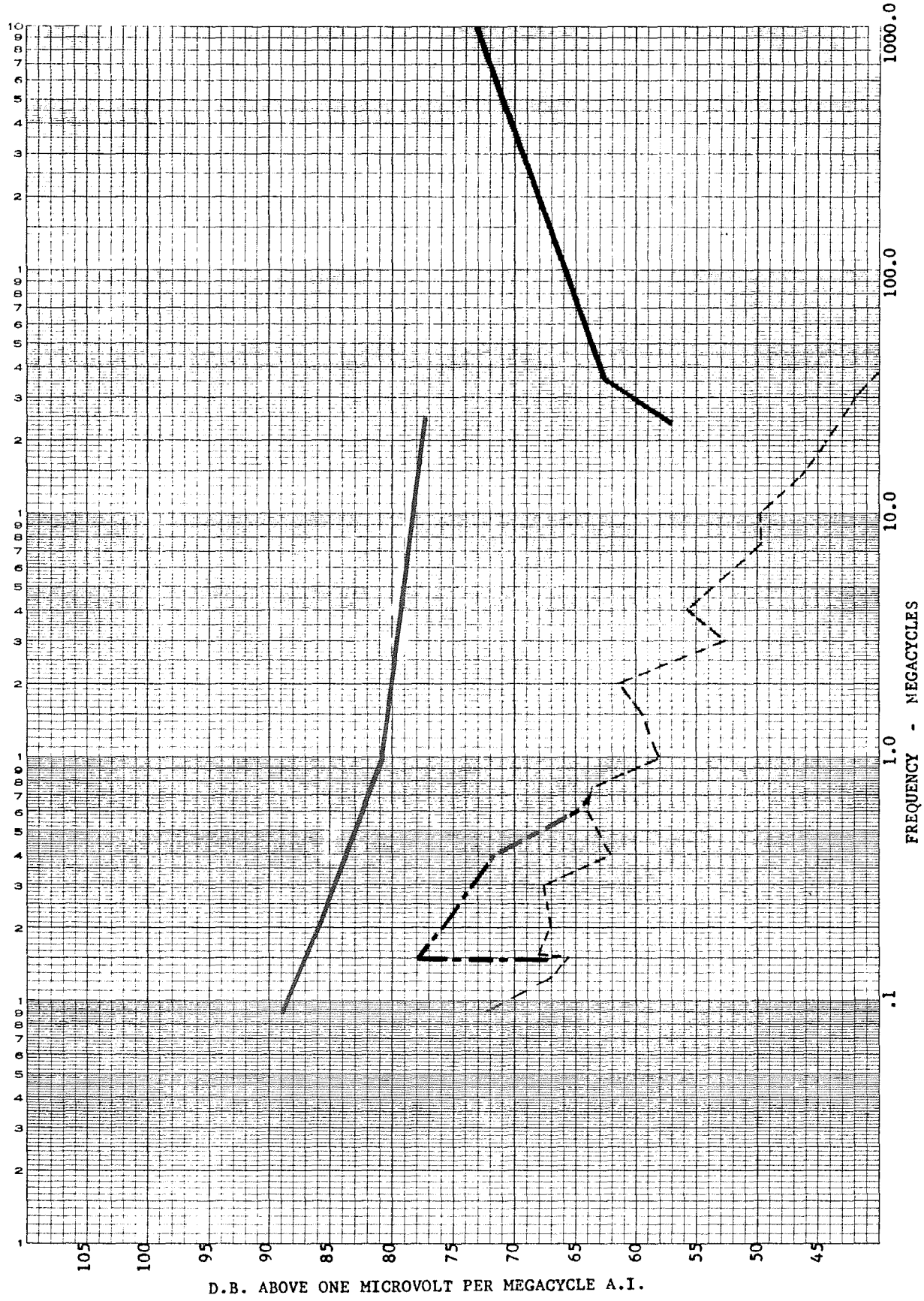


FIGURE 1.2 EMISSION RADIATED

TEST CONDITION: Broadband Conducted
TEST MODE: Steady State Mode
LEGEND: SPECIFICATION
MEASURED LEVEL
AMBIENT LEVEL

TEST SPECIMEN: Flite-Tronics Co. Static Inverter M/N PC-15, S/N 100
SPECIFICATION: R.T.C.A. Paper 120-61/ DO-108, Appendix A
DATE: 12 June '66

No narrow band C.W. detected.

Statement by Test Lab.; Cornell-Dublier Electronics Division.

Summary of Results for Radiated and Conducted RFI:

The Static Inverter M/N PC-15, S/N 100, was subjected to an electromagnetic interference investigation test program per R.T.C.A. Paper 120-61/DO-108, Appendix A. Upon evaluation of the test data, it was found that the above referenced static inverter generated interference which was below the specification limits of R.T.C.A Paper 120-61/DO-108, Appendix A.

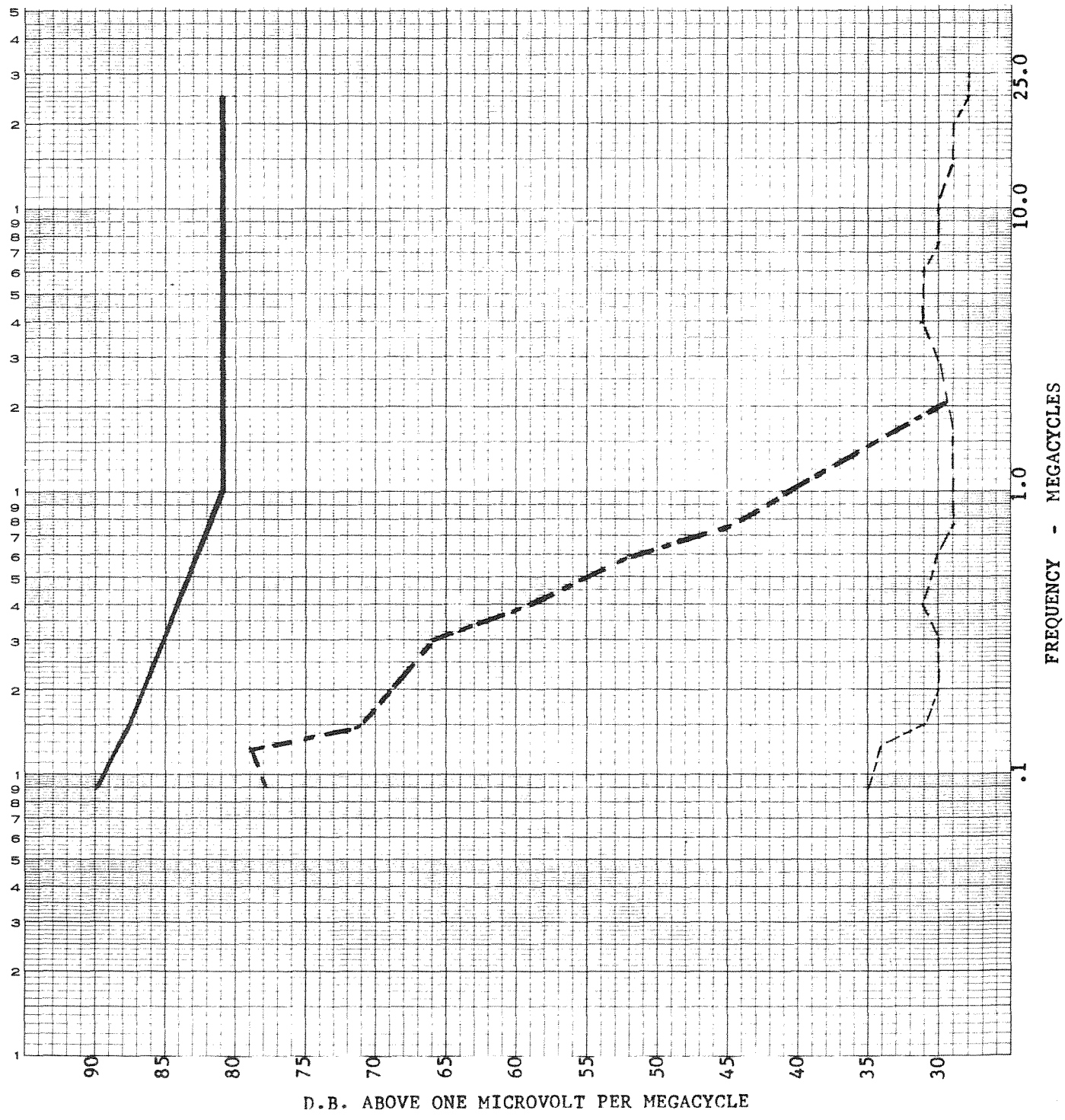


FIGURE 1.3 EMISSION RFI CONDUCTED

NOTE TO SECTION II

N2.1 The installation and mounting dimensions for different model series when applicable in addition to pages 8 and 9 are shown on following pages.

MODEL SERIES	PAGE
PC-15B	A7
PC-15E	A11
PC-15F	A14
PC-15G	A16

N2.2 Addition to N2.1

Rev. 7	63

N2.3 Any reference to PC-15 or PC-15A in this section is applicable to PC-15B( ) unless otherwise noted under Model PC-15B.

Section II

Installation

2.1 General

The Model PC-15 and PC-15A (hereinafter referred to as PC-15s) is a 400 HZ Inverter, ready to install when delivered from the factory.

To determine that the unit is operating satisfactorily, a bench test may be made. The external hook-up for such a test is illustrated in Figure 4.1 page 22.

The PC-15s will deliver 250 VA of power to a load having a power factor between .8 lag to 1.0. The PC-15s will operate into loads which are more reactive; however, an external phase correcting capacitor will be required.

The capacitance value may be determined by noting what value causes a null in the input current reading. This, of course, should be determined with the load the PC-15 or PC-15A delivers power to. A poly-carbonate type capacitor having a rating of 300 volts or greater may be used for this phase correcting.

Installation where more than 250 VA of continuous power is required, the PC-15s may be paralleled, as necessary, to double, triple, or even quadruple the power of a single unit.

2.2 Installation Procedure

The PC-15s are environmentally designed to mount on a rack with other equipment, or in any suitable location in the aircraft.

Figure 2.1 illustrates the installation dimensions and mounting centers; see page 8 for PC-15 and page 9 for PC-15A. Mounting hardware should be 10-32 and length long enough to have 1-1/2 threads exposed after installing the necessary hardware.

The mating connector plug to the PC-15s' receptacle is MS3106B18-9S.

A wire size AWG #10 or #12 is suggested for the low voltage DC input and an AWG size #18 for the AC output leads. The low voltage input to the PC-15s should be protected with a 25 amp circuit breaker.

Figure 2.3 page 10 illustrates the electrical connection to operate units in parallel for greater output power capability.

Figure 2.4 page 11 illustrates the electrical connection to operate units in parallel, not only for greater power, but also switching the PC-15s for parallel or independent operation remotely.

Units operating in parallel must have oscillators phase locked. This is

accomplished by connecting pin F together. To frequency lock the PC-15s to other 400 HZ ± .5%, 115 VAC source, R25 is changed .0047 ufd and pin F is connected to that source.

Frequency locking of PC-15s is only necessary when other 400 HZ ± 2 HZ power sources are in an aircraft and resulting in an undesirable beating effect.

CAUTION

THE PC-15S SHOULD NOT BE INSTALLED IN AN AREA WHERE THE AMBIENT AIR TEMPERATURE EXCEEDS 172° F. UNDER ALL WEATHER AND OPERATING CONDITIONS. THE UNIT MAY BE MOUNTED IN ANY POSITION. IN AN INSTALLATION THE VENT HOLES SHOULD NOT BE RESTRICTED. ALSO, THE PC-15S SHOULD BE MOUNTED DIRECTLY TO METALLIC PLATES OR SUPPORTS.

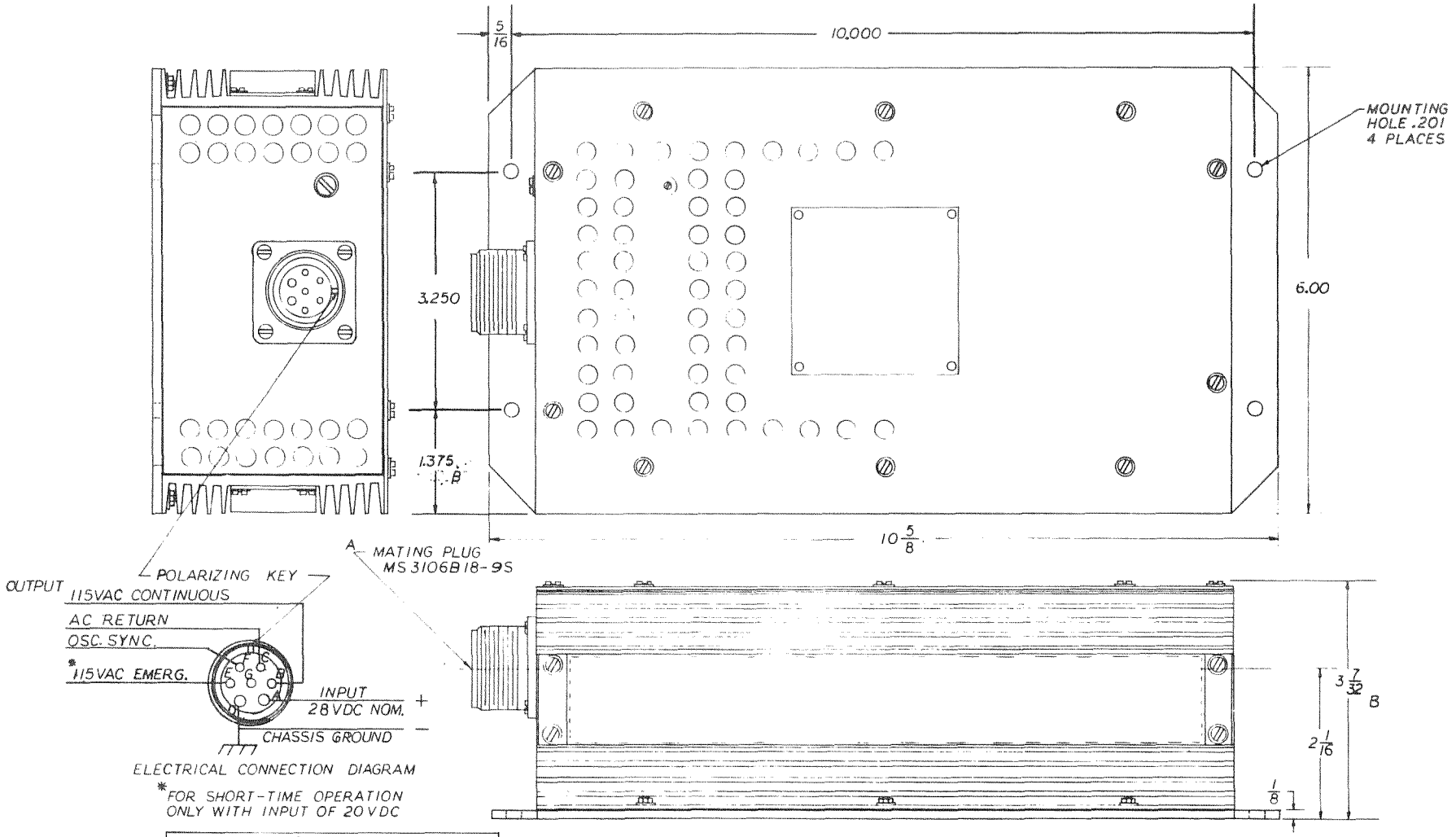
WHEN PC-15S ARE CONNECTED IN PARALLEL, ALL UNITS MUST BE TURNED ON. OTHERWISE, THE PARALLEL CONNECTION SHOULD BE DISCONNECTED TO OPERATE INDEPENDENTLY.

WHEN THE PC-15S ARE OPERATED IN THE FREQUENCY LOCKED MODE TO OTHER 115 VAC 400 HZ ± 2 HZ SOURCE, THE OUTPUT, OF COURSE, SHOULD NOT BE PARALLELED.

EMERGENCY OUTPUT CONNECTION

The 115 VAC output from pin E is for emergency operation only into a load of 90% (225 VA) when the input A+ is 20 VDC.

Means should be provided to connect the load to pin E in an emergency input of 20 VDC. Possible method of remotely switching the load is illustrated on page 11.



ELECTRICAL CONNECTION DIAGRAM

*FOR SHORT-TIME OPERATION ONLY WITH INPUT OF 20VDC

ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	7.75

NOTE:
1. REVISION EFFECTIVE ON S/N 312 & UP, SEE ADDENDUM
2. PC15 WITH 5 PINS SEE SERVICE BULLETIN No. 1

FIGURE 2.1
INSTALLATION AND MOUNTING DIMENSIONS

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
B	Ft 8	4/1/68	gt.	
A	Ft 1	1/27/67	Jm	

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03, XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 1°

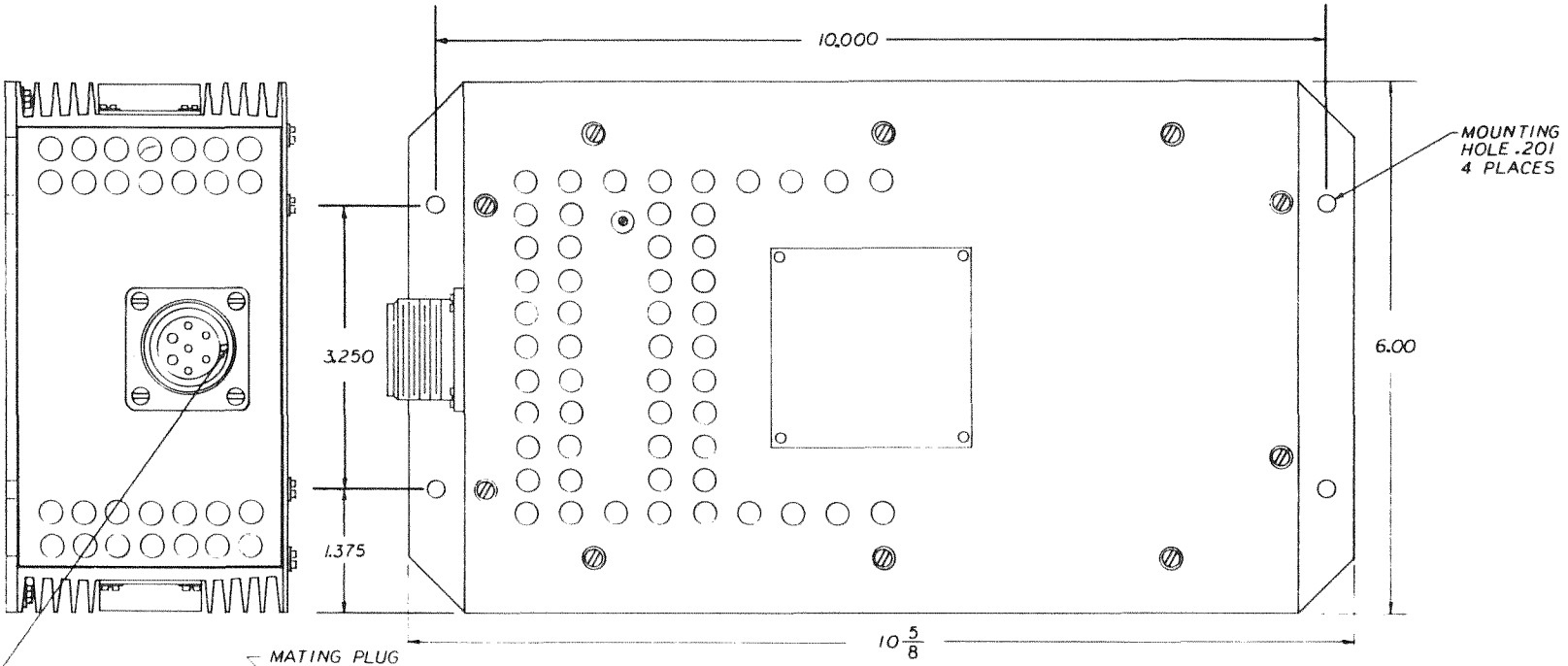
ITEM | PART NO. | CIRCUIT REF. NO. | DESCRIPTION | NO.

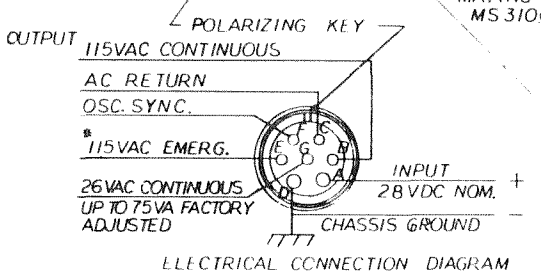
MAT'L.

FLITE-TRONICS, INC.
2312 BURTON AVE., BURBANK, CALIF.

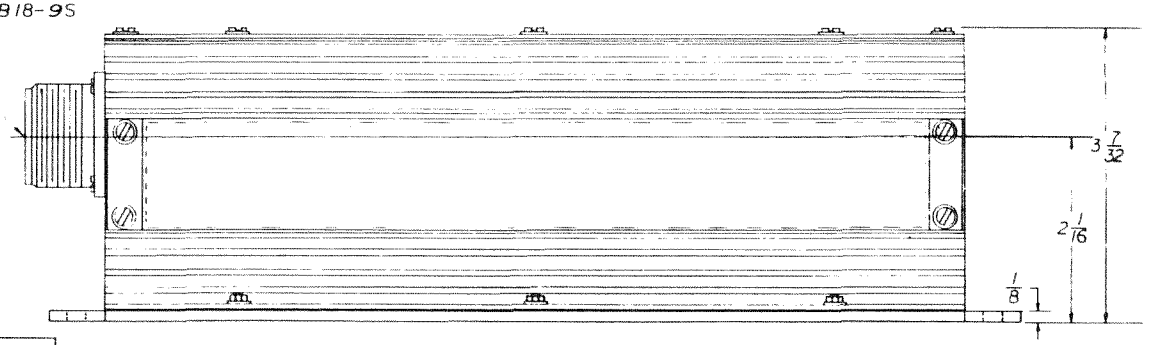
TITLE
PC15 STATIC INVERTER MOUNTING DETAILS

DRAWN Jm 4/8/66
CHK'D
APPR'D 4/8/66
SCALE FULL
MODEL PC15
NEXT ASSY.
SIZE C DWG. NO. 91008





*FOR SHORT-TIME OPERATION ONLY WITH INPUT OF 20VDC



ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115&26
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	7.75

FIGURE 22
INSTALLATION AND MOUNTING DIMENSIONS

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D	ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D

MAT'L

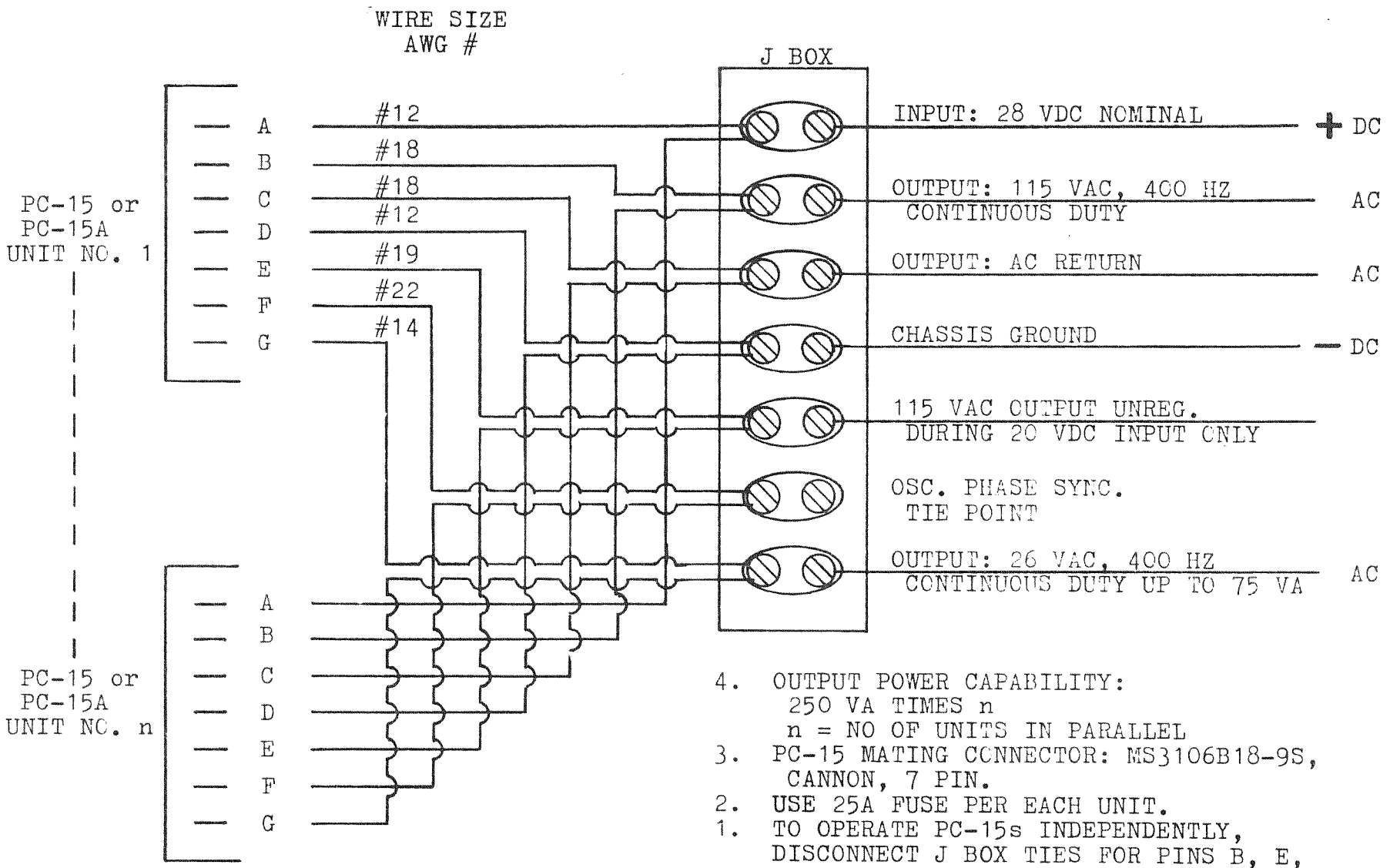
FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15 STATIC INVERTER MOUNTING DETAILS

DRAWN 4/8/66
CHK'D
APPR'D
SCALE FULL
MODEL PC15A
NEXT ASSY.
SIZE C
DWG. NO. 91008-1

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03
XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± .5°

NOTE :



NOTES:

1. TO OPERATE PC-15s INDEPENDENTLY, DISCONNECT J BOX TIES FOR PINS B, E, F AND G.
2. USE 25A FUSE PER EACH UNIT.
3. PC-15 MATING CONNECTOR: MS3106B18-9S, CANNON, 7 PIN.
4. OUTPUT POWER CAPABILITY:
   250 VA TIMES n
   n = NO OF UNITS IN PARALLEL

FIGURE 2.3

CONNECTION TO OPERATE PC-15s IN PARALLEL

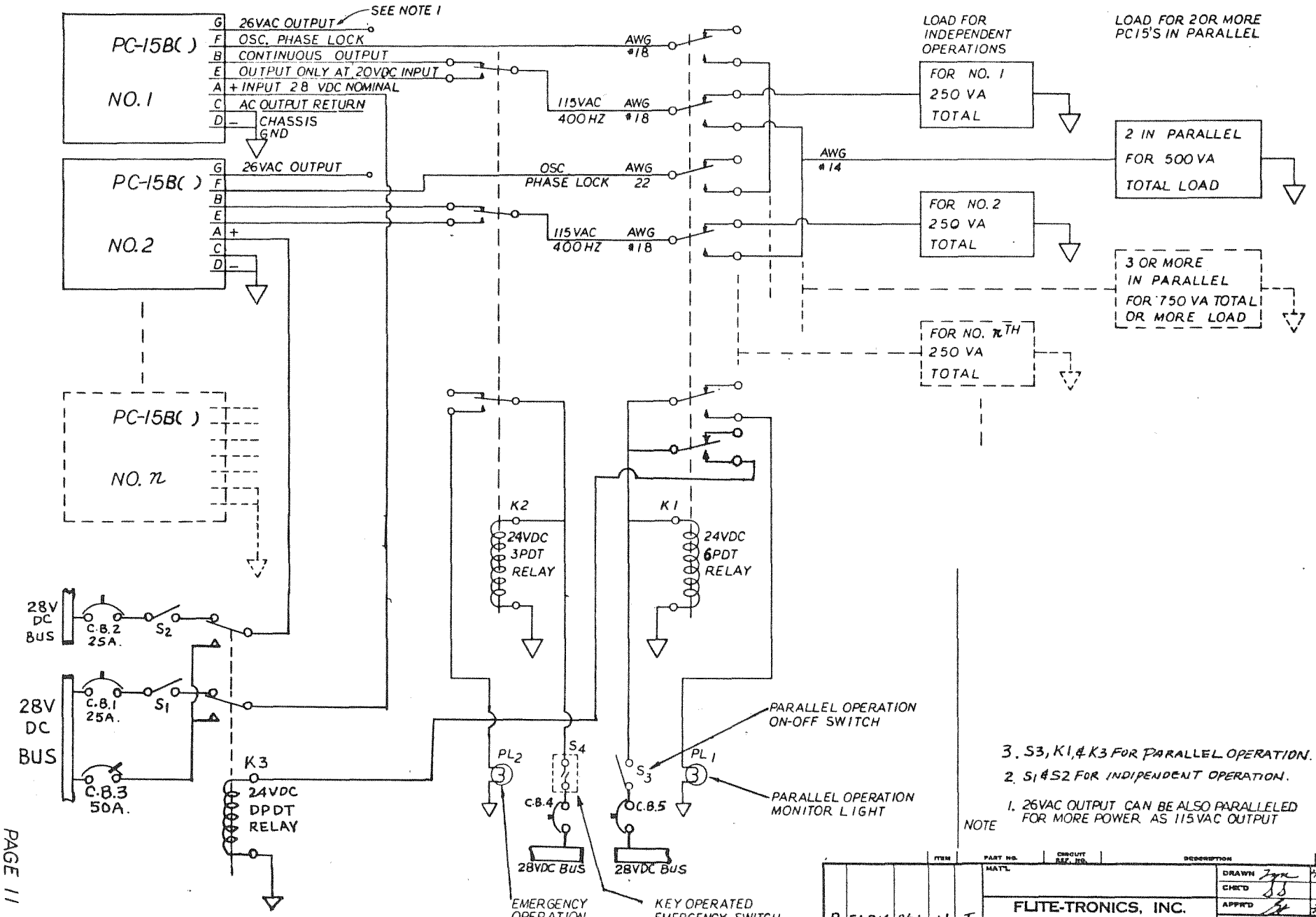


FIGURE 2.4
CONNECTION TO OPERATE PC15'S IN PARALLEL WITH REMOTE DISCONNECT

NOTE TO SECTION III

N3.1 Pages for changes and additions to this section due to revisions and introduction of new model series are listed below for quick reference.

REV. NO/MODEL SERIES	PAGE
Rev. 1, 2, 3	Incorporated
Rev. 4	55, 56
Rev. 5	Incorporated
Rev. 6	58, 61, 62
PC-15B	A1
PC-15D	A0
PC-15E	A0
PC-15F	A0
PC-15G	A0

N3.2 Addition to N3.1

Rev. 7	63
PC-15B( ) Series	63

N3.3 Any reference to PC-15 or PC-15A in this section is applicable to Model PC-15B( ) unless otherwise noted under PC-15B.

Section III

Principles of Operation

3.1 General

The PC-15 and PC-15A (referred to as PC-15s) convert DC energy to AC electrical energy.

The nominal output is 115 VAC on pin B and 26 VAC output from pin G, for Model PC-15A only. However, in an emergency battery condition of 20 VDC input, the output from pin E is 115 VAC working into 90% of full rated load. The output from pin G, the 26 VAC output, will follow the input DC voltage variation below 24.0 VDC. The 400 HZ is generated by an L/C tuned push-pull oscillator. The sine wave signal is amplified by four stages of class B push-pull amplifier. The final power output stage is also class B, but the transistors are cascaded. This permits operating at higher temperature and also decreases the collector to emitter operating voltage in half; i.e., eliminates the possibility of an 88 volt peak transient on the 28.0 VDC buss destructing the transistors. A schematic of the PC-15s is illustrated in Figure 3.2 and 3.3.

3.2 Block Diagram

Figure 3.1 shows the PC-15s' operation in a block diagram form. The block diagram illustrates the time tested and proven circuitry for power amplification of a low level AC signal. All the stages are class B push-pull emitter follower configuration. The emitter follower circuitry having inherent negative feedback introduces very little amplitude and phase distortion.

The output signal is sampled by current and voltage transformers. These components deliver a signal to operate the output overload and output voltage level circuitry.

This output, in turn, controls the push-pull 400 HZ oscillator amplitude.

The output overload reduces the output current and voltage when a load excess of 160% is applied to the output. This same circuitry operates in the event of a short circuit on the output.

The automatic level control maintains the output voltage constant for load and temperature variation.

3.3 400 HZ Sine Wave Oscillator

Inductor-transformer T1 is the feedback, output and resonant tuning transformer. The center tapped primary winding is 1-2-3. Feedback winding is 4-5-6. The output and resonant tuning winding is 7-8-9.

Capacitor C10 (.47 ufd) resonates with the inductance of the output winding at 400 HZ.

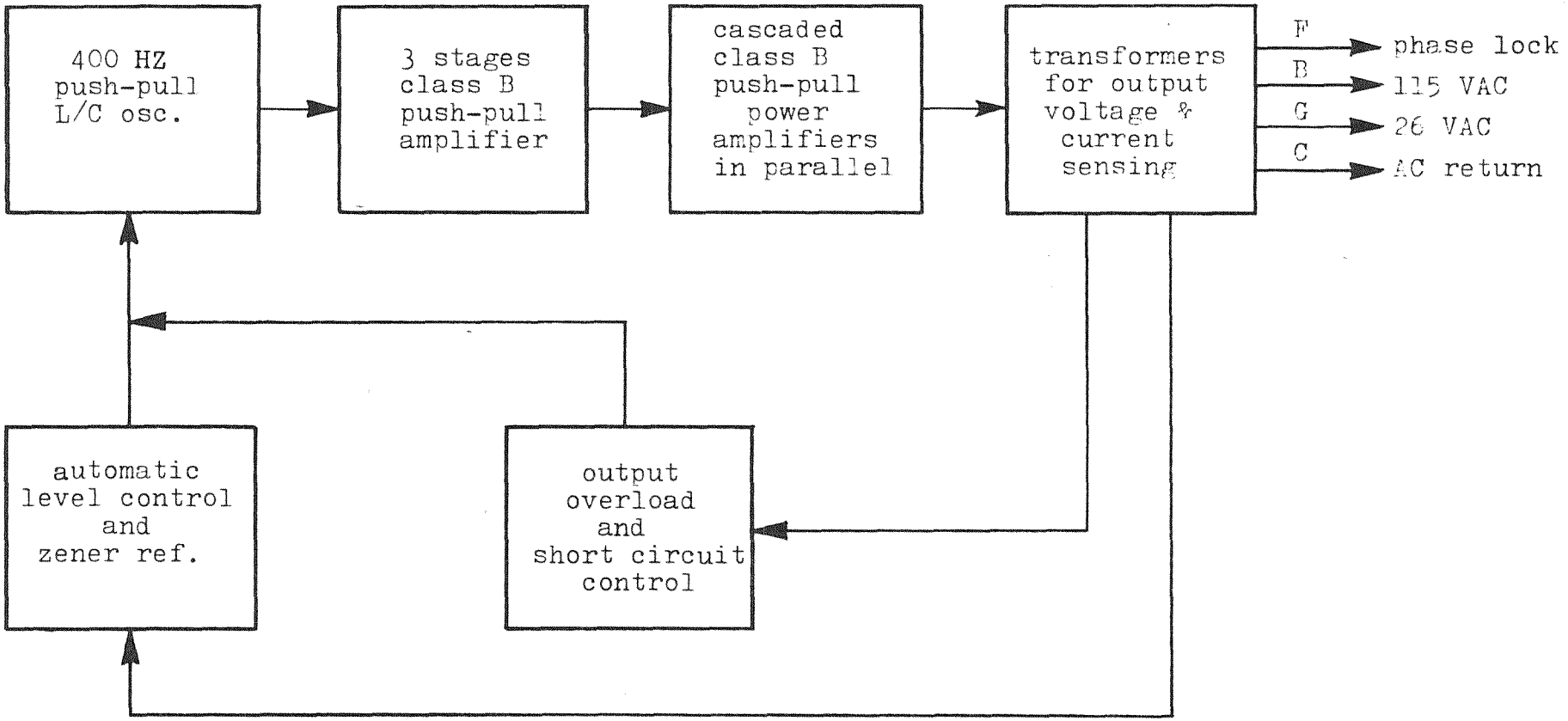
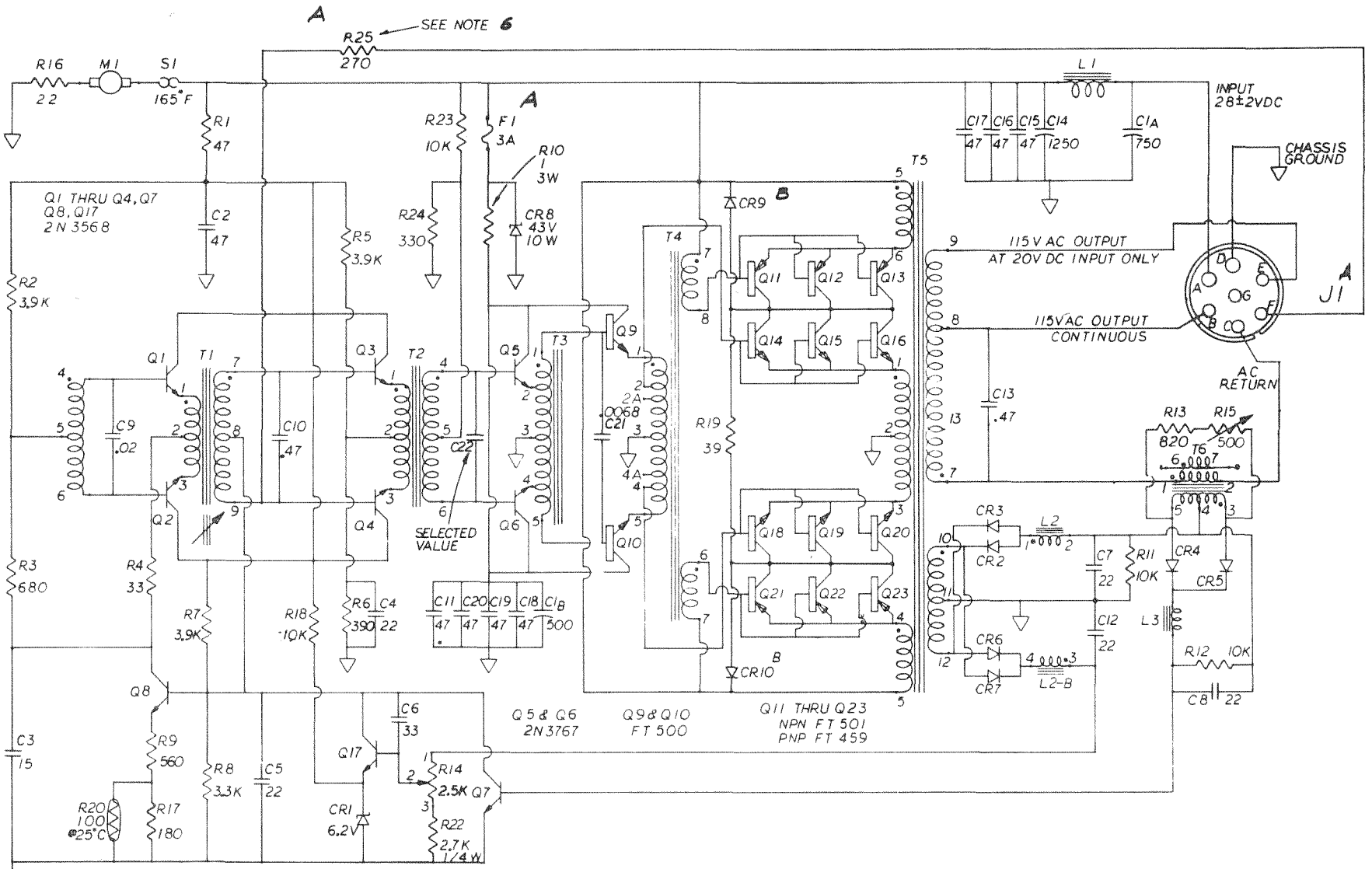


FIGURE 3.1 BLOCK DIAGRAM



7. PC15 WITH 5 PINS SEE SERVICE BULLETIN No. 1

B 6. USE CAPACITOR TO FREQ. LOCK TO OTHER 115VAC, 400HZ LINE (C_{23} TYPICALLY .0047 µF, 600V.), PHASE LOCK WITH R25

B 5. CHANGE B EFFECTIVE ON S/N 349 & UP, CR9 & CR10 ADDED

A 4. CHANGE A EFFECTIVE ON S/N 312 & UP, R25 & F1 ADDED

3. MATING PLUG FOR J1: MS 3106B 18-9S, S/N 312 & UP

2. CAPACITORS IN µF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 µF

REV. 1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.2

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
B		6/22/66		
A		1-26-72		

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL .XX ± .03 .XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± .5°

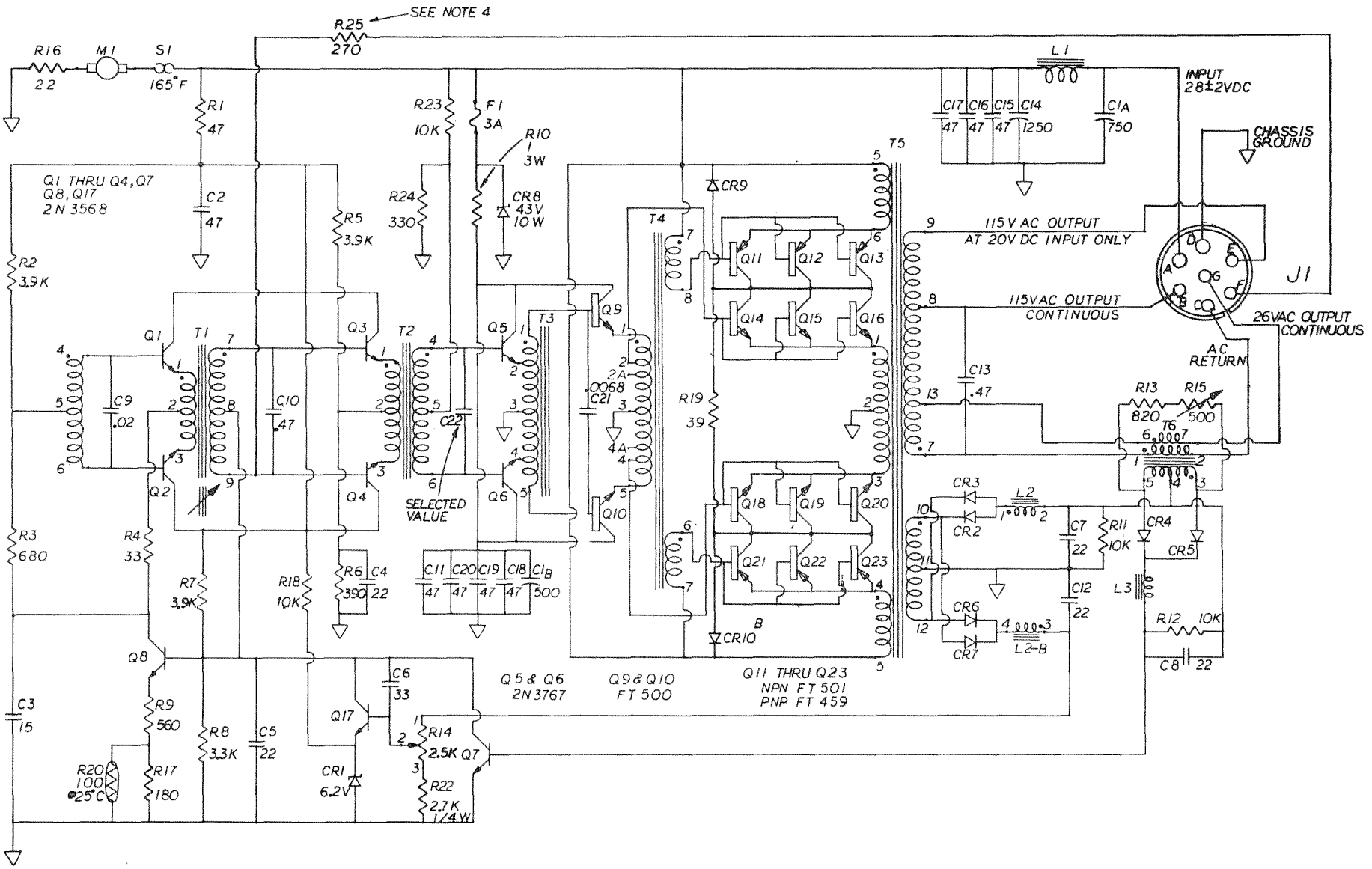
ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D

MAT'L

FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15
SCHEMATIC

DRAWN		10/1/67
CHK'D		
APPR'D		10/1/67
SCALE		
MODEL	PC15	
NEXT ASSY.		
SIZE C	DWG. NO. 91003	



4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S,
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D	ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03, XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± .5°

MAT'L

FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15A
SCHEMATIC

DRAWN 10/1/67
CHK'D
APPR'D 10/1/67
SCALE
MODEL PC15A
NEXT ASSY.
SIZE C DWG. NO. 91003-1

Transformer T1 has a tuning slug which is adjusted at the factory for an oscillator frequency of 400 HZ.

Transistors Q1 and Q2 are the class B push-pull amplifier to sustain oscillation. Resistors R2 and R3 biases the transistors to cause oscillation to start. Capacitor C9 suppresses any tendency for high frequency mode oscillation. Resistor R4 is the degenerating resistor.

The output winding 7-8-9 drives the bases of Q3 and Q4 in opposite phase.

3.4 Low Level Amplifiers

Between the sine wave oscillator and power amplifiers, there are three stages of class B push-pull emitter follower amplifiers.

The first stage consists of transistors Q3 and Q4 and the interstage transformer T2. Resistors R5 and R6 biases the transistors operating point.

The output from the transformer T2 drives the bases of Q5 and Q6. Resistors R24 and R23 biases transistors Q5 and Q6. Transistors Q5 and Q6 emitters drive the matching autotransformer T3. By using an autoformer connection for T3, the unit is designed compactly and yet permits proper step-up to drive transitors Q9 and Q10. Capacitor C22, a selected value connected across 4 and 6 of T2, is used to suppress ringing.

Capacitor C21 connected to the base of Q9 and Q10 suppresses parasitic oscillation. The emitter of Q9 and Q10 drives transformer T4. Transformer T4 delivers proper voltage and current to the final power output transistors.

Decoupling network for the oscillator stage and first low level amplifier is R1 and C2. Decoupling network for the intermediate stage is R10.

Zener CR8 clips transient voltage above 43 VDC.

3.5 Power Amplifier

The power amplifier consists of power transistors connected in cascaded pairs. Transistors Q11 through Q16 and Q18 through Q23 are driven in alternate half cycles. The multiple winding primary of transformer T5 divides the 28.0 VDC input, so the transistors support 26.75 peak AC signal.

These power transistors are controlled to Flite-Tronics' specifications. These devices are inspected for certain minimum breakdown voltage, gain and recovery time. Therefore, an 88 volt peak transient on the 28.0 VDC input will not cause a collector to emitter voltage to exceed the minimum breakdown voltage. The primaries of the transformer forces this voltage division. In spite of the unusual connection of transistors Q11 through Q23, they are connected for class B push-pull amplifier.

The tapped secondary of T5 delivers 26 VAC from terminal 13, and 115 VAC from terminal 8. (Model PC-15A only)

The output from terminal 19 is 115 VAC working into 90% of rated load, during an input of 20 VDC on the A+ line.

This output is to be used only during emergency 20 VDC input condition and the load should be connected to pin E of J1. There will exist, however, a slight squaring of the peaks of the sine wave in this condition.

Capacitor C13 is the phase compensating capacitor to permit the unit to operate efficiently with a load power factor between .8 lag and 1.0.

3.6 Output Voltage Control

The output voltage sample is realized from the center tapped winding 10-11-12 of T5. Rectifiers CR6 and CR7 converts the AC signal to a DC output. Filter consisting of L2-B and C12 is the L section choke input to give an average DC output which is proportional to the 115 VAC level.

This DC output is also applied across a variable resistor R14 in series with R22. The variable portion of the resistor is connected to the base of Q17. In essence, this output voltage sample is compared with the zener CR1 in the emitter of Q17. Resistor R18 is the bleeder resistor to the zener to permit operating this zener on its flat portion of its transfer characteristics curve.

The variable resistor R14 is adjusted for an output of 115 VAC. A common load resistor R7 is connected to the collector of Q7 and Q17. The DC current passing through R7 determines the bias point for transistor Q8. Transistor Q8 is the variable DC source for the push-pull 400 HZ oscillator.

The push-pull oscillator represents an impedance to the collector circuit of Q8. Hence, the conduction of Q8 will determine the magnitude of DC voltage across the oscillator circuit. This, in turn, determines the amplitude of oscillation, which controls the AC output level. Resistor R9 and R17 are the degenerating resistors for transistor Q8.

Thermistor R20 is a temperature compensating resistor.

Resistor R8 is the starting resistor for transistor Q8 until the oscillator amplitude builds up sufficiently for the automatic level control circuitry to take over.

Capacitor C6 is a low frequency feedback capacitor to prevent the automatic level control circuitry from motor boating. Capacitor C3 and C5 are simply by-pass capacitors.

3.7 Output Overload Control

The output AC current is sampled by the transformer T6. The current flowing through the winding 1-2 causes a voltage to be developed across the center tapped winding 3-4-5. The magnitude of voltage across this winding is controlled by the variable resistor R15 in series with R13.

The AC voltage from winding 3-4-5 is rectified by CR4 and CR5. The averaging choke input filter, consisting of L3 and C8, develops a DC voltage across R12, which is proportional to the output AC current. For the Model PC-15A, the 26 VAC output current is sampled by winding 6-7 of transformer T6.

To realize an overload that causes quenching action, the overload current resulting in DC voltage across R12 is compared with the output DC voltage across R11. This tends to give a trigger-like action when an overload condition is sustained.

The output voltage sample is taken from winding 10-11-12 of transformer T5. CR1 and CR3 rectifies this voltage. The L section choke input filter, consisting of L2 and C7, places across resistor R11 a ripple-free DC voltage. The voltage across R11 is a negative polarity with respect to ground.

The DC voltage across R12, which is proportional to the output current, is compared with the voltage across resistor R11. When the output current causes a voltage across R12 to exceed the compared voltage across R11, transistor Q7 will start conducting. The extent of overload determines the magnitude of current Q7 will conduct. As Q7 conducts, this tends to cut off Q8, which, in turn, decreases the voltage across the 400 HZ oscillator circuit.

When the load is in excess of 165% of 250 VA, the oscillator circuit will exhibit anything from low frequency quenching to almost a complete shut down.

During output short circuit, the current overload circuitry will reduce the voltage across the push-pull oscillator until a feeble oscillation is maintained.

Of course, on removal of the short circuit condition, the unit will immediately return to normal operating condition.

3.8 Input Filtering and Blower

The input is filtered by a pi section filter, consisting of capacitors C1A, C14 through C17 and choke L1.

Additional filtering for the low level stage is done by the RC filter, consisting of R1, C2, and R10, C1B, C11, C18 through C20.

Blower motor M1 is thermostatically controlled and used for protection only. The blower motor turns on when the heat sink temperature exceeds 165° Fahrenheit.

In normal installation where thermal conduction by the aircraft structure is adequate, the blower motor may never come on. Resistor R16 simply reduces the speed slightly to measurably increase the life of the blower.

F1 fuses the intermediate amplifier stages.

3.9 Transient Protection

To eliminate deleterious effects of voltage transients, zener and diodes are used.

Transient voltage passing through the A+ input filter section and exceeding 43 volts are clipped by the zener diode CR8.

Transient voltage occuring at the junctions of the power output transistors exceeding the input voltages are clipped by diodes CR9 and CR10.

3.10 Phase & Frequency Locking

When the PC-15s are paralleled together, it is necessary to phase synchronize the output voltage. Resistor R25 is the coupling resistor to phase lock the oscillator together through pin F of J1.

When the PC-15s are paralleled, it is necessary to have all the parallel units operating. The loading effect of the non-operating unit causes the other parallel unit or units to shut down. Refer to page 11 for remotely disconnecting non-operating unit.

To frequency lock the PC-15s to other 115 VAC sources, resistor R25 is changed to C23. Typically .0047 ufd, as shown in the bill of material may be used.

When PC-15s are frequency locked, the output should not be paralleled to the 115 VAC source.

NOTE TO SECTION IV

N4.1 Pages for changes and additions to this section due to revision and introduction of new model series are listed below for quick reference.

REV. NO/MODEL SERIES	PAGE
Rev. 1, 2, 3	Incorporated
Rev. 4	55, 56
Rev. 5	Incorporated
Rev. 6	58, 61
PC-15B	A1, A2, A3, A4, A5, A6
PC-15D	A6
PC-15E	A6
PC-15F	A13
PC-15G	A13

N4.2 Addition to N4.1

Rev. 7	63
PC-15B( ) Series	63

N4.3 Any reference to PC-15 or PC-15A in this section is applicable to Model PC-15B() unless otherwise noted under Model PC-15B.

Section IV

Maintenance

4.1 General

This section covers the bench check of the PC-15s to determine conformance to manufacturers specification. Periodic preventative maintenance is not necessary, since no moving parts are employed to realize functional electrical performance.

For safety feature only, a thermostat is used to control the blower motor. It will come on only when the heat sink temperature exceeds 165°F.

Table 4.2, page 23, is used to functionally check the PC-15s to manufacturers performance.

The instructions on table 4.3 will aid in localizing the cause of defective operation, should any component fail.

4.2 Test Equipment

Table 4.1 lists the recommended components and test equipment to be employed in conducting electrical test per manufacturers test procedures.

Figure 4.1 illustrates the bench test inter-connection diagram. The Flite-Tronics Test Set TS15-1 is a unit for readily conducting the test in table 4.2 and 4.3. Table 4.2 indicates the readings and step-by-step procedure to test PC-15s operating normally. Table 4.3 notes test procedure and possible cause of abnormal reading.

Table 4.1 Component and Test Equipment

EQUIPMENT	MODEL OR TYPE	FUNCTION
Power Supply	0-40 VDC, 0-25 Amp	Low voltage power source
Oscilloscope	HP122A or equiv.	Visual display
Distortion Analyzer	HP330B or equiv.	Measure distortion
Frequency Counter	HP5512A or equiv.	Measure frequency
Components for TS15-1 Test Set		
Circuit Breaker	25 Amp Breaker	Protection
Current Meter 12	0-5.0 Amps AC 400 HZ	Monitor output I
Voltmeter V2	0-50/0-150 VAC 400 HZ	Monitor output voltage
Reactor L1	12.7 Millihenry @115 VAC 400 HZ	Reactance load simulator
Resistor R1	1.6K ohm 25 watt	Resistive load
Resistor R2	100 ohm 100 watt	Resistive load

Component and Test Equipment (continued)

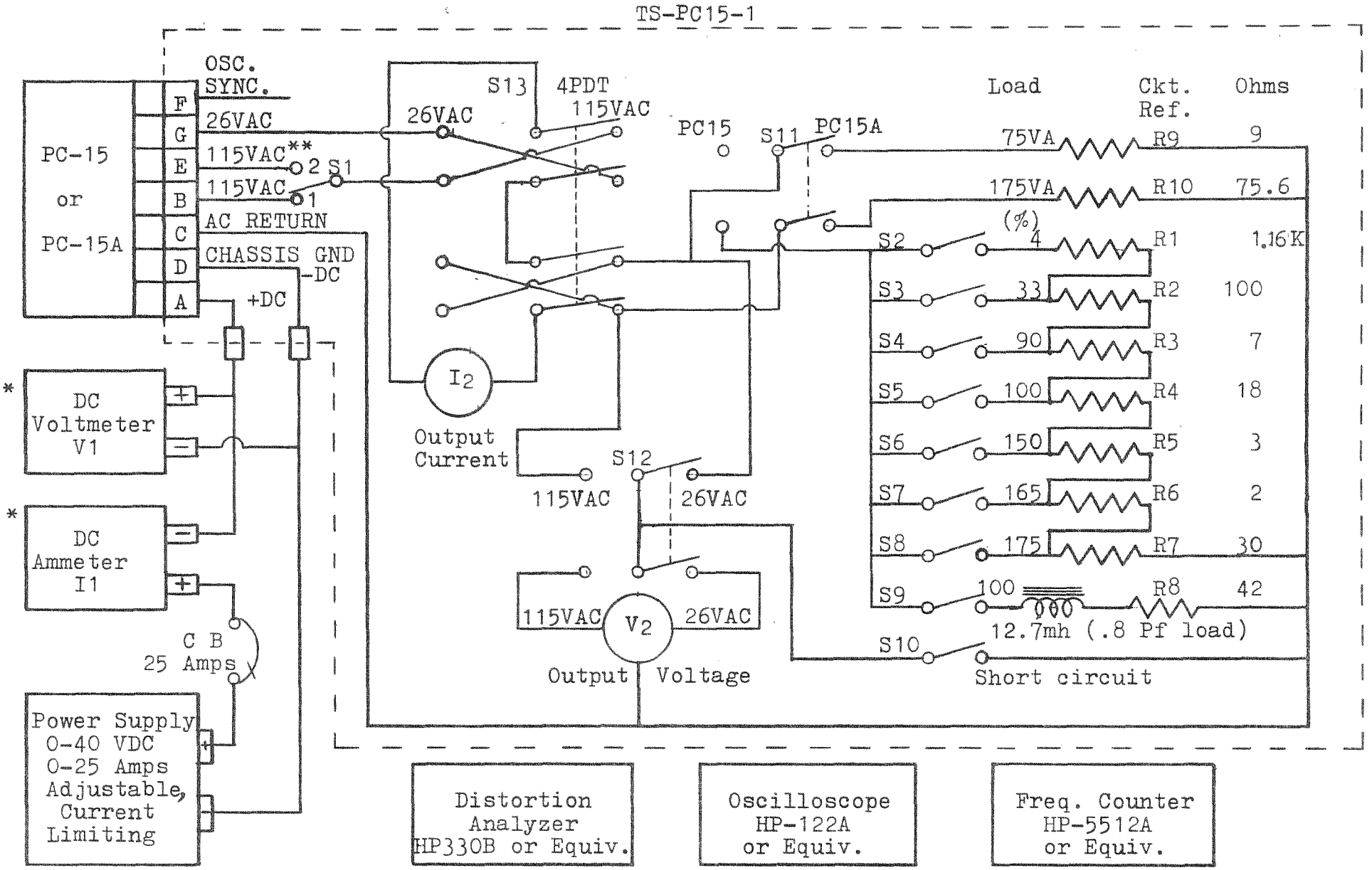
EQUIPMENT	MODEL OR TYPE	FUNCTION
Resistor R3	7 ohm 100 watt	Resistive load
Resistor R4	18 ohm 250 watt	Resistive load
Resistor R5	3 ohm 100 watt	Resistive load
Resistor R6	2 ohm 100 watt	Resistive load
Resistor R7	30 ohm 750 watt or equiv.	Resistive load
Resistor R8	42 ohm 500 watt or equiv.	Resistive load
Resistor R9	9 ohm 150 watt	Resistive load
Resistor R10	75.6 ohm 350 watt or equiv.	Resistive load
Switch S1	SPDT	20 VDC input switch
Switch S2	SPST	4% load switch
Switch S3	SPST	33% load switch
Switch S4	SPST	90% load switch
Switch S5	SPST	100% load switch
Switch S6	SPST	150% load switch
Switch S7	SPST	165% load switch
Switch S8	SPST	175% load switch
Switch S9	SPST	.8 power factor switch
Switch S10	SPST	Short circuit switch
Switch S11	DPDT	PC-15/PC-15A load selector switch
Switch S12	DPDT	Output voltage selector switch
Switch S13	4PDT	Output current selector switch

4.3 Performance Test and Localizing Trouble Source

Table 4.3 outlines a step-by-step procedure to performance test the PC-15s to localize fault source, if troubles exist.

It is suggested the technician acquire familiarity of the unit by studying the principles of operation section prior to attempting this section.

In table 4.3, test 1 through 14 is valid for the Models PC-15 and PC-15A. Test 15 and 16 are for the Model PC-15A only.



*These meters are required only if the power supply does not contain them.
**Emergency output at 20 VDC input only.

FIGURE 4.1 BENCH TEST SET AND HOOK-UP

4.4 Check Procedure for PC-15 and PC-15A

To functionally test Flite-Tronics Static Inverter connect the PC-15 or PC-15A to the test rack TS-PC15-1.

A. Model PC-15: 1 output; 115 VAC, 400 Hz, 250 VA Max.
B. Model PC-15A: 2 outputs; 115 VAC, 400 Hz, *250 VA Max.
26 VAC, 400 Hz, *75 VA Max.
C. Frequency: 400 Hz ± 4 Hz, both Models.
D. Amplitude Distortion: 7% or less under normal operating conditions, both Models.
E. Tests for 115 VAC output of PC-15 and PC-15A are identical.
*Sum of powers from the 115 VAC and 26 VAC outputs should not exceed 250 VA.

*Table 4.2 Test Conditions and Typical Readings

Model	Condition	Switch	Position	Typical Readings			
				DC Input		AC Output	
				Voltage	Current	Voltage	Current
PC-15 or PC-15A	No load	S1 S2 thru S10 S11 S12 & S13	#1 Off PC15 115 VAC	Set to 28 VDC	.75 Amps or less	120.7 VAC maximum	0 Amp
PC-15 or PC-15A	4% load	S1 S2 S3 thru S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	2.0 Amps maximum	Between 115 VAC and 120.7VAC	.1 Amps maximum
PC-15 or PC-15A	33% load	S1 S3 S2 & S4 thru S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	5.0 Amps typical	Between 115 VAC and 120.7VAC	.72 Amps typical
PC-15 or PC-15A	100%	S1 S5 S2 thru S4 & S6 thru S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	14 Amps typical	Between 108 VAC and 120.7VAC	2.17Amps typical
PC-15 or PC-15A	150% overload	S1 S6 S2 thru S5 & S7 thru S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	22 Amps typical	At least 107 VAC	3.3 Amps typical
PC-15 or PC-15A	165% overload	S1 S7 S2 thru S6 & S8 thru S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	24 Amps typical	At least 100 VAC	3.6 Amps typical
PC-15 or PC-15A	175% overload	S1 S8 S2 thru S7 & S9 & S10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	Between 5.0 Amps and 13 Amps	Output voltage & current motor-boating typically @ 60 VAC and @ 2.2 Amps	

*Table 4.2 additions for Pc-15B
See page A2

4.4 Check Procedure for PC-15 and PC-15A (Continued)

Model	Load Condition	Switch	Position	Typical Readings			
				DC Input		AC Output	
				Voltage	Current	Voltage	Current
PC-15 or PC-15A	100% Reactive Load	S1 S9 S2 thru S8&10 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	14 Amps typical	Between 107 VAC and 120 VAC	Between 2.2 Amps and 2.5 Amps
PC-15 Only	Output Short Circuit	S1 S10 S2 thru S9 S11 S12 & S13	#1 On Off PC15 115 VAC	Set to 28 VDC	3 Amps or less	0 VAC	1 Amp or less
PC-15 or PC-15A	Pin E Output @20 VDC Input	S4 S1 S5 thru S10 S11 S12 & S13	On #2 Off PC15 115 VAC	Set to 20 VDC	15 Amps typical	Between 107 VAC and 115 VAC	1.95Amps typical
PC-15A Only	*Full load 175 VA @115 VAC	S1 S2 thru S10 S11 S12 & S13	#1 Off PC15A 115 VAC	Set to 28 VDC	14 Amps typical	Between 107 VAC and 120 VAC	1.5 Amps typical
	75 VA @26 VAC	S1 S2 thru S10 S11 S12 & S13	#1 Off PC15A 26 VAC	Set to 28 VDC	14 Amps typical	Between 24.2VAC and 27.3VAC	2.9 Amps typical
	Output Short Circuit Test 26 VAC	S1 S2 thru S10 S11 S12 & S13 S10	#1 Off PC15A 26 VAC On	Set to 28 VDC	3 Amps or less	0 VAC	8 Amps initial transi-ent,2Amp typical
	115 VAC	S1 S2 thru S10 S11 S12 & S13 S10	#1 Off PC15A 115 VAC On	Set to 28 VDC	3 Amps or less	0 VAC	1 Amp or less

* S11 in PC-15A position, 175 VA resistive load is connected to 115 VAC output and 75 VA resistive load is connected to 26 VAC output.

4.4.1 Switch Nomenclature:

S1 115 VAC normal and emergency output selector switch; position #1 normal, position #2 emergency, when input power is 20 VDC
S2 4% Resistive load switch
S3 33% " " "
S4 90% " " "
S5 100% (250VA) Resistive load switch
S6 150% Resistive load switch
S7 165% " " "
S8 175% " " "
S9 100% Reactive load switch
S10 Output short circuit switch for 115 VAC or 26 VAC - the AC voltmeter indicates output being shorted
S11 PC-15 and PC-15A output selector switch
S12 Output voltage selector switch. 115 VAC or 26 VAC
S13 Output current selector switch. 115 VAC or 26 VAC current

Table 4.3 Performance Test and Localizing Trouble Procedures

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
1	Interconnect unit per bench test hook-up	a) Turn on power supply, keep input voltage set at zero. b) Turn on all measuring equipment for warm-up. c) Check polarity of power supply. d) Set S1 to No. 1 position. e) Set switches S2 through S10 in the Off position.		
2	S2 through S10 in the Off position S11 in the PC-15 position S12 & S13 in the 115V position	a) Gradually increase power supply voltage to 27.5 VDC	Input DC current I1 should not exceed 3/4 amps DC	Test set-up incorrectly connected. Capacitor C1A, C1B, C11, and C14 through C20 may be shorted. Transistors Q9 through Q23 shorted. C2 or CR8 shorted.
3	S2 through S10 in the Off position S11 in the PC-15 position S13 in the 115V position	a) Input voltage set at 27.5 VDC b) Adjust R14 as required, so V2 reads 117 VAC if necessary	V2 should read between 107 VAC to 120.7, with S12 in the 115 VAC position. V2 should read between 24.2 to 27.3 VAC with S12 in the 26.0 VAC position for the PC-15A only.	Check for following likely defective components: CR6, CR7, C12, R14, C6, CR1, Q17, C3, Q8, and R20

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
4	S2 through S10 in the Off position S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC. b) If frequency is out of tolerance, adjust turning slug on transformer T1.	Frequency meter should read 400 HZ ± 4 HZ I1=3/4 A	Defective parts likely to cause abnormal reading: Transformer T1, Capacitor C10 or C9
5	S2 through S10 in the Off position S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC. b) Vary input voltage between 26 to 30 VDC.	Distortion meter should read less than 7%. I1=3/4 A	Defective parts likely to cause abnormal reading: Transistors Q3 through Q6 and Q9 through Q23. Capacitors C3, C5.
6	Switch S5 on for full load output S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC. b) Resistor R14 may require readjusting; however, if adjusted, step 3 should be re-tested. c) Vary input voltage between 26 to 30 VDC.	I2 read 2.17 amps AC V2 should read between 107 to 120.7 VAC. I1 should read approximately 14.2 A. Frequency should be 400 HZ ± 4 HZ Distortion less than 7%.	Defective parts likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Transistor Q1 through Q17.

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
7	Switch S6 for 150% overload test. S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set 27.5 VDC. b) Resistor R15 may require adjusting if unit tends to motor boat. However, in the event of any adjustment, step 3 should be repeated.	I2 should read approximately 3.25 amp. V2 should read at least 107 VAC. I1 should read approximately 22.0 amps.	Defective parts likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Transistor Q1 through Q17.
8	Switch S7 on for 165% overload test S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC. b) R15 adjust the overload threshold point. The proper setting is at the 165% overload point; the unit should almost start motorboating.	I1 should read 24 amps. V2 should read at least 95 VAC. I2 should read approximately 3.6 amps.	Defective components likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Capacitors C7 and C8. Transistors Q7 and Q8.
9	Switch S8 on for 175% overload test S11 in the PC-15 position S12 and S13 in the 115V position	a) Input set at 27.5 VDC. b) R15 adjust the overload threshold point. The proper setting at 175% overload point, the PC-15 should be in the motorboating mode.	I1 should be motorboating between 1.0 to 10 amps. I2 and V2 should indicate output current and voltage is motorboating.	Defective components likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Capacitors C7 and C8. Transistors Q7 and Q8.
10	Switch S10 on for output short circuit test S11 in the PC-15 position S12 and S13 in the 115V position	a) Input set anywhere between 26 and 28 VDC. b) If I1 exceeds 6 amps at anytime, the unit should be turned off.	I1 less than 6 amps. V2 = zero I2 less than 1 amp.	Defective components likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Capacitors C7 and C8. Transistors Q7 and Q8.

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
11	Switches S2 through S8 in the Off position Switch S9 on 250 VA S10 in Off position S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC. b) Vary input voltage between 28 to 30 VDC.	I2 read 2.0 to 2.3 amps AC. V2 read between 107 to 120.7 VAC.	Defective parts likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Transistor Q1 through Q17. Capacitor C13.
12	Switch S3 on and S4 through S10 in Off position for 33% load test S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage set at 27.5 VDC.	I1 read 5.0 amps. I2 read .72A V2 read between 117 to 120.7 VAC. Distortion meter should read less than 7%. Frequency meter should read 400 HZ ± 4 HZ.	Defective parts likely to cause abnormal reading: Transformer T1. Capacitor C3, CR5 and C10. Transistors Q3 through Q6 and Q9 through Q16.
13	Switch S2 on. Switch S3 through S10 in Off position S11 in the PC-15 position S12 and S13 in the 115V position	a) Input voltage between 26.0 to 28 VDC	Distortion less than 7%. Frequency 400 HZ ± 4 HZ. V2 read 115 to 120.7 VAC. I1 read 2 amps DC. I2 read .20 to .35 amps AC.	Defective parts likely to cause abnormal reading: Diodes CR6, CR7, C12, R14, C6, CR1, Q17, C3, Q8 and R20.

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
14	Switch S1 to #2 position. S4 on, and S5 through S10 in Off position S11 in the PC-15 position S12 and S13 in the 115V position	a) Set input voltage at 20 VDC.	V2 read 107 to 120.7 VAC. I2 read 1.93 to 2.12 amps AC. I1 read approximately 15.0 amps DC.	Defective parts likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Transistor Q1 through Q17.
15	Switch S1 to #1 position Switch S11 in the PC-15A position	a) Input voltage set at 28.0 VDC.	I1 should read approximately 14.2 amps. I2 read 1.52 amps, S13 in 115V position. I2 read 2.9 amps, S13 in 26V position. V2 should read between 107 to 120.7 VAC with S12 in 115V position. V2 should read between 24.2 to 27.3 VAC with S12 in 26V position. Distortion for 26 VAC and 115 VAC output should be 7% or less.	Defective parts likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Transistor Q1 through Q17.

STEP	SET-UP	PROCEDURE	PERFORMANCE READING	POSSIBLE CAUSE OF ABNORMAL READING
16	Switch S11 in the PC-15A position for output short circuit test S12 in the 26V position S13 in the 26V position	a) S10 switched on after unit is operating normally. b) If I1 exceeds 6.0 amps at anytime, the unit should be turned off.	I1 less than 6.0 amps. V2 reads zero. I2 less than 1.5 amps.	Defective components likely to cause abnormal reading: Diodes CR2, CR3, CR4 and CR5. Capacitors C7 and C8. Transistor Q7 and Q5. Resistor R15.

4.5 Voltage Measurement

To enable the technicians to effectively service the PC-15's table 4.4 tabulates the typical D.C. and/or A.C. voltage to assist in localizing a fault source.

Table 4.3 indicates the possible component for an abnormal reading. If a voltage other than those listed in table 4.4 is measured this will enable the technician to determine which component is possibly faulty.

TABLE 4.4 PC-15's VOLTAGE DISTRIBUTION MEASUREMENT CONDITION

1. Input 27.5 VDC.
2. Full load with Switch S5 on.
3. Switch S1 in the #1 position.
4. DC and AC measurement made with a Simpson 270 or equivalent.
   (Note: Make AC measurement in the output connection to this meter.)

CIRCUIT REF.	TEST POINT	VOLTAGE MEASUREMENT D.C.	VAC RMS	CIRCUIT REF.	TEST POINT	VOLTAGE MEASUREMENT D.C.	VAC RMS
Q1 and Q2	Emitter	8 to 20*	6				
	Base	8 to 20*	6	Q9, Q10	Emitter	.7	16
	Collector	26	0		Base	1.2	17
Q3 and Q4	Emitter	8.2	10		Collector	26	0
	Base	8.2	10	Q11, Q12, Q13	Emitter	27	8
	Collector	26	0	Q21, Q22, Q23	Base	26.5	8
					Collector	14	0 to 5
Q5 and Q6	Emitter	.5	16	Q14, Q15, Q16	Emitter	1	8
					Base	1	8
	Base	1.0	16	Q18, Q19, Q20	Collector	14	0 to 5
	Collector	26	0	Q17	Emitter	6 to 7.5	0

*These voltages are load dependent.

CIRCUIT REF.	POINT	VOLTAGE MEASUREMENT D.C.	VAC RMS
Q7	Emitter	0	0
	Base	-1.5 to -6*	0
	Collector	8 to 10	0
Q8	Emitter	8 to 9	0
	Base	8.2 to 9.2	0
	Collector	8 to 20	0

CIRCUIT REF.	POINT	TEST VOLTAGE MEASUREMENT D.C.	VAC RMS
Q17	Base	6 to 7.5	0
	Collector	8.2to9.2	0
CR2, CR3	Anode	0	10
CR6, CR7	Cathode	8	6
R11 and L2	Junction	-8.5	0
CR4, CR5	Anodes	0	0 to 9*
	Cathode	-9 to +1	6 to 0

*These voltages are load dependent.

4.6 Servicing Practice and Replacement

Section 5.0 lists the table of replaceable parts. Figures 5.1 thru figure 5.7 illustrates the location of these components.

When installing or removing transistors, semiconductor diodes and heat sensitive components, grasp the lead between the solder joint and the component with a thermal dissipator, such as a spring loaded copper clip or long nose pliers. This will bleed off the heat being applied at the solder joint.

A temperature controlled soldering iron is recommended for such use. The wattage rating of the iron should not be greater than 35 watts. Always work with an iron that the tip is well tinned so the soldering can be done quickly and cleanly.

Power transistors Q5, Q6, Q9, thru Q16 and Q18 thru Q23 are insulated from ground. The insulating is done by means of insulating washers made of fiber and mica. When replacing these transistors, be sure washers are replaced in proper order and coating the washers with a film of silicone grease is recommended.

After such replacement, check with an ohmmeter to see that the insulation is effective.

NOTE TO SECTION V

N5.1 Component changes, additions, and relocations due to revisions and introduction of new model series are listed under each revision number and model series in the addenda section.

Following pages should be consulted for above informations.

REV. NO/MODEL SERIES	PAGE
Rev. 1, 2, 3	Incorporated
Rev. 4	53, 54, 56
Rev. 5	Incorporated
Rev. 6	58, 59, 60, 62
PC-15B	A1, A4, A8
PC-15D	A10
PC-15E	A12
PC-15F	A13, A15
PC-15G	A13, A17

N5.2 Addition to N5.1

Rev. 7	63
PC-15B( ) Series	63

N5.3 Any reference to PC-15 or PC-15A in this section is applicable to Model PC-15B( ) unless otherwise noted under PC-15B.

Section V

Table of Replaceable Parts

5.1 General

This section illustrates and lists components that can be replaced for repair purposes. It is recommended that PC-15s requiring replacement of parts that are not listed in table 5.1, be returned to the factory for service.

Figures 5.1 through 5.7 illustrates the location of all the components that are listed in the Table of Replaceable Parts.

5.2 *Manufacturer's Code

Code	Name and Address
FT	Flite-Tronics Co., Inc. Burbank, California
KGS	K.G.S. Electronics, Inc. Pasadena, California
AB	Allen-Bradley Co. Milwaukee, Wisconsin
EI	Essex International Inc. Fort Wayne, Indiana
GUL	Gulton Industries, Inc. Metuchen, New Jersey
SAN	Sangamo Springfield, Illinois
NCI	National Capacitor Inc. West Palm Beach, Florida
ECI	Electro-Cube Pasadena, California
MOT	Motorola Phoenix, Arizona
FD	Fairchild Mountain View, California
DL	Diehl Mfg. Co. Finderne, New Jersey

(*Manufacturer may be substitued for equal or superior components.)

5.1 Manufacturer's Code (Continued)

Code	Name and Address
SEM	Semtech Newbury Park, California
W	Westinghouse Youngwood, Pennsylvania
SPG	Sprague Electric North Adams, Massachusetts
OHM	Ohmite Mfg. Co. Skokie, Illinois
BUS	Bussman St. Louis, Missouri
BR	Bourns Riverside, California
HTP	Hughes Semiconductor Newport Beach, California
IMB	IMB Electronic Products Inc. Santa Fe Springs, California

5.1 *Table of Replaceable Parts

CIRCUIT REFERENCE	QUANTITY	DESCRIPTION	SOURCE	FUNCTION
C1A, C1B, C14	2	Dual Capacitor 50 VDC 750-500 mfd 505-2052-02	SAN	Filter
C2, C11, C15 through C20	8	Capacitor 47 mfd 50 VDC HM47QD	NCI	Filter
C4, C5, C7, C8, C12	5	Capacitor 22 mfd 22 VDC HM22LD	NCI	Filter
C3	1	Capactor 15 ufd 30 VDC HM15MD	NCI	Filter
C6	1	Capacitor 33 ufd 15 VDC HM33JD	NCI	Filter
C9	1	Capacitor .02 ufd 200 VDC 210B	ECI	Bypass
C10	1	Capacitor .47 ufd 200 VDC 627A1C474J	ECI	Osc. cap.
C13	1	Capacitor .47 ufd 400 VDC 625B1E474M	ECI	Power factor Correction
C21	1	Capacitor .0068 to .01 ufd select 625B	ECI	Bypass
C22	1	Capacitor .00 to .0068 ufd select 200 VDC 625B	ECI	Bypass
C23	1	When used for frequency lock .0047 ufd 600 VDC 625B	ECI	Freq. lock
CR1	1	Zener 6.2 VDC 1 watt 1N4735	MOT	Reference Voltage
CR2, CR3, CR4, CR5, CR6, CR7, CR9, CR10	8	Silicon diode 200 piv 1N5393 or SC2	W SEM	Rectifier
CR8	1	Zener 43 VDC 10 watt 1N 2993A	MOT	Reference Voltage

(*Components may be substituted for equal or superior part.)

CIRCUIT REFERENCE	QUANTITY	DESCRIPTION	SOURCE	FUNCTION
F1	1	Fuse 3A GKN 3	BUS	Fuse
L1	1	Inductor FT #91027 KGS #343L	FT	Filter
L2-A, L2-B	1	Inductor FT #85102 KGS #287L	FT	Filter
L3	1	Inductor FT #85103 KGS #290L	FT	Filter
J1	1	Connector, receptacle MS3102A18-9P	CAN	Input Jack
M1	1	D.C. Motor SSFD6-21	DL	Blower
Q1, Q2	2	Transistor 2N3568	FAD	Push-Pull Osc.
Q3, Q4	2	Transistor 2N3568	FAD	Low Level Amp. Push-Pull
Q5, Q6	2	Transistor 2N3767	MOT	Push-Pull Interstage Amp
Q7, Q8, Q17	3	Transistor 2N3568	FAD	ALC and OL
Q9, Q10	2	Transistor FT500/501	FT	Push-Pull Driver
Q11, Q12, Q13, Q21, Q22, Q23	6	Transistor FT 459	FT	Output Push-Pull
Q14, Q15, Q16, Q18, Q19, Q20	6	Transistor FT500/501	FT	Output Push-Pull Power
R1	1	Resistor 47 ohm ± 10% ½ watt	AB	Filter
R2, R5, R7	3	Resistor 3.9 kilohm ± 10% ½ watt	AB	Bias
R3	1	Resistor 680 ohm ± 20% ½ watt	AB	Bias
R4	1	Resistor 33 ohm ± 20% ½ watt	AB	Bias, degenerating
R6	1	Resistor 390 ohm ± 10% ½ watt	AB	Bias, degenerating

CIRCUIT REFERENCE	QUANTITY	DESCRIPTION	SOURCE	FUNCTION
R8	1	Resistor 3.3 kilohm ± 20% ½ watt	AB	Bias
R9	1	Resistor 560 ohm ± 5% ½ watt	AB	Bias
R10	1	Resistor 1 ohm 5 watt wire wound 995-5B	OHM	Filter and degenerating, decoupling
R11, R12, R18, R23	4	Resistor 10 kilohm ± 20% ½ watt	AB	Loading
R13	1	Resistor 560 ohm ± 5% ½ watt	AB	Current Limiting
R14	1	Variable Pot 2.5K ½ watt		Level Control
		3067s-1-252	BR	
R15	1	Variable Pot 500 ohm ½ watt		Output Current Set
		3067s-1-501	BR	
R16	1	Resistor 22 ohm 3 watt wire wound 242E2205	SPG	Speed Reducer
R17	1	Resistor 180 ohm ± 10% ½ watt	AB	Degenerating
R19	1	Resistor optional 10 to 47 ohm ± 20% ½ watt	AB	Voltage Divider
R20	1	Thermister 100 ohm @ room temp. 21NE1	GUL	Temperature Compensating
R22	1	Resistor 2.7 kilohm ± 10% ¼ watt	AB	Level Control Divider
R24	1	Resistor 330 ohm ± 10% ½ watt	AB	Bias
R25	1	Resistor 270 ohm ± 10% ½ watt	AB	Osc. Phase Lock
S1	1	Thermostat 165° F. 430-545	EI	Temperature Sensing
T1	1	Transformer Adjustable FT 85076A KGS #524T-E	FT	Transformer Inductor 400 HZ
T2	1	Transformer FT91028 KGS #746T	FT	Input

CIRCUIT REFERENCE	QUANTITY	DESCRIPTION	SOURCE	FUNCTION
T3	1	Transformer FT91029 KGS #714T	FT	Interstage
T4	1	Transformer FT91030B KGS #715T	FT	Driver
T5	1	Transformer FT91135 KGS #849T	FT	Power Output
T6	1	Transformer FT91136 KGS #850T	FT	Output Current Sense

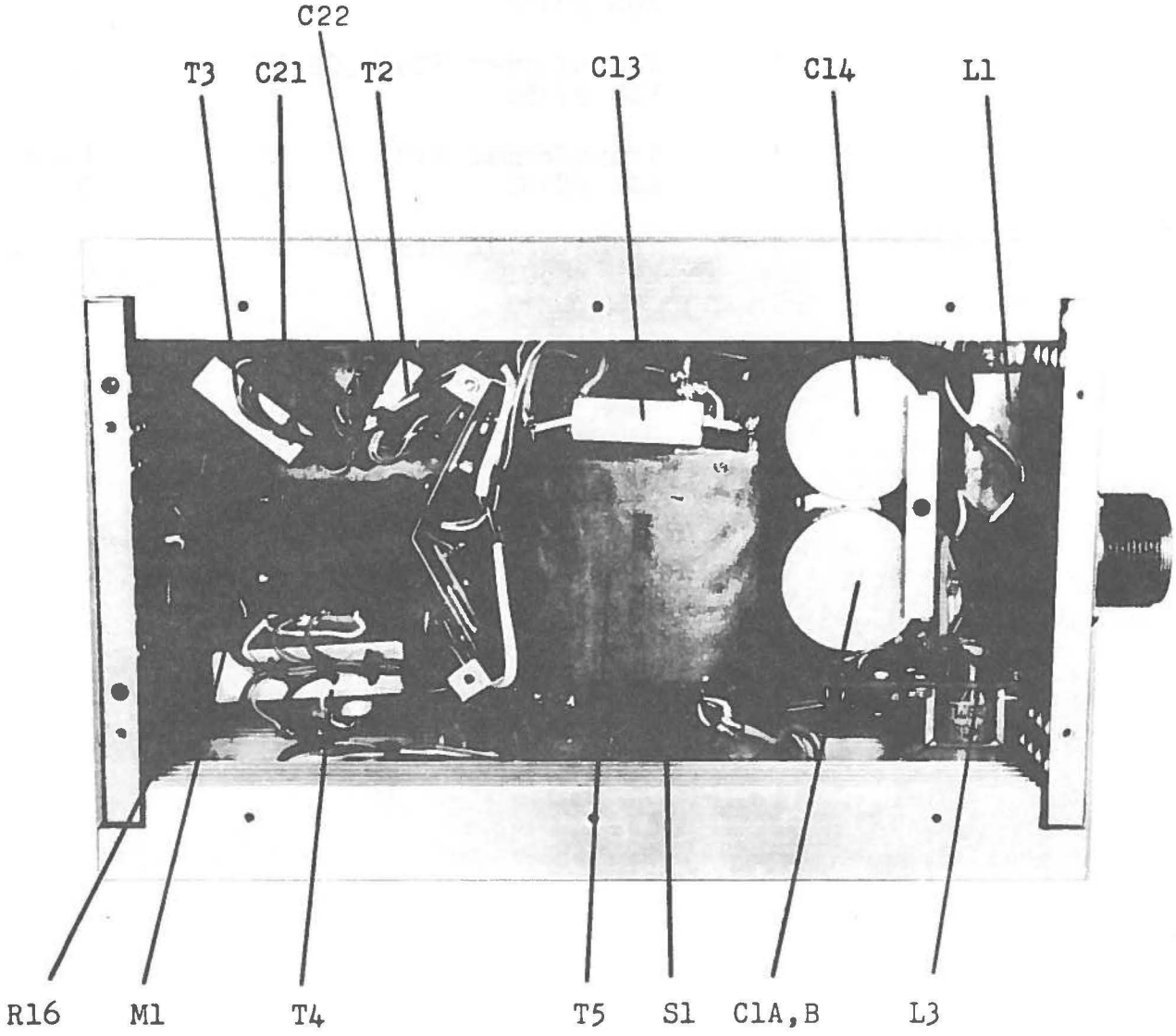


FIGURE 5.1 COMPONENT LAYOUT DUST COVER REMOVED

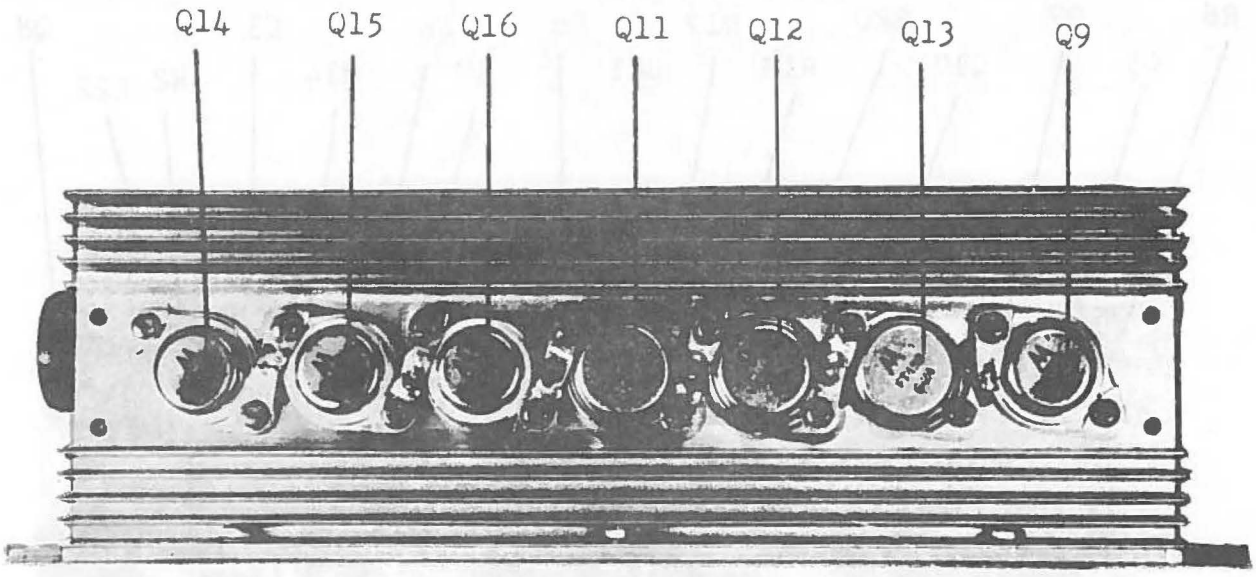


FIGURE 5.2 TRANSISTOR LAYOUT LEFT SIDE

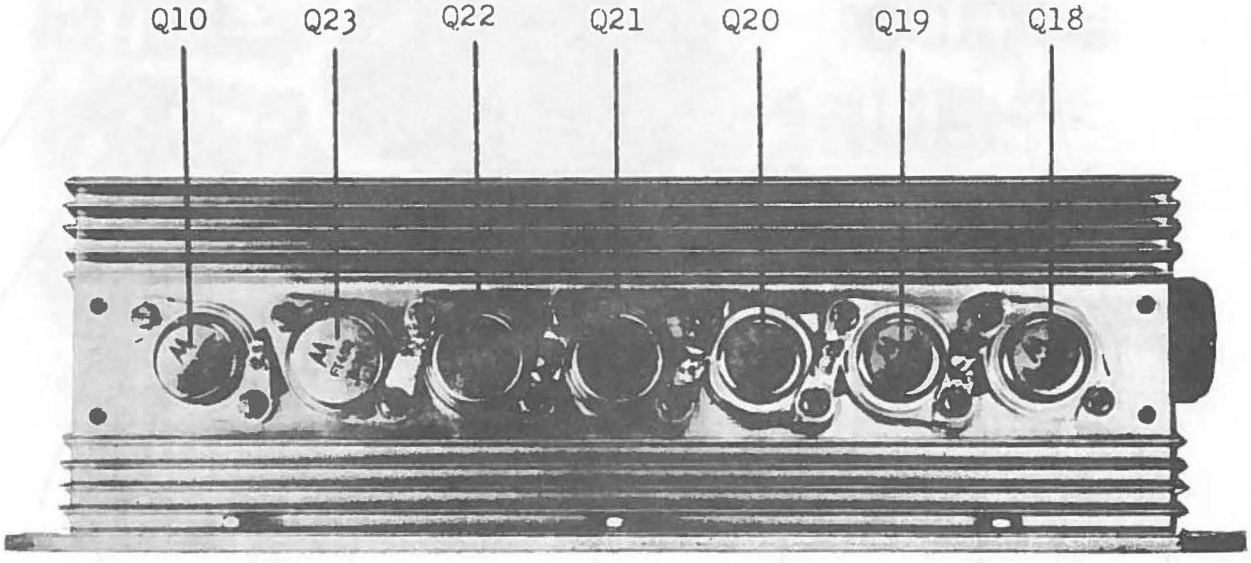


FIGURE 5.3 TRANSISTOR LAYOUT RIGHT SIDE

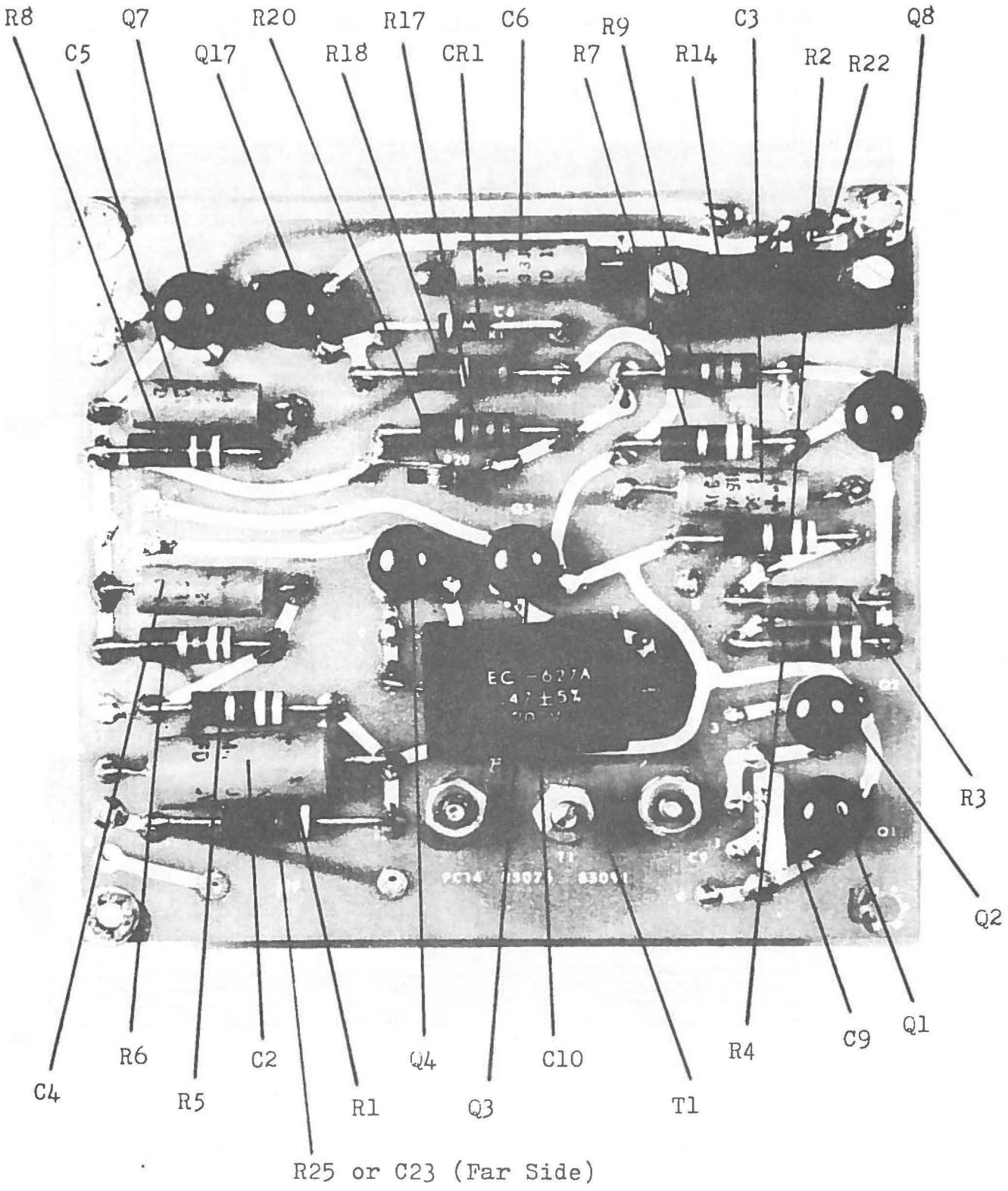


FIGURE 5.4 COMPONENT LAYOUT OSCILLATOR AND LOW LEVEL AMPLIFIER

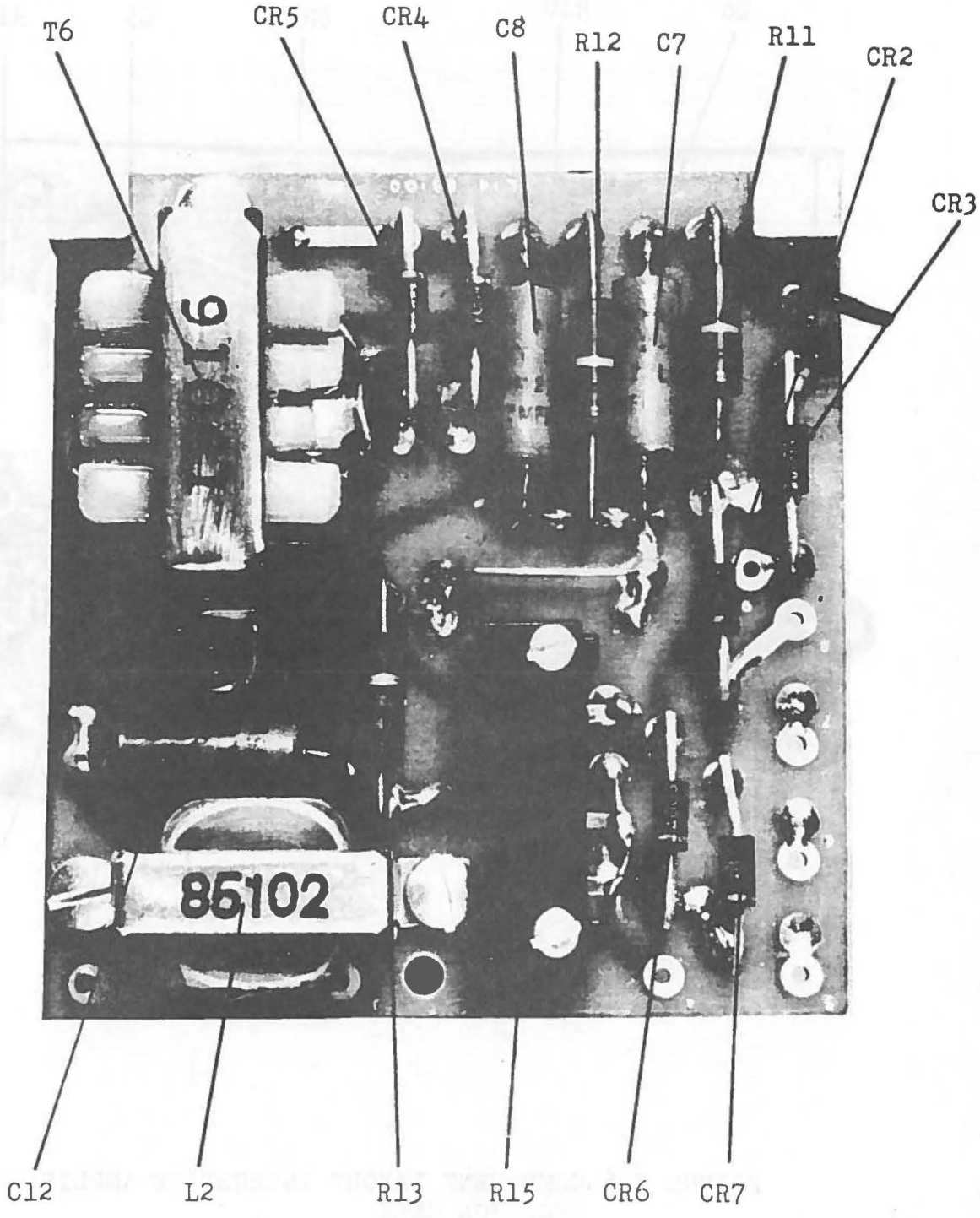


FIGURE 5.5 COMPONENT LAYOUT OL & ALC CIRCUIT

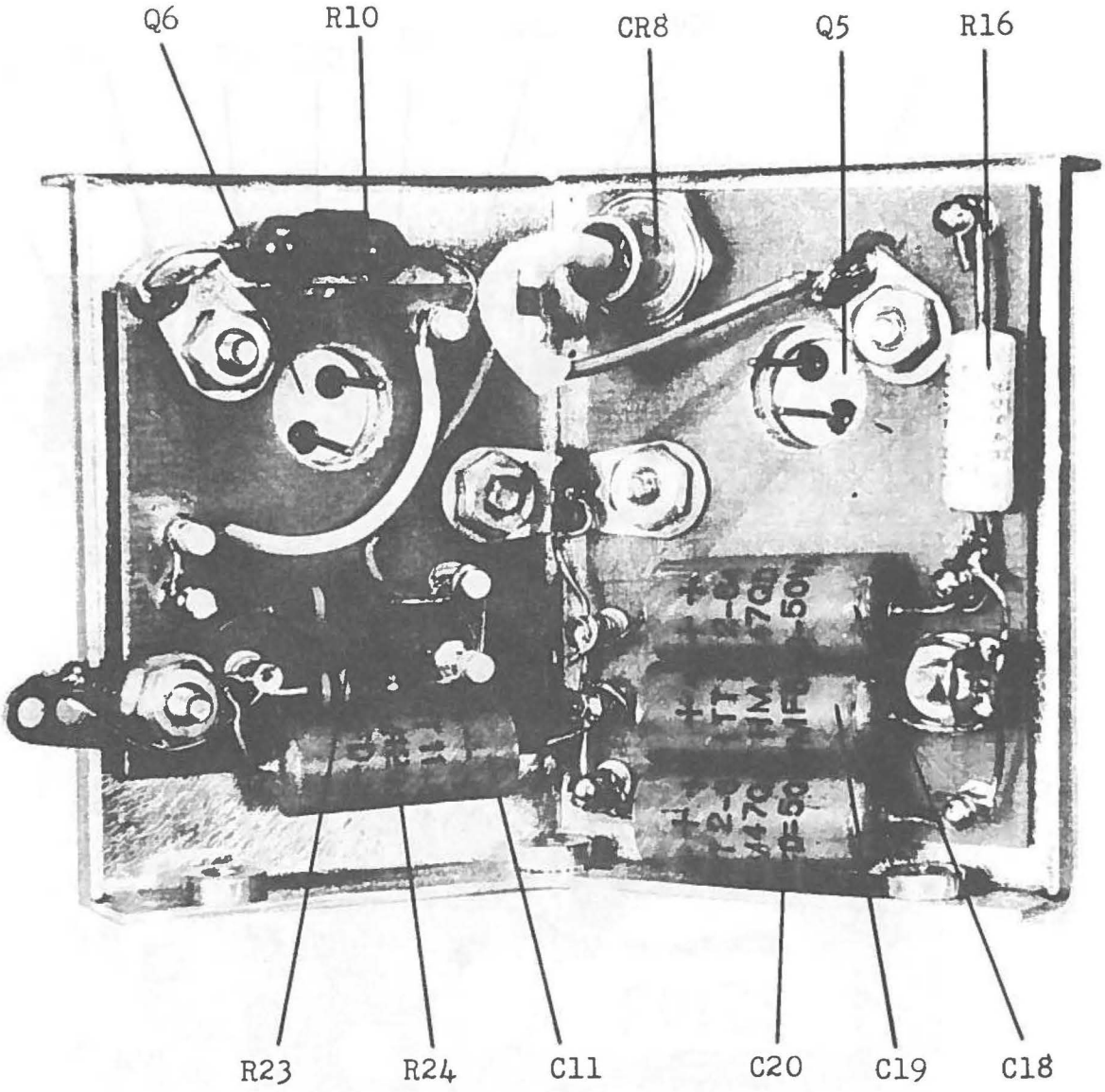


FIGURE 5.6 COMPONENT LAYOUT INTERSTAGE AMPLIFIER
LOCATION ONLY

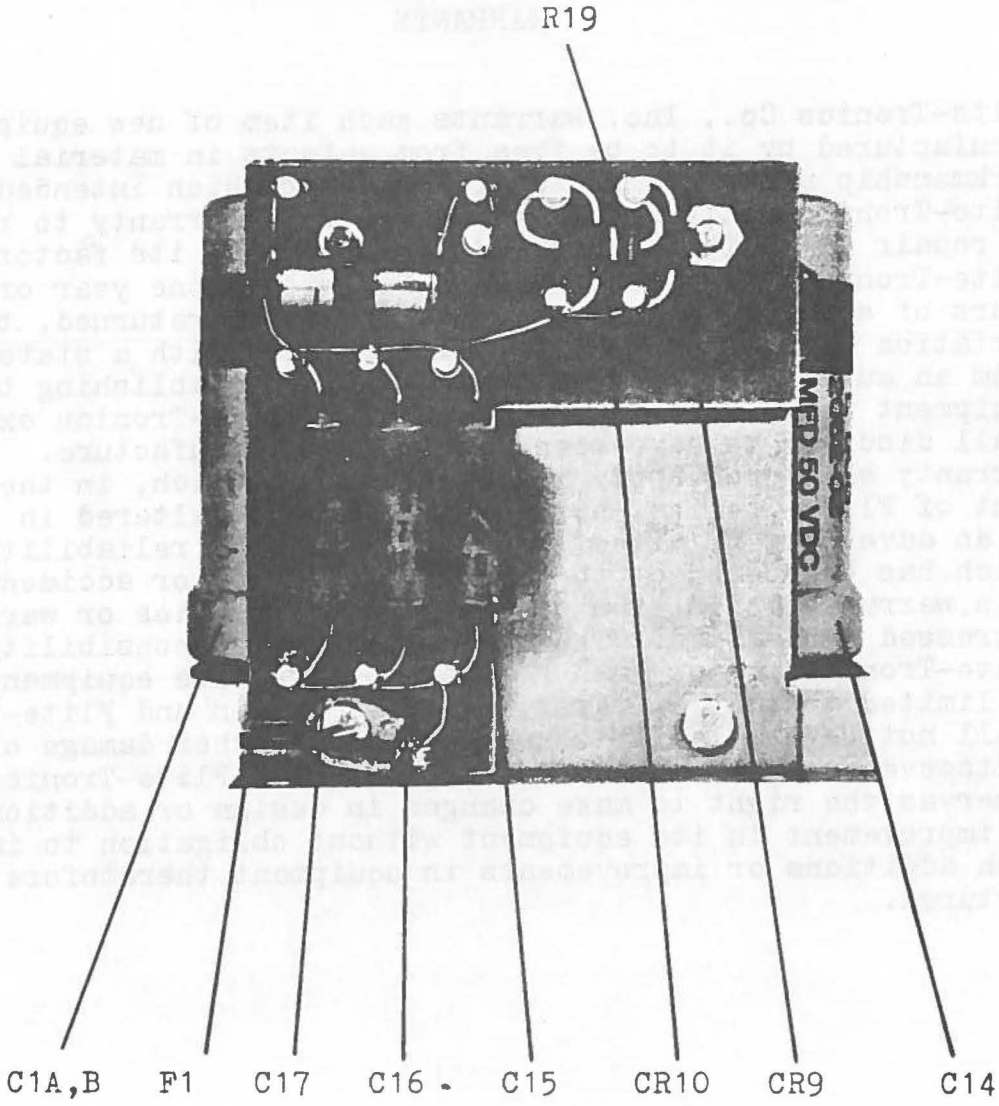


FIGURE 5.7 COMPONENT LAYOUT FILTER CAPACITOR

WARRANTY

Flite-Tronics Co., Inc. warrants each item of new equipment manufactured by it to be free from defects in material and workmanship under normal service use for which intended. Flite-Tronics obligates itself under this warranty to replace or repair (at Flite-Tronics' discretion), at its factory, any Flite-Tronics' equipment which shall within one year or 1,000 hours of service, whichever comes first, be returned, transportation charges prepaid to Flite-Tronics with a statement from an authorized Flite-Tronics' Dealer establishing the date equipment was placed in service, which Flite-Tronics examination shall disclose to have been defective in manufacture. This warranty shall not apply to any equipment which, in the judgment of Flite-Tronics, has been repaired or altered in any way so as adversely to affect its performance or reliability, or which has been subject to misuse, negligence or accident. This warranty is in lieu of all other guaranties or warranties expressed or implied. The obligation and responsibility of Flite-Tronics for or with respect to defective equipment shall be limited to that expressly provided herein and Flite-Tronics shall not be liable for consequential or other damage or expense whatsoever therefor or by reason thereof. Flite-Tronics reserves the right to make changes in design or additions to or improvement in its equipment without obligation to install such additions or improvements in equipment theretofore manufactured.

5.4 HOW TO ORDER REPLACEMENT PARTS

When ordering replacement parts, you should direct your order as indicated below and furnish the following information insofar as applicable.

ADDRESS: Flite-Tronics Co., Inc., Sales Service Department
3314 Burton Avenue
Burbank, California

INFORMATION NEEDED:

1. Quantity required.
2. Part Number (Obtain from parts list or schematic diagram.)
3. Type number and serial number of equipment.

5.5 HOW TO RETURN MATERIALS OR EQUIPMENT

If, for any reason, you should wish to return material or equipment, whether under warranty or otherwise, you should notify us, giving full particulars including the details listed below, insofar as applicable. Upon receipt of such notice, Flite-Tronics Co., Inc. will promptly advise you respecting the return. Failure to secure our advice prior to the forwarding of the goods, or failure to provide full particulars, may cause unnecessary delay in handling of your returned material.

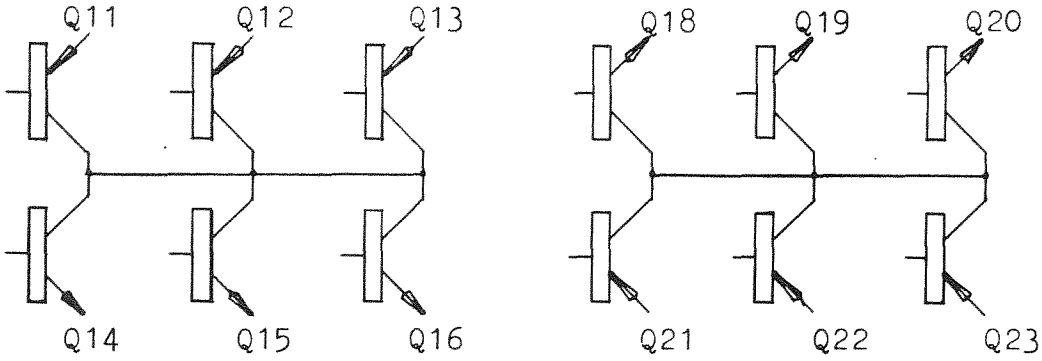
ADDRESS: Flite-Tronics Co., Inc., Sales Service Department
3314 Burton Avenue
Burbank, California

INFORMATION NEEDED:

1. Date of delivery of equipment.
2. Date placed in service.
3. Number of hours in service.
4. Part number (obtain from parts list or schematic diagram).
5. Type number and serial number of equipment.
6. Nature and cause of failure.
7. Remarks.

6.1 Revision No. 1

DESCRIPTION OF CHANGE	PAGE NO.
6.1.1 Electrical connection omission in the original manual.	14



Effectivity All Units

6.1.2 Note 4 Added 14

Resistor R25, Fuse F1
Effectivity
Serial number 312 and up.
Also including nos. 107, 120, 146, 155, 194, 201, 202, 225, 226, 229, 259, 261, 262, 276, 285 & 292.

6.1.3 Note 5 Added 14

Semiconductor diodes CR9 and CR10.
Effectivity
Serial number 349 and up.
Also including nos. 107, 120, 146, 155, 194, 201, 202, 225, 226, 229, 259, 261, 262, 285 & 292.

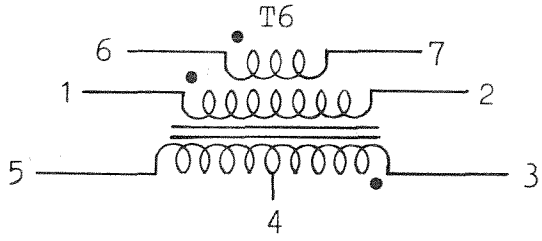
6.1.4 Note 6 Added 14

Use capacitor to frequency lock.
To other 115 VAC, 400 HZ line.
(C23 typically .0047 uf, 600V)
Phase lock with R25.

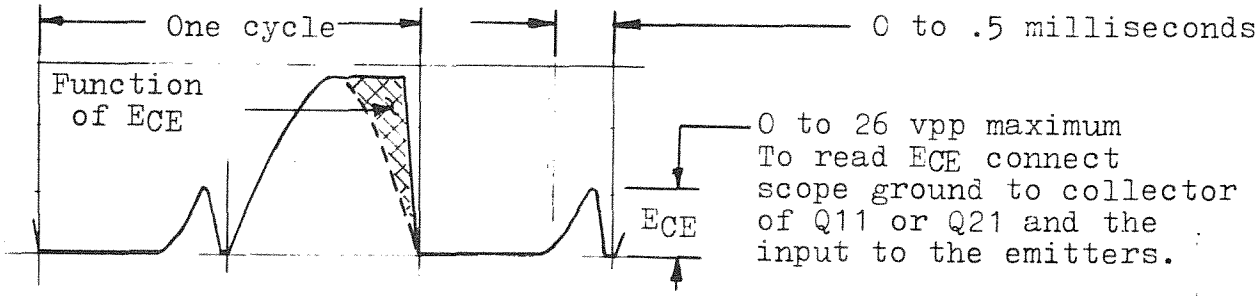
6.1.5 Note 7 Added 14

5 pin connector shown on Revision no. 1-5 Pin.

DESCRIPTION OF CHANGE	PAGE NO.
6.1.6 Revised: Call out of transistor type 2N3713 (Q14, Q15, Q16, Q18, Q19 & Q20) changed to FT501. (PC 15s may use either type.) When FT501 is used as a replacement or original installation, transistors Q14, Q15, Q16, Q18, Q19 & Q20 should all be the same device type. Also T4 is replaced with a FT91030B and connected per paragraph 6.1.10.	14
6.1.7 Revised: Call out of transistor type 2N3714 (Q9 & Q10) changed to FT500. (PC 15s may use either type.) When FT500 is used as a replacement or original installation, transistors Q9 & Q10 should be the same device type.	14
6.1.8 Semiconductor type call out for CR2 thru CR7 deleted.	14
6.1.9 Added: Schematic for secondary winding 6-7 to T6. Transformer FT91136 is a universal transformer and can be installed in place of FT91061. Winding 6-7 is used to sample the overload current for the 26.0 VAC output for the PC 15A.	14



6.1.10 Added: Taps 2A and 4A to transformer T4 and designated FT91030B. This tap addition changes this transformer to a universal type. Taps 2A and 4A are used when the h_{FE} of transistors Q14, Q15, Q16, Q18, Q19 & Q20 are high. i.e. greater than 100 @ 2.0 Amps with VCE 2.0 VDC. Tap is selected electrically to give the following collector to emitter (E_{CE}) wave shape across Q11 and Q21. 14, 39

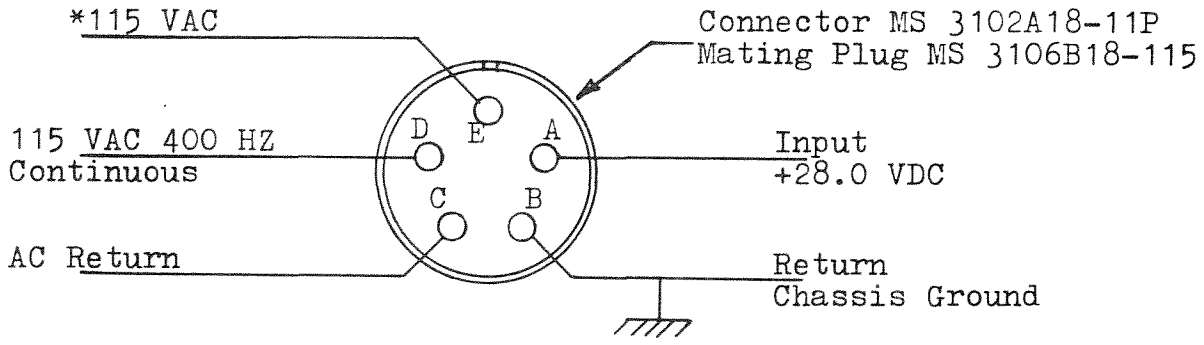


If E_{CE} is greater than 26.0 vpp it is recommended that the tap 2A and 4A be connected. PC 15s using transistor type FT501 will probably require the 2A and 4A connection. E_{CE} is the reading of importance the balance of the waveshape should not exceed 30 VPP.

DESCRIPTION OF CHANGE	PAGE NO.
6.1.11 Added: Resistor R19, 10 to 47 ohms, ½ watt ± 20%. Optional.	14, 38
6.1.12 Updated regarding installation	7
Added 1.375 DIM. Note: Correction 3 7/32 was 3 3/16.	8
Added New Page	9, 10
" " "	11, 15
Updated	16, 17
"	19, 20, 21
Corrected to include testing of PC 15A	22
Added New Page	23, 24
Updated	25, 26
"	27, 28
Added Step 15 and Updated	29
Added Step 16 and Updated	30
Updated	34, 35, 36
"	37, 38
Changed: FT 91030B, KGS 715T-1 (Universal type for FT 91030, KGS 715T)	39
Changed: FT 91135, KGS 849T (Universal type for FT 91031, KGS 716T)	39
Changed: FT 91136, KGS 850T (Universal type for FT 91060, KGS 717T)	39
Updated	41, 42
Updated - R4 and C9 identification corrected	44
Added - CR9, CR10, F1 and R19	45

6.2 PC-15 Revision No. 1 - 5 Pin

6.2.1 Electrical connection for the PC-15 having 5 pin. (5 pin connector units do not have paralleling capability)



* For emergency operation only 115 VAC output into a load of 225 VA at an input of 20 VDC.

ELECTRICAL CONNECTION DIAGRAM

6.2.2 Serial Number Effectivity

All PC-15 with serial numbers through 311 have the five pin connectors as shown in 6.2.1. Except units noted in paragraph 6.2.3 seven pin connector revision, which have been converted from five to seven pin.

Also the following units have five pin connectors. Serial Numbers: 423 thru 434, 498, 499, 502 thru 516, 552 thru 568, 498 and 592 thru 599.

6.2.3 Electrical connection for the seven pin connector are shown in the mounting details and schematics on pages 8, 9, 14 and 15 respectively.

PC-15 units with serial number 312 and up are seven pin connectors except those serial numbers shown in paragraph 6.2.2. Also the following units preceding serial number 312 have been converted to seven pin connectors. Serial Numbers: 201, 202, 226, 229, 261, 262 and 292.

6.3 Revision No. 2

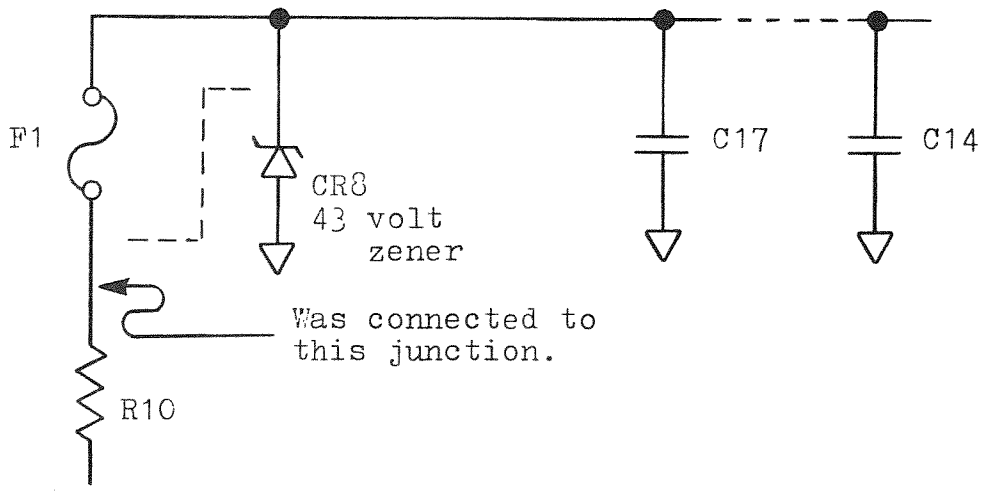
DESCRIPTION OF CHANGE	PAGE NO.
Effective on serial number 1471 and up. Transistors Q11, Q12, Q13, Q21, Q22 and Q23 can be type FT 459 or FT 460.	37

CAUTION: The use of either device type should not be mixed in a given PC-15( ).

6.4 Revision No. 3

Effective immediately and all units manufactured after serial number 1934.

Description of change: Connect zener CR8 as shown.



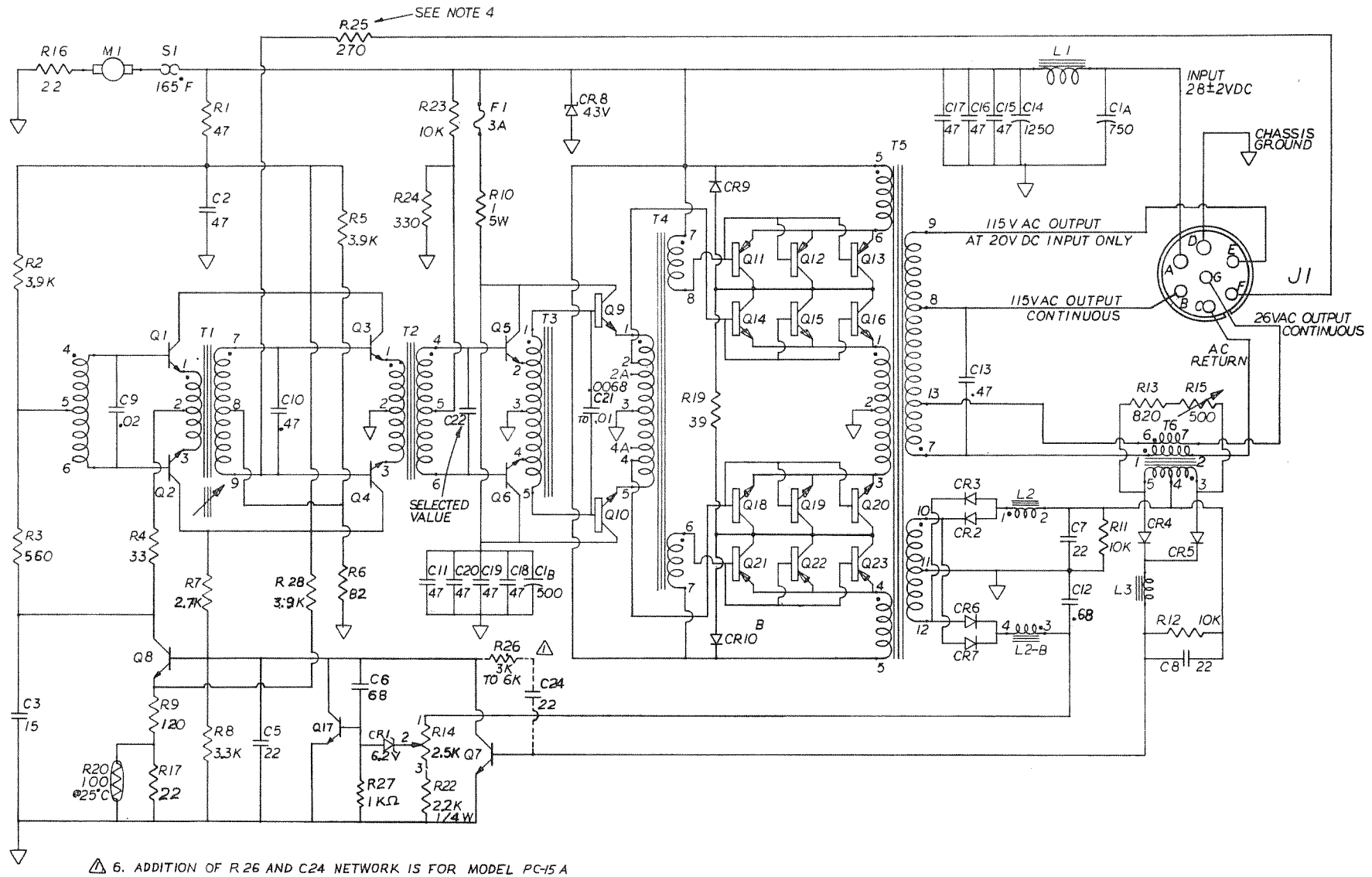
Reason for change: To prevent undesired rupturing of fuse F1 when zener CR8 is forced into conduction by a transient voltage exceeding 43 volts.

6.5 Revision No. 4

6.5.1 The Revision No. 4 applies to static inverter model PC-15( ) Series manufactured starting with serial number 2779. (Refer to Flite-Tronic's supplementary list of lower serial number units corrected to Revision 4). The purpose of this revision is to maintain a minimum output of 115 VAC -7% down to an input of 22 VDC and 100 VAC output down to an input of 20 VDC.

The following Rev. 4 changes are also shown in schematic on page 54 and in Figure 5.4A on page 56.

	DESCRIPTION OF REV. 4 CHANGES	AFFECTED PAGE NO.
6.5.1.1	C4 is deleted was 22 uf 25 VDC	14, 15, 36
6.5.1.2	C6 is 68 uf 6 VDC CL65BB680-UP3 was 33 uf 15 VDC	14, 15, 36
6.5.1.3	C12 is .68 uf 35 VDC A684K035 was 22 uf 25 VDC	14, 15, 36
6.5.1.4	CR1 is 1N753A in base of Q17 was 1N4735 1W in emitter of Q17	14, 15, 36
6.5.1.5	R3 is 560 ohms was 680 ohms	14, 15, 37
6.5.1.6	R6 is 82 ohms was 390 ohms	14, 15, 37
6.5.1.7	R7 is 2.7 K ohms was 3.9 K ohms	14, 15, 37
6.5.1.8	R9 is 120 ohms was 560 ohms	14, 15, 38
6.5.1.9	R17 is 22 ohms was 180 ohms	14, 15, 38
6.5.1.10	R18 is deleted was 10 K ohms	14, 15, 38
6.5.1.11	R27 is 1 K ohm, ½ W added	
6.5.1.12	R28 3.9 K ohm, ½ W added	
6.5.1.13	Gray (8) lead wire from T1 is connected to junction of R5 and R6 was connected to the base of Q8	14, 15
6.5.1.14	Terminal 2 of T2 is grounded was connected to junction of R5 and R6	14, 15
6.5.1.15	Emitter of Q17 is grounded was connected to CR1 cathode	14, 15



⚠ 6. ADDITION OF R 26 AND C24 NETWORK IS FOR MODEL PC-15 A WITH LETTER A AFTER SERIAL NUMBER ONLY.

5. REVISION 4 CHANGE: SERIAL NO. EFFECTIVITY, SN 2779.

4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A WITH R25

3. MATING PLUG FOR J1: MS 3106B 18-9S,

2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF

1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3A

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
B	FE 227	8/71		
A	FE 166	3/71		

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03, XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 2°

ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D
MAT'L				

FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15A SCHEMATIC

DRAWN		10/1/67
CHK'D		10/1/67
APPR'D		10/1/67
SCALE		
MODEL	PC15A	
NEXT ASSY.		
SIZE C	DWG. NO. 91003-1B	

6.5.2.1 Add the following paragraph under <u>Emergency Output Connections</u> of Sec. II on page 7

The AC voltage from the normal output (Pin B) of the PC-15( ) after serial number 2779 shall be greater than 115 VAC -7% at 22 VDC input and greater than 100 VAC delivering up to 90% of rated load for an input battery condition of 20 VDC.

6.5.2.2 The second paragraph and the first sentence in the third paragraph Sec. 3.5 on page 17 is:
The output from terminal 8 (Pin B) shall be greater than 100 VAC working into 90% of rated load, during an input of 20 VDC and at least 115 VAC -7% with 22 VDC input. The output from terminal 9 is 115 VAC +5% -7% working into 90% of rated load, during an input between 19 VDC and 20 VDC on the A+ line.

This output, if needed, can be used only during emergency 20 VDC input condition and the load should be connected to Pin E of J1.

6.5.2.3 The second and third sentence in the second paragraph Sec. 3.6 is:
The variable portion of the resistor is connected to the base of Q17 via CR1. In essence, this output voltage sample is compared with zener CR1 in the base of Q17. "Resistor R18" of the next sentence is "Resistor R27"

6.5.2.4 Check procedure for Pin E output for Table 4.2, Sec. 4.4, on page 24, is as follows under each heading.
Model: PC-15( )
Load condition: Pin Boutput at 20 VDC input
Switch position: S4 on; S1 to #1; S5 thru S10 off; S11 to PC-15; S12 and S13 to 115 VAC
Input Voltage: Set to 20 VDC
Input Current: 12 Amps typical
Output Voltage: 100 VAC minimum
Output Current: 1.72 Amps typical

6.5.2.5 Step 14, Table 4.3, page 29, is changed as follows:

6.5.2.5.1 Under Set Up
is "Switch S1 to #1"
was "Switch S1 to #2"

6.5.2.5.2 Under Reference reading
is "V2 read 100 VAC minimum"
was "V2 read 107 to 120.7 VAC"

6.5.2.6 DC voltage measurement changes for Q3 and Q4 Sec. 4.5, page 31
is "Emitter .1 to .4" was "Emitter 8.2"
is "Base .55" was "Base 8.2"

6.5.2.7 DC voltage measurement change for Q7, page 32
is "Collector 2.5 to 4" was "Collector 8 to 10"

6.5.2.8 DC voltage measurement change for Q17 page 31 and 32
is "Emitter 0" was "Emitter 6 to 7.5"
is "Base .5 to .7" was "Base 6 to 7.5"
is "Collector 2.5 to 4" was "Collector 8.2 to 9.2"

6.5.2.9 DC voltage measurement change for Q8 page 32
is "Emitter 2 to 3.5" was "Emitter 8 to 9"
is "Base 2.5 to 4" was "Base 8.2 to 9.2"

6.5.2.10 Figure 5.4 on page 42 is Figure 5.4A as shown below

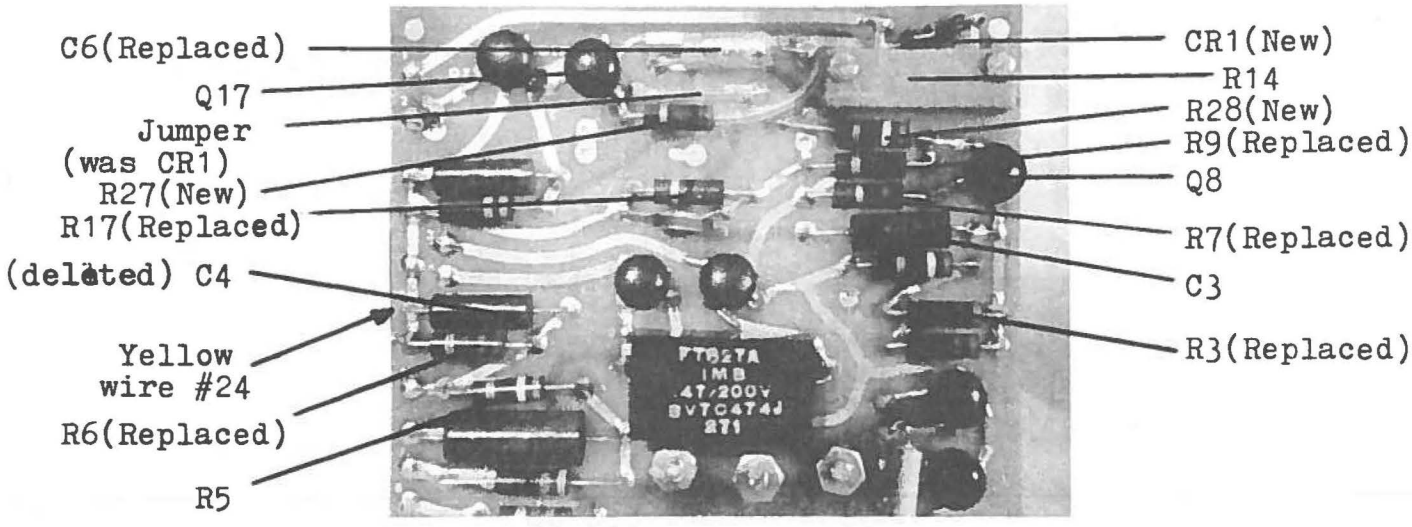


Figure 5.4A component layout changes reflecting Rev. 4

6.6 Revision No. 5

6.6.1 Heading "Service Bulletin" on page 51 is changed to read "Revision". The change is to improve classification.

6.6.2 Heading "PC-15 Service Bulletin No. 1" in Sec. 6.2 is changed to read "PC-15 Revision No. 1-5 Pin". The change is to improve classification.

6.6.3 R22 is 2.2 K ohms was 2.7 K ohms on pages 14, 15 and 38. Typographic error.

6.6.4 R13 is 820 ohms was 560 ohms on page 38. Typographic error.

6.6.5 R1 on page 21 and 22 is 1.16K ohms for 4% load was 1.2K ohms. Serial number effectivity: None

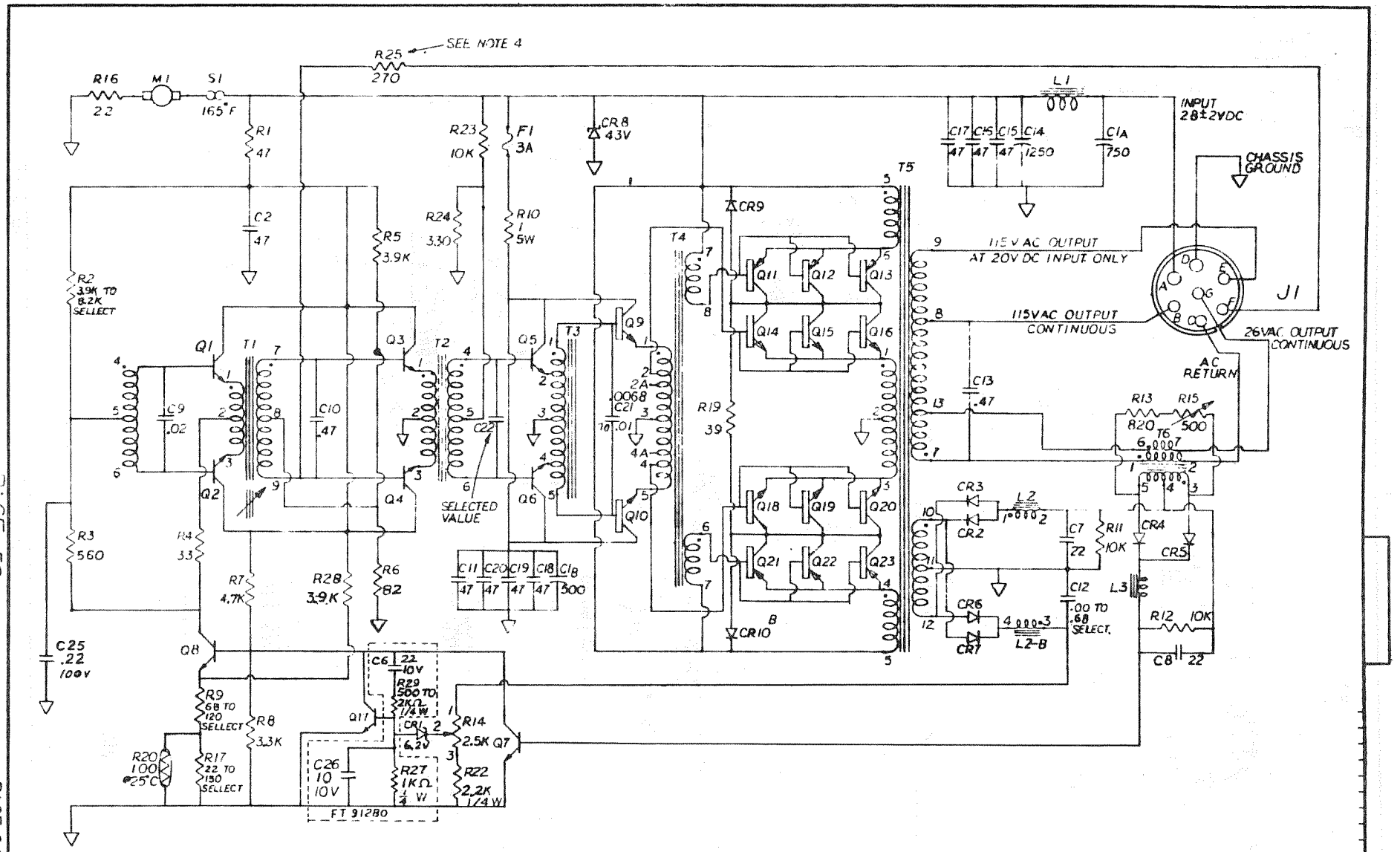
6.6 Revision No. 6

6.7.1 The Revision No. 6 applies to all static inverter model PC-15( ) Series manufactured starting with Serial number 3174 except 3176 and 3177. (Refer to Flite-Tronic's supplementary list of lower serial number units corrected to Revision No. 6)
The purpose of this revision is to improve the frequency response of the unit to decrease the effect of low frequency ripple and transient on the 28VDC bus from appearing on 115VAC output.

The changes for Revision No. 6 are shown in the schematic on page 59 and 60. Figure 5.4B on page 62 is component layout.

6.7.2 Description of Rev. 6 Changes		Affected Page No.
6.7.2.1	C_3 is deleted, was 15uf 50VDC	14, 15, 36, 42, 56 A8, A9, A10, A12
6.7.2.2	C_5 is deleted, was 22uf 25VDC	14, 15, 36, 42, 54, 56, A8, A9, A10, A12
*6.7.2.3	C_6 is 22uf 10Vdc, CS13BC226K	14, 15, 36, 42, 54, 56, A8 A9 A10, A12
6.7.2.4	C12 is selected between 0 and .68uf, 35VDC, was .68uf 35VDC	14, 15, 36, 42, 54, 56, A8, A9, A10, A12
6.7.2.5	C25, .22uf 100VDC, BA2B224K added	
6.7.2.6	C26 10uf 10VDC, Cs13BC106K added	
6.7.2.7	R_2 is 5.6K ohms selected was 3.9K ohms	14, 15, 37, 42, 54, 56, A8, A9, A10, A12
6.7.2.8	R_7 is 4.7K ohms selected was 2.7K ohms	14, 15, 37, 42, 54, 56, A8, A9, A10, A12
6.7.2.9	R_9 is 82 ohms selected, was 120 ohms	14, 15, 38, 42, 54, 56, A8, A9, A10, A12
6.7.2.10	R_{17} 8s 75 ohms selected, was 22 ohms	14, 15, 38, 42, 54, 56, A8, A9, A10, A12
*6.7.2.11	R_{29}, ¼W 500 ohms to 2K ohms selected, added in series with C_6	
*6.7.2.12	R_{27} is ¼W, was ½W	53, 54, 56, A8, A9, A10, A12

*These Components are encapsulated in a module identified as FT 91280 in Model PC-15( ) with serial numbers between 3174 and 3261 inclusive except 3176 and 3177.



5. REV. 6 CHANGE: S/N EFFECTIVITY. 3174, 3175, 3178 AND UP.

4. USE CAPACITOR C23 (TYPICALLY .0047 μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A WITH R25

3. MATING PLUG FOR J1: MS 3106B 18-9S.

2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF

1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3B

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
E	FE 511	8/72		
D	FE 392	6/72		
C	FE 356	1/72		
B	FE 177	7/71		
A	FE 156	7/71		

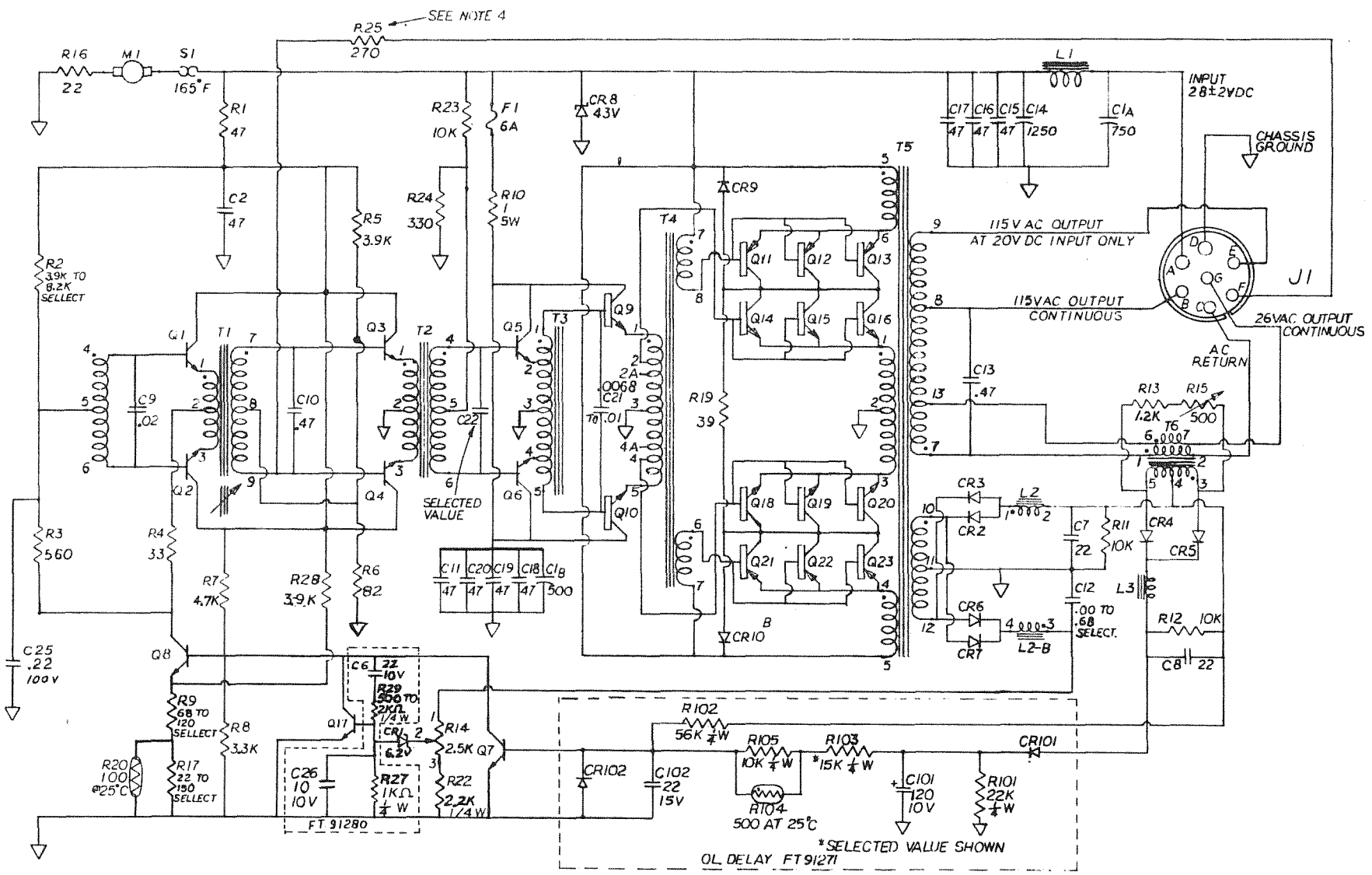
TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL .XX ± .03, .XXX ± .005; FRACTIONAL ± 1/32; ANGULAR ± 2°

MAT'L

FLITE-TRONICS, INC.
2312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15A
SCHEMATIC

DRAWN		7/1/67
CHK'D		7/1/67
APPR'D		7/1/67
SCALE	—	
MODEL	PC15A	
NEXT ASSY.	—	
SIZE C	DWG. NO. 91003-1E	



6 REV. 6 CHANGE: S/N EFFECTIVITY, 3174, 3175, 3178 AND UP.
5 PC-15B TO TRIP 1A C.B. WITH NORMAL CHARACTERISTIC.
4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15B WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .0012 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-1B

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
C	F1 256	1/72		
B	F1 228	8/71		
A	F1 160	3/71		

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03, XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 1°

ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D
MAT'L				

FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC15B
SCHEMATIC

DRAWN		10/67
CHK'D		11/67
APPR'D		7/68
SCALE	—	
MODEL	PC15B	
NEXT ASSY.	—	
SIZE C	DWG. NO. 91003-2C	

6.7.3 Description of Changes and Additions to the Manual for Revision No. 6 Modifications to the PC-15( ).

6.7.3.1 Add the following sentence at the end of 4th paragraph under Sec. 3.3, Page 16.
Capacitor C25 suppresses any tendency for low frequency motor boating.

6.7.3.2 Add the following sentence at the end of the second paragraph under Sec. 3.6. (Refer also to Rev. 4 changes under Sec. 6.5.2.3, Page 55)
RC network formed by C6, R29 and C26 at the base of Q17 compensate the closed loop circuit gain over operating temperature range and prevents the automatic level control circuitry from motor boating.

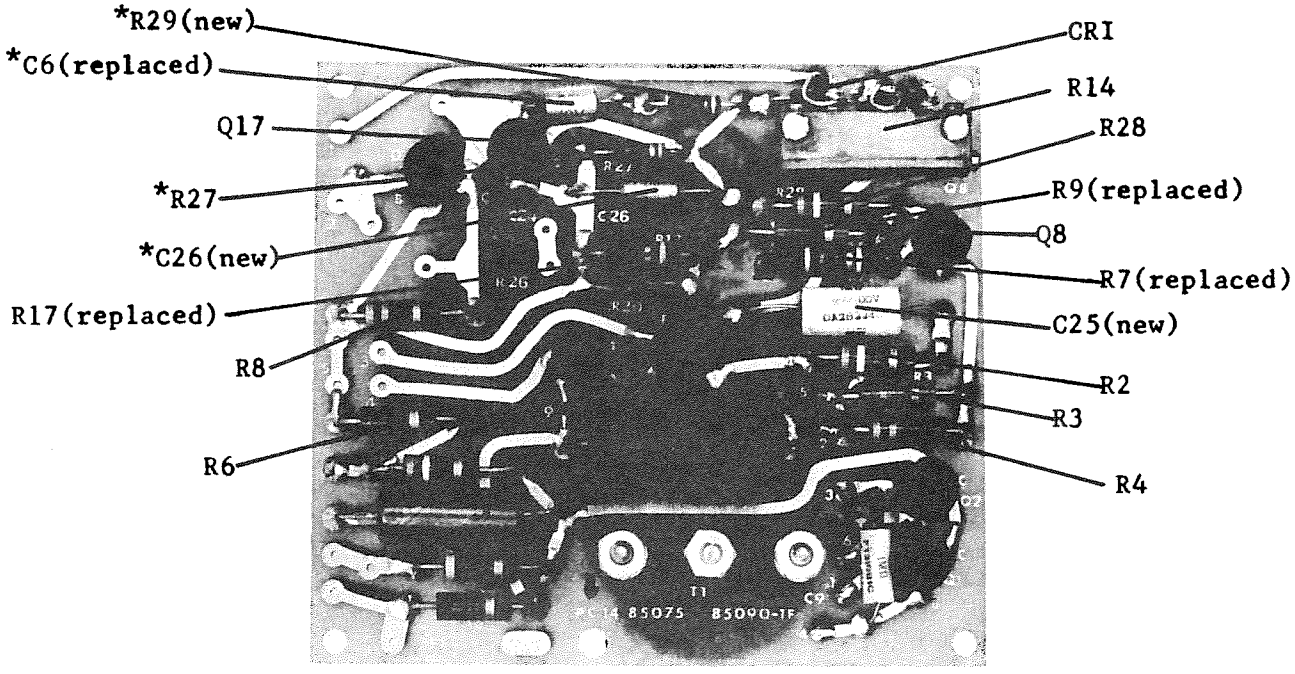
6.7.3.3 Delete the entire seventh paragraph under Sec. 3.6, Page 17.

6.7.3.4 AC voltage measurement change for Q7, Sec. 4.5, Page 32.
is "collector .1 to .2" was "Emitter 0"

6.7.3.5 AC voltage measurement change for Q8, Page 32
is "Emitter .1 to .2" was "Emitter 0"
is "Base .1 to .2" was "Base 0"
is "Collector .2 to .4" was "Collector 0"

6.7.3.6 AC voltage measurement change for Q17, Page 32
is "Collector .1 to .2" was "Collector 0"

6.7.3.7 Figure 5.4 on Page 56 is Figure 5.4B as Shown Below



* Refer to * mark note on page 58 for detail

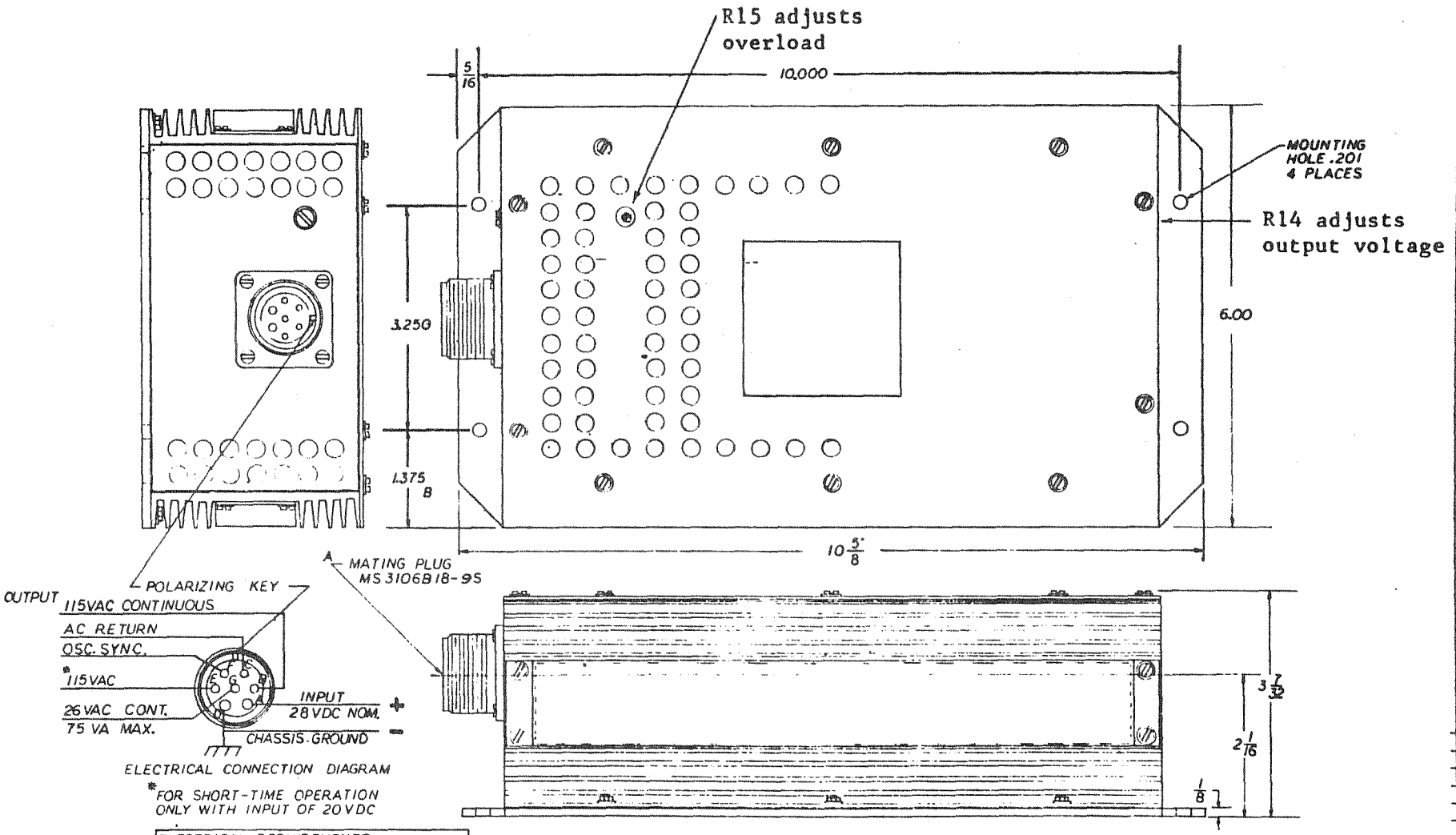
FIGURE 5.4B Component Layout changes reflecting Revision No. 6.

6.7 Revision No. 7

6.7.1 Revision No. 7 applies to all 250 VA static inverter model series manufactured starting with Serial Number 3700

The purpose of this revision is to incorporate model identification change.

MODEL ID IS	MODEL ID WAS
PC-15B( )	PC-15B
PC-15B-D	PC-15D
PC-15B-E	PC-15E
PC-15B-F	PC-15F
PC-15B-G	PC-15G



ELECTRICAL CONNECTION DIAGRAM

*FOR SHORT-TIME OPERATION ONLY WITH INPUT OF 20VDC

ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115, 26
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	8.2

FIGURE 2.2-1A
INSTALLATION AND MOUNTING DIMENSIONS

A	F7194	4/5/66	JA	JL	ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D
CHG. LTR	E.C.O. NO.	DATE	BY	CHK'D					

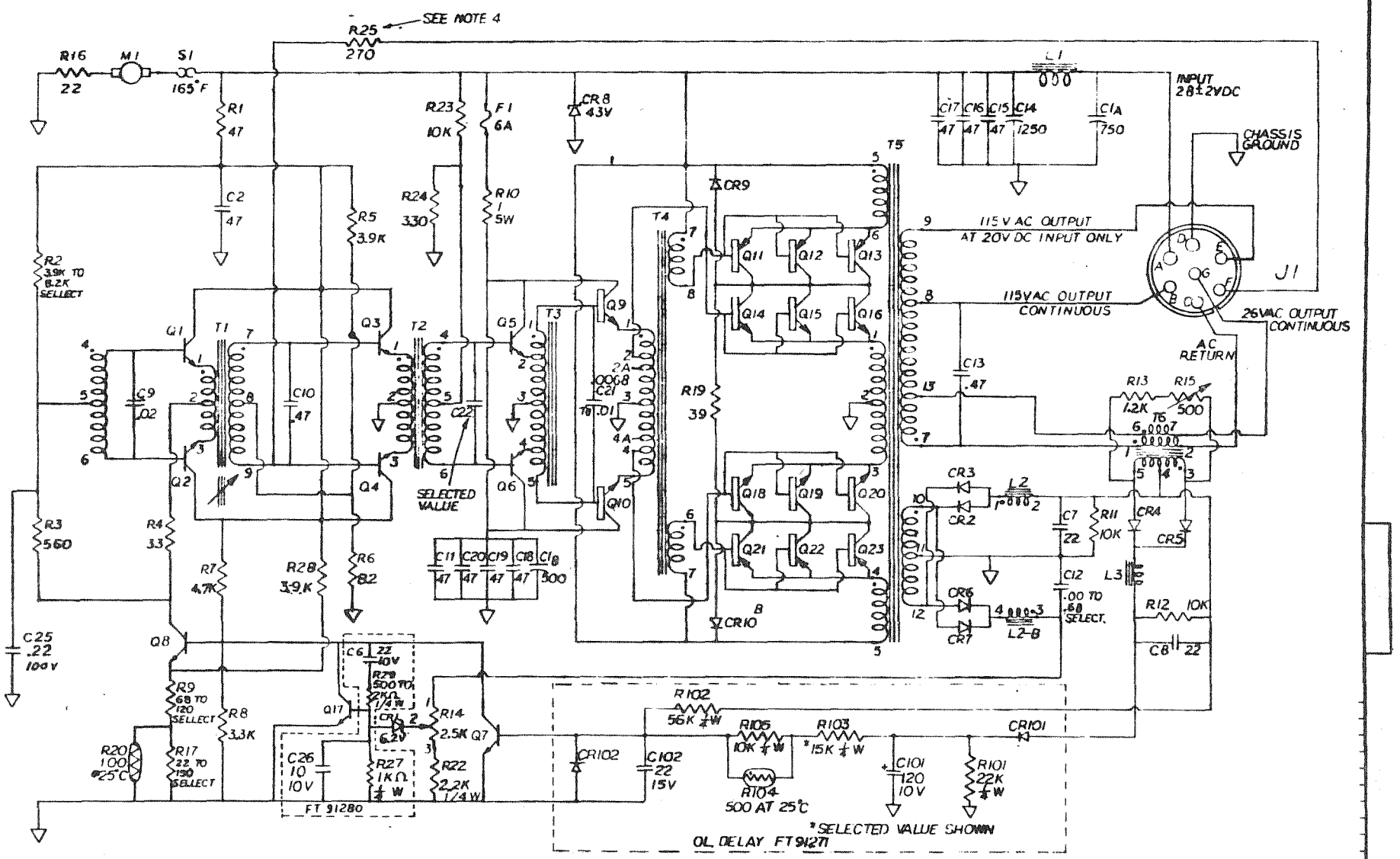
MAT'L

FLITE-TRONICS, INC.
3312 BURTON AVE., BURBANK, CALIF.

TITLE
PC 15B() STATIC INVERTER
MOUNTING DETAILS

DRAWN	4/5/66
CHK'D	4/8/66
APPR'D	
SCALE	FULL
MODEL	PC15B()
NEXT ASSY.	
SIZE C	DWG. NO. 91008-2A

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL .XX ± .09
.XXX ± .015
FRACTIONAL ± 1/32
ANGULAR ± 1°



6. REV. 7 CHANGE: S/N EFFECTIVITY, 3700
5. REV. 6 CHANGE: S/N EFFECTIVITY, 3174, 3175, 3178 AND UP.
4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15B( ) WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-1C

D	FE 291	6/72			
C	FE 278	1/72			
B	FE 238	8/71			
A	FE 146	8/71			
ORIG. LTR.	E.C.O. NO.	DATE	BY	CHKD	

TOLERANCES UNLESS OTHERWISE NOTED

FLITE-TRONICS, INC.
2812 SURTON AVE., BURBANK, CALIF.

TITLE
PC15B( )
SCHEMATIC

DRAWN		
CHK'D		
APPR'D		
SCALE	—	
MODEL	PC15B( )	
NEXT ASSY.	—	
SIZE C	DWG. NO. 91003-2D	

ADDENDA

SECTION VII - DESCRIPTION OF MODEL SERIES

SECTION	ADDENDUM	MODEL SERIES	DESCRIPTION
7.1	No. 1	PC-15B or with letter B after serial number on model PC-15A.	250 VA unit with overload (OL) delay to trip 1 amp circuit breakers having characteristic to trip within 3 seconds at 3.0 amperes.
7.2	No. 2	PC-15A with letter M1 after serial number.	PC-15( ) modified to increase overload capacity per Service Bulletin No. 1/PC-15
7.3	No. 3	PC-15A with letter A after serial number	PC-15( ) modified to rupture 1 amp medium slow blow type fuse per Service Bulletin No. 2/PC-15
7.4	No. 4	PC-15D	PC-15B modified to deliver 115 VAC up to 100 VA 26 VAC up to 150 VA
7.5	No. 5	PC-15E	PC-15B modified for remote on and off
7.6	No. 6	PC-15F	PC-15B with DC return isolated from chassis
7.7	No. 7	PC-15G	PC-15B with new connector

7. DESCRIPTION OF ADDENDUMS

7.1 Model PC-15B

7.1.1 Refer to page A7 for PC-15B mounting detail

7.1.2 Refer to page A8 for PC-15B schematic

7.1.3 Refer to figure 7.1.1 on page A4 for FT91271 overload delay module schematic

7.1.4 Refer to figure 7.1.2 on page A4 for FT91271 overload delay module layouts

7.1.5 R13 is 1.2K ohms, was 820 ohms

7.1.6 F1 is 6A, GKN 6

7.1.7 C101 is 120 uf, 10 VDC, CS13BC127K

7.1.8 C102 is 22 uf, 15 VDC, CS13BD226K

7.1.9 CR1 is 1 amp, 200 VDC, IN5393 or equiv.

7.1.10 CR2 is same as CR1

7.1.11 R101 is 22K ohms, $\frac{1}{4}$w, 10%

7.1.12 R102 is 33K to 82K ohms selected, $\frac{1}{4}$w, 10%

7.1.13 R103 is 10K to 27K ohms selected, $\frac{1}{4}$w, 10%

7.1.14 R104 is 500 ohms @ 25 °C, 25KE1 ,GUL, or equiv.

7.1.15 R105 is 10K ohms, $\frac{1}{2}$w, 10%

7.1.16 The second sentence of the 4th paragraph, sec. 3.7, on page 18 is "when the output current causes a voltage across R12 to exceed the compared voltage across R11, transistor Q7 will start conducting after a time delay introduced by the overload delay module FT91271.

7.1.17 The DC voltage of base of Q7, Table 4.4, page 32 is -.2 to -.5 , was -1.5 to -6*

7.1.18 The 175% overload and output short-circuit tests of Table 4.2, page 23 and 24 are changed as follows

Table 4.2 Test Conditions and Typical Readings

MODEL	CONDITION	SWITCH	POSITION	TYPICAL READINGS			
				DC INPUT		AC OUTPUT	
				VOLTAGE	CURRENT	VOLTAGE	CURRENT
PC-15B Only	175% Overload	S1 S8 S2-S7 S9&S10 S11 S12&S13 S14&S15	#1 on off off PC-15 115 VAC off	Set to 28 VDC	Meter Deflection Between 0 and 25 amp motorboating	Meter Deflection Between 0 and full scale motorboating	Meter Deflection Between 0 and full scale motorboating
PC-15B See Note 1	Output short CKT 115 VAC Output only Loaded	S1 S2-S9 S11 S12&S13 S14&S15 S10(For Short)	#1 off PC-15 115 VAC on on	Set to 28 VDC	See Note 3 Page A3		
	Full Load 175 VA on 115 VAC and 75 VA on 26 VAC	S1 S2-S10 S11 S12&S13 S14&S15	#1 off PC-15A 115 VAC off	Set to 28 VDC	14 Amps Typical	Between 107 VAC and 120 VAC	1.5 Amps Typical
		S12&S13	26 VAC			Between 24.2 VAC and 27.3 VAC	2.9 Amps Typical
	26 VAC Ouput Short CKT	S1 S2-S9 S11 S12&S13 S14&S15 S10(For Short)	#1 off PC-15A 26 VAC on on	Set to 28 VDC	See Note 3 Page A3		

Notes: 1. Modify TS-PC-15-1 as follows for the output short circuit test only.

a. Refer to figure 7.1.3, page A5, for TS-PC-15-1 modified per this note 1 for output short circuit test.

b. Add S14 directly across terminals of current meter I_1

c. Add S15 directly across terminals of current meter I_2

d. Replace a wire between low side of S10 and AC return with a resistor R11 2 ohms, 200 watts

e. Above modifications prevent any damage to test-set meters, but effectively test the output short circuit performance of PC-15B

2. For output short circuit test close S10 so that 115 VAC or 26 VAC output is shorted to ground through R11

3. The initial output short circuit current burst is relatively long in duration and high in amplitude. The second and subsequent burst will normally settle down to exhibit anything from quenching burst to motorboating. Refer to reference short circuit wave shape shown in Figure 7.1.4 page A6.

7.1.19 Changes in step 9 of Table 4.3, page 27, are as follows

7.1.19.1 Under procedure; add c) Check that the PC-15B is in a motorboating mode at 175% overload before proceeding to step 10.

7.1.19.2 Under Reference Reading
I_1 will be pulsating from 0 to 25 amps

7.1.19.3 Under Possible Cause of Abnormal Readings; add all the components in the FT91271 overload delay module.

7.1.20 Changes in step 10 of Table 4.3, on page 27, are as follows

7.1.20.1 Under Set-Up
add S14 and S15 position "on"

7.1.20.2 Under Procedure
"b" is deleted

7.1.20.3 Under Reference Reading
I_1 and I_2 both indicate motorboating

7.1.20.4 Under Possible Cause of Abnormal Reading; add all components in FT91271 overload delay module

7.1.21 Changes in step 14 of Table 4.3, on page 29, for PC-15B are the same as changes per paragraph 6.5.2.5 on page 55

7.1.22 Changes in step 16 of Table 4.3 on page 30 are as follows

7.1.22.1 Under Set-Up
Add S14 and S15 position "on"

7.1.22.2 Under Procedure
"b" is deleted

7.1.22.3 Under Reference Reading
I_1 and I_2 both indicate motorboating

7.1.22.4 Under Possible Cause of Abnormal Reading add, all components in FT91271 overload delay module

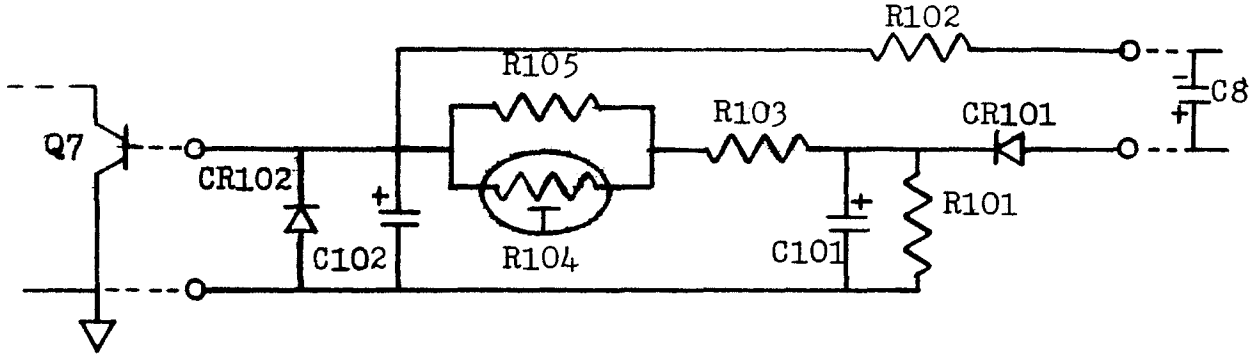


Figure 7.1.1 Overload Delay Module
FT91271 Schematic

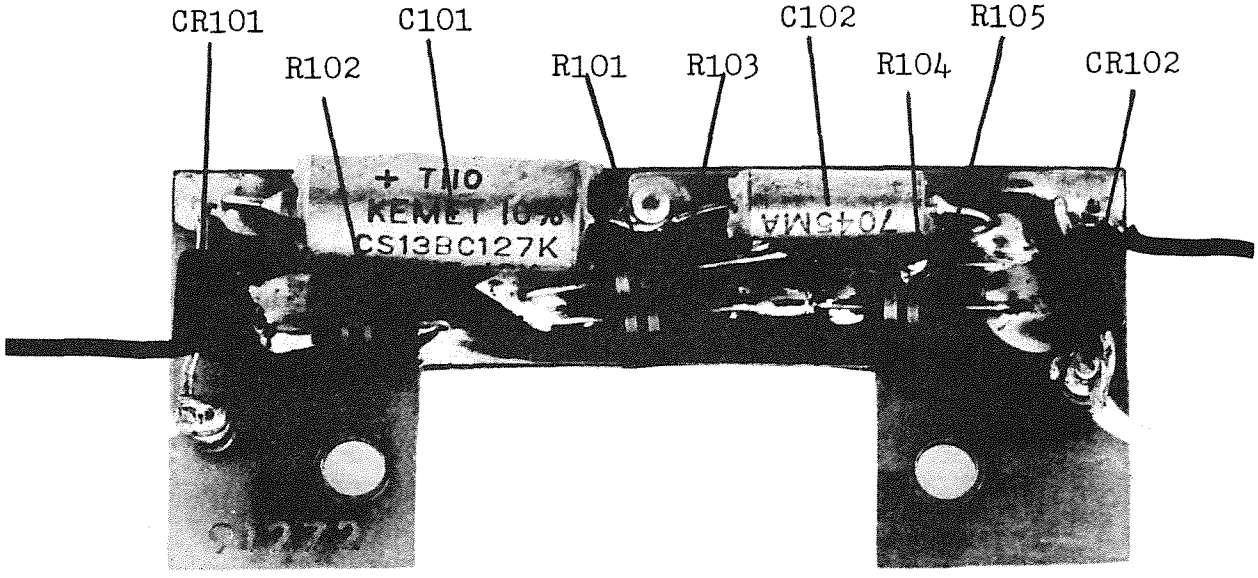
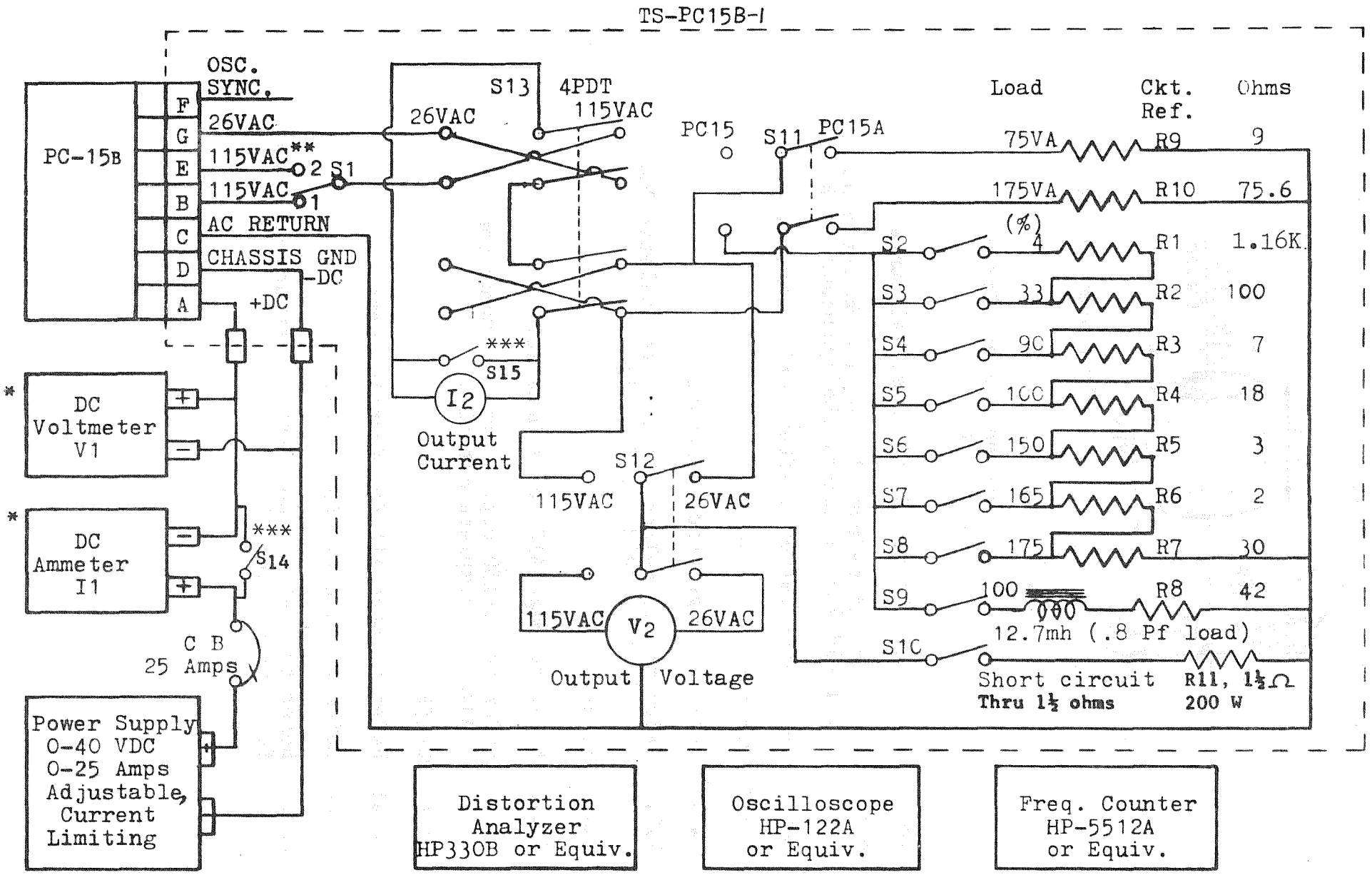


Figure 7.1.2 Overload Delay Module
FT91271 Layouts



*These meters are required only if the power supply does not contain them.
**Emergency output at 20 VDC input only.
***S14 and S15 are closed only during output short circuit test.

FIGURE 7.1.3 BENCH TEST SET AND HOOK-UP

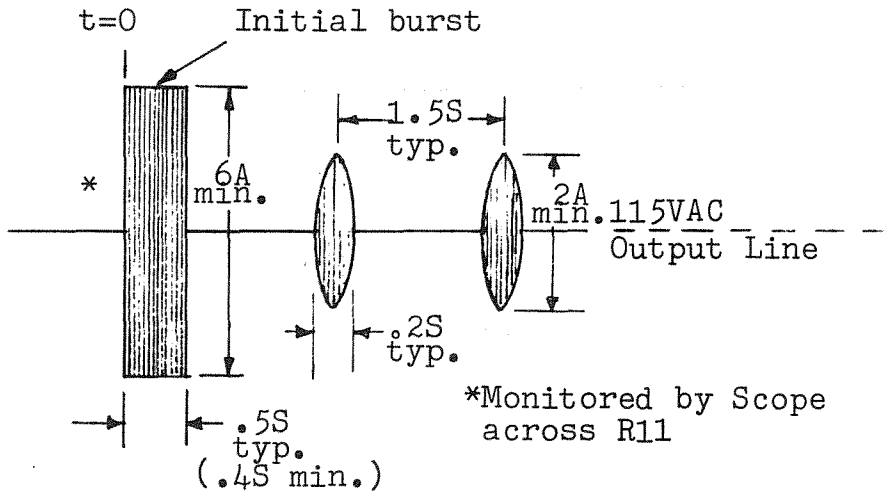


Figure 7.1.4 Reference Short Circuit Waveshape*

7.2 Model PC-15A with letter M1 after serial number.

7.2.1 Refer to Flite-Tronic's Service Bulletin No. 1/PC-15 for field modification. (Readjustment of R15)

7.3 Model PC-15A with letter A after serial number.

7.3.1 R26 and C24 added.

7.3.2 Refer to page A9 for schematic.

7.3.3 Refer to Flite-Tronic's Service Bulletin No. 2/PC-15 for field modification.

7.4 Model PC-15D

7.4.1 Refer to page A10 for schematic.

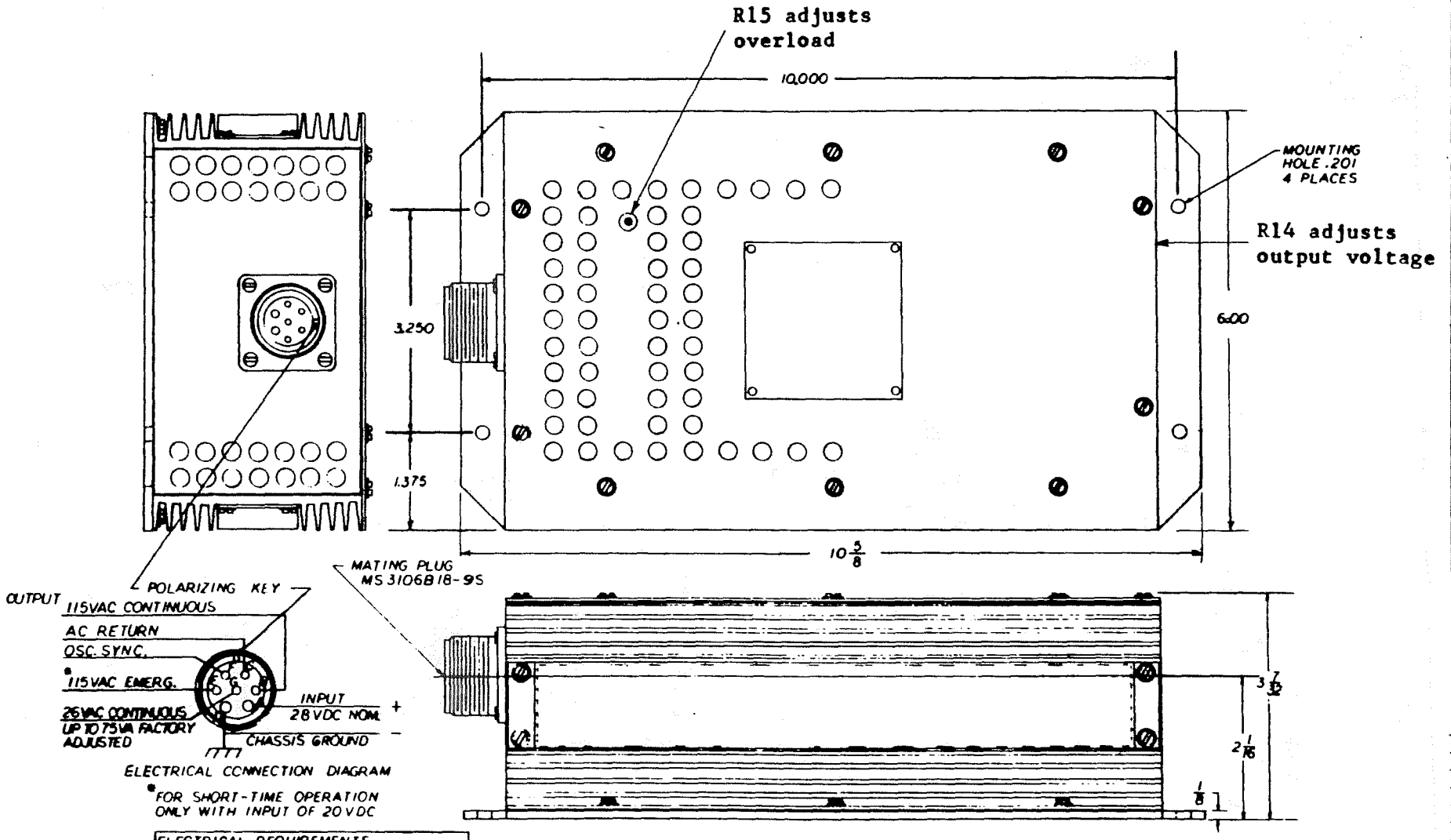
7.4.2 Refer to PC-15D supplemental instruction manual for complete details.

7.5 Model PC-15E

7.5.1 Refer to page A11 for Mounting Detail.

7.5.2 Refer to page A12 for Schematic.

7.5.3 Refer to PC-15E supplemental instruction manual for complete details.

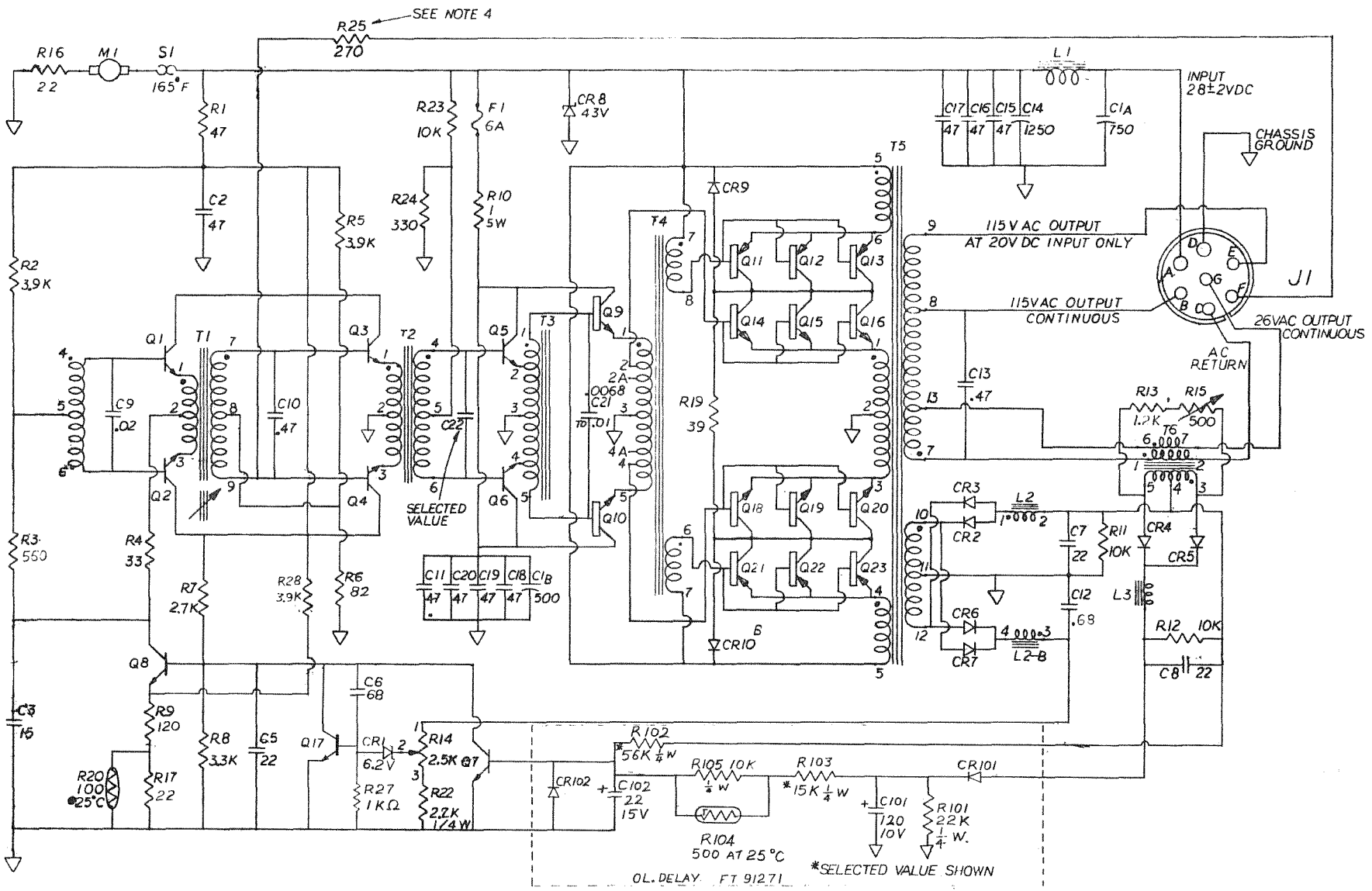


ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115&26
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	8.2

FIGURE 22-1
INSTALLATION AND MOUNTING DIMENSIONS

NOTE: 1. PC-15B DESIGNED TO TRIP 1.0 AMPERE THERMAL TYPE CIRCUIT BREAKER WITH NORMAL CHARACTERISTIC.

FLITE-TRONICS, INC.
PC15B STATIC INVERTER MOUNTING DETAILS
SCALE FULL
MODEL PC15B
C 91008-2A



5. PC15B TO TRIP 1A. THERMAL C.B. WITH NORMAL CHARACTERISTIC.
4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-1A

CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D
B	FT228	8/21		
A	FT133	3/7		

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03, XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 15°

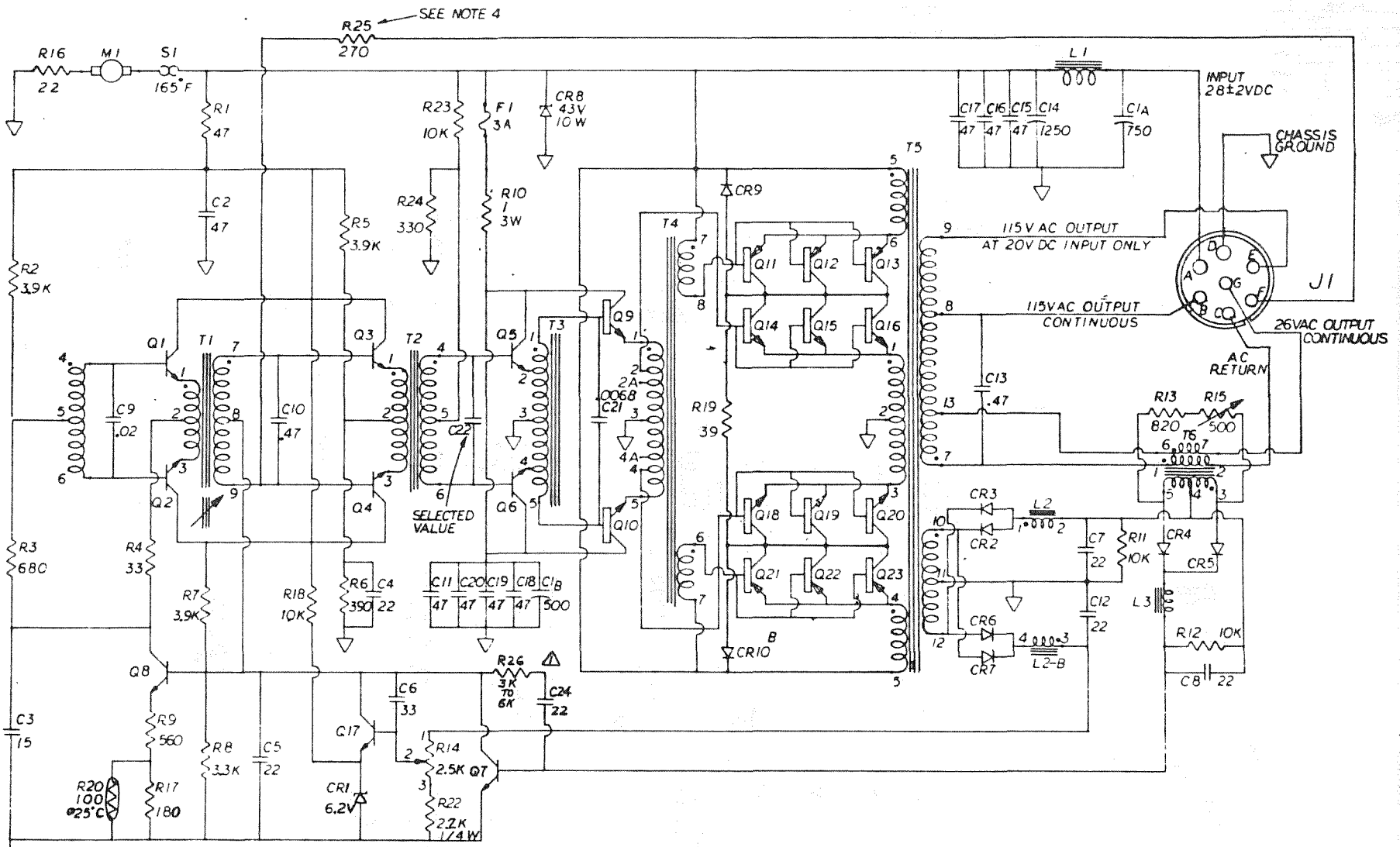
ITEM | PART NO. | CIRCUIT REF. NO. | DESCRIPTION | NO. REQ'D

MAT'L

FLITE-TRONICS, INC.
2812 BURTON AVE., BURBANK, CALIF.

TITLE
PC15B
SCHEMATIC

DRAWN		12/1/67
CHK'D		12/1/67
APPR'D		12/4/67
SCALE		
MODEL	PC15B	
NEXT ASSY.		
SIZE C	DWG. NO. 91003-2B	



⚠ 5. R26 AND C24 ADDED TO RUPTURE 1.0 AMPERE MEDIUM SLOW BLOW TYPE FUSE WITH NORMAL CHARACTERISTIC.

4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A S/N XXXA WITH R25

3. MATING PLUG FOR J1: MS 3106B 18-9S.

2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF

1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

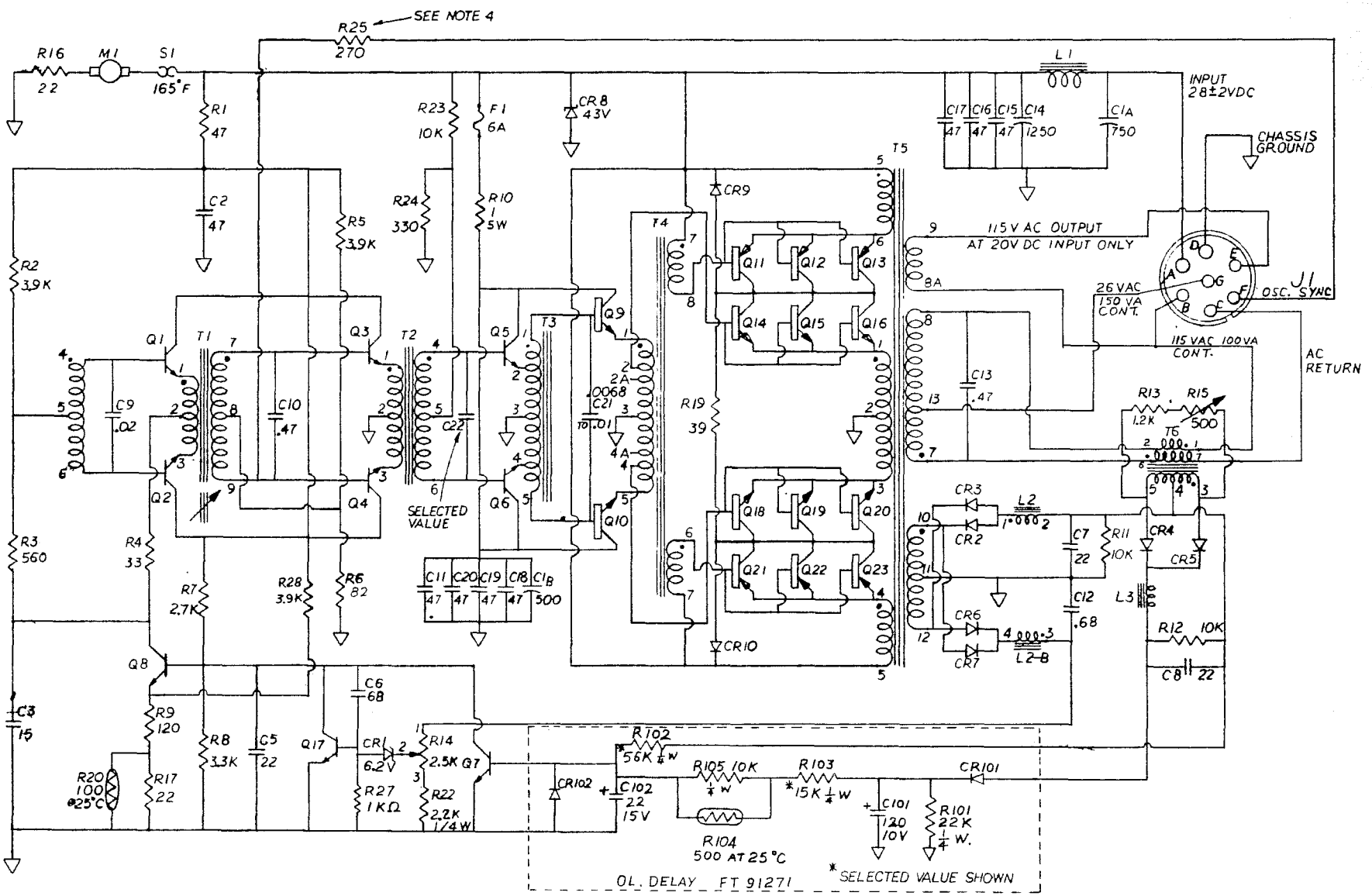
FIGURE 3.3-2

						ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION		NO. REQ.
						MATL.				DRAWN	17/1/80
										CHK'D	19/1/80
										APPR'D	17/1/80
										SCALE	
										MODEL PC15A S/N XXXA	
										NEXT ASSY.	
ORIG. LTR.	S.O.R. NO.	DATE	BY	CHK'D						SIZE C	91003-3

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL .XX ± .03
.XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 2°

FLITE-TRONICS, INC.
8312 BURTON AVE., BURBANK, CALIF.

PC-15A WITH LETTER A AFTER S/N SCHEMATIC



4. USE CAPACITOR C23 (TYPICALLY .0047μF, 50DV.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15A WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .001 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-3

ITEM	PART NO.	CIRCUIT DEST. NO.	DESCRIPTION
	MATL		

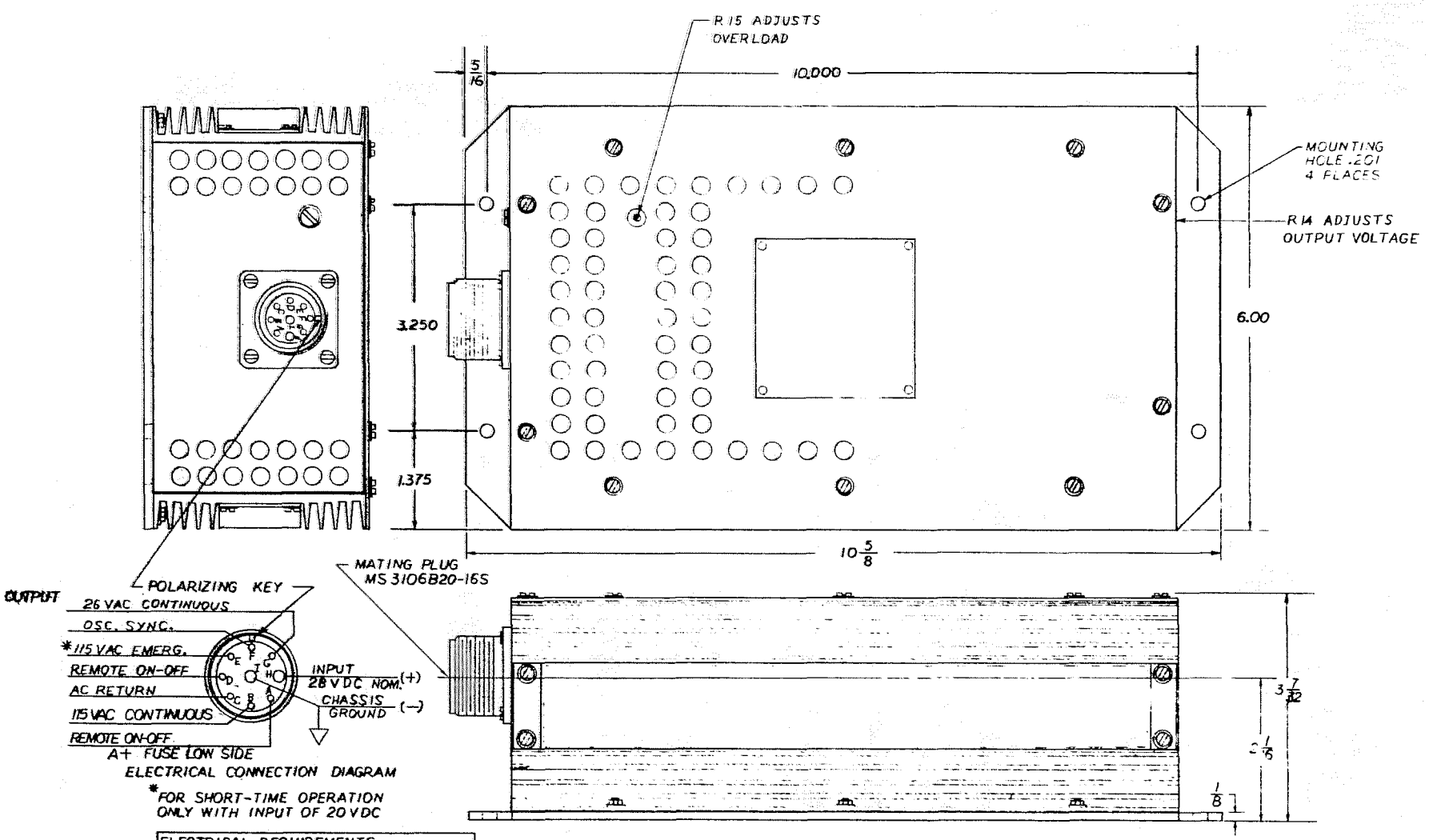
FLITE-TRONICS, INC.
3812 BURTON AVE., BURBANK, CALIF.

TITLE: PC15D SCHEMATIC

DRAWN 7/21
CHK'D 3/21
APPR'D 3/21
SCALE
MODEL PC15D
NEXT ASSY.
SIZE C 91003-4A

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL .XX ± .06
.XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 1°

A CHG. LTR. 11-6-6 E.O.B. NO. DATE BY CHK'D



ELECTRICAL CONNECTION DIAGRAM

*FOR SHORT-TIME OPERATION ONLY WITH INPUT OF 20 VDC

ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115 & 26
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	8.2

FIGURE 2.2-3
INSTALLATION AND MOUNTING DIMENSIONS

NOTE: 1. JUMPER PIN A & D ON MS3106B-20-16S FOR NORMAL OPERATION
2. CONNECT SPST SWITCH BETWEEN PIN A & D FOR REMOTE ON-OFF

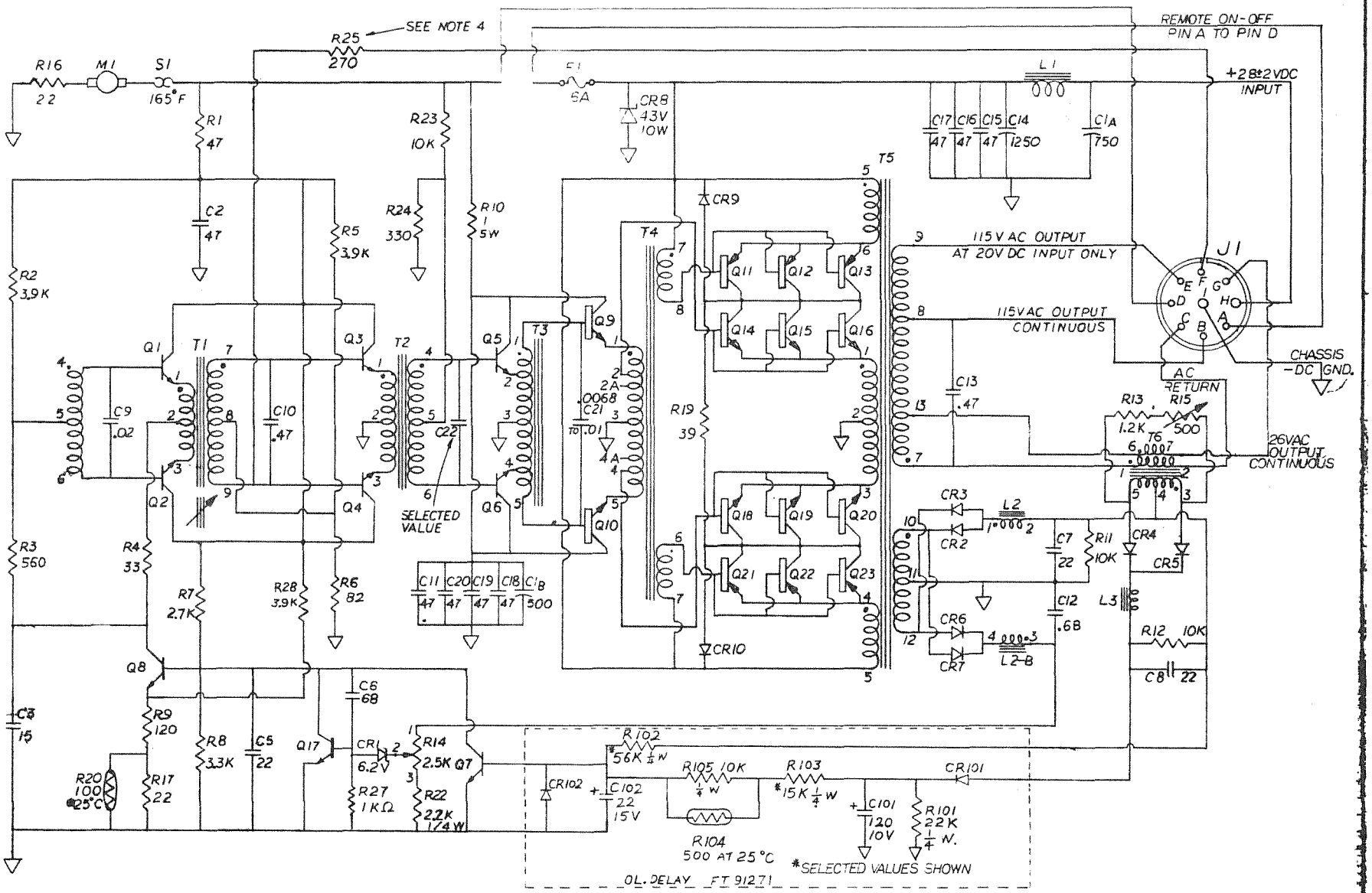
ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D

MATL

FLITE-TRONICS, INC.
5812 BURTON AVE., BURBANK, CALIF.

TITLE
PC15E STATIC INVERTER MOUNTING DETAILS

DRAWN 8/10/71
CHK'D 8/10/71
APPR'D 8/10/71
SCALE FULL
MODEL PC15E
NEXT ASSY.
SIZE C
DWG. NO. 91008-5



6. CONNECT SPST SWITCH BETWEEN PIN A&D FOR REMOTE ON-OFF
5. JUMPER PIN A & D ON MS3106B-20-16S FOR NORMAL OPERATION
4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15E WITH R25
3. MATING PLUG FOR J1: MS 3106B-20-16S
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-4

FLITE-TRONICS, INC.
8878 BURTON AVE., BURBANK, CALIF.

TITLE
PC15E SCHEMATIC

DRAWN 8/71
CHK'D 8/71
APPV'D 8/71
MODEL PC15E
C 91005-5

7.6 PC-15F

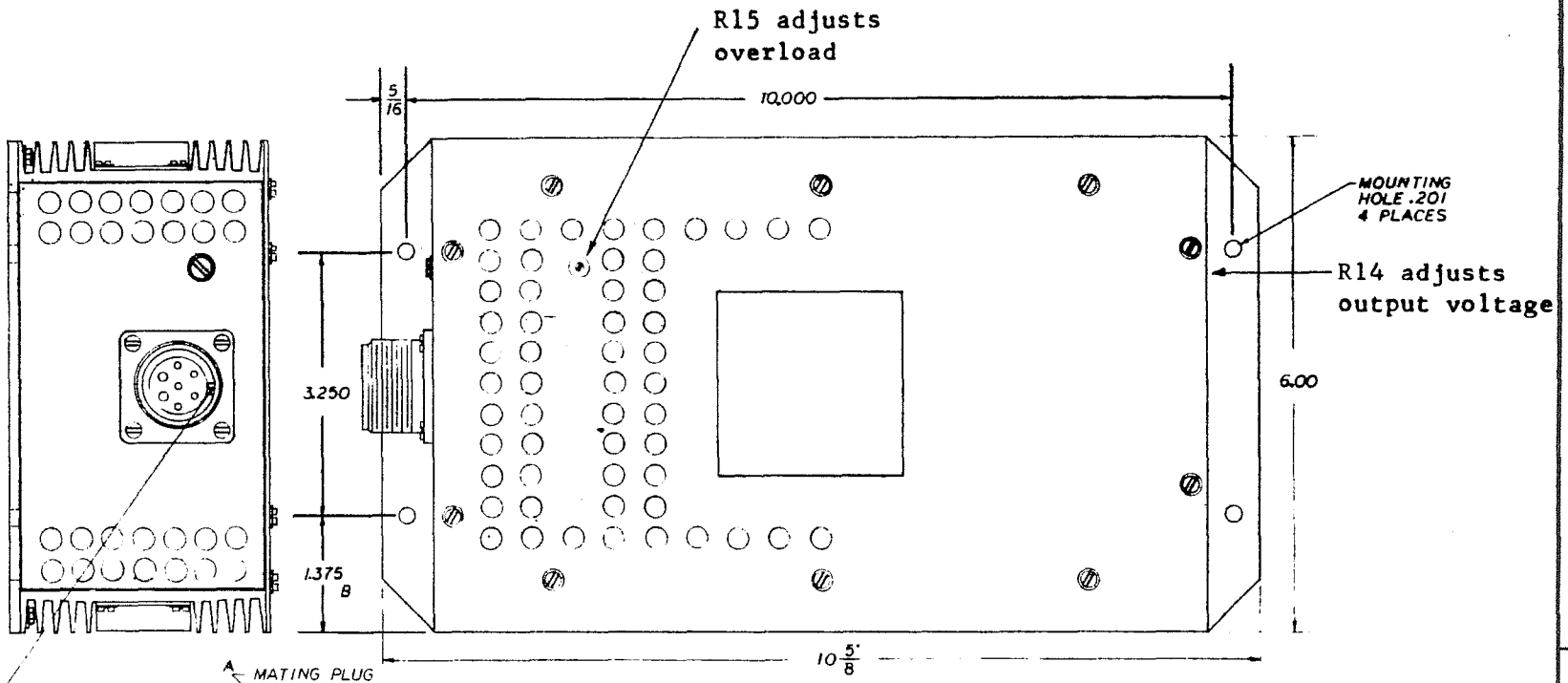
7.6.1 Refer to Page A14 for mounting detail

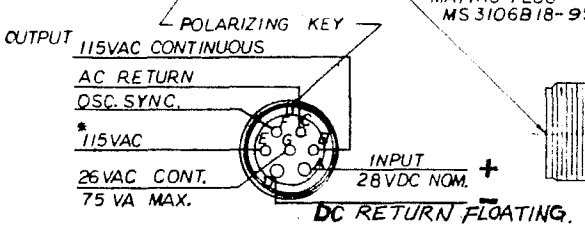
7.6.2 Refer to Page A15 for schematic

7.7 PC-15G

7.7.1 Refer to Page A16 for mounting detail

7.7.2 Refer to Page A17 for schematic





ELECTRICAL CONNECTION DIAGRAM

*FOR SHORT-TIME OPERATION ONLY WITH INPUT OF 20VDC

ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115, 26
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	8.2

FIGURE 2.2-2
INSTALLATION AND MOUNTING DIMENSIONS

ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D
	NAT'L			

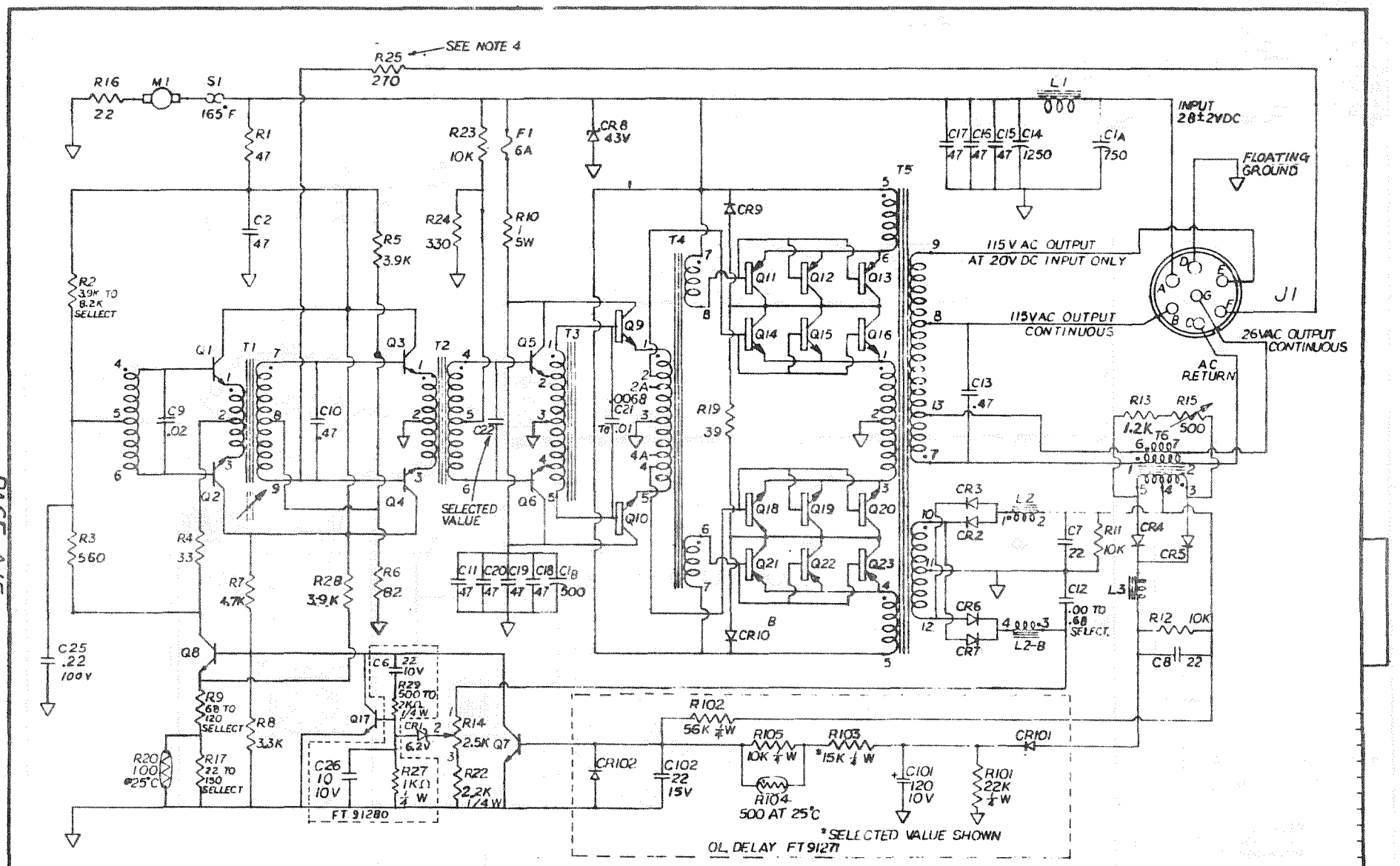
FLITE-TRONICS, INC.
2312 BURTON AVE., BURBANK, CALIF.

TITLE PC-15F STATIC INVERTER MOUNTING DETAILS

DRAWN Lyn 5/18/70
CHK'D 5/19/70
APPR'D 5/25/70
SCALE FULL
MODEL PC15F
NEXT ASSY.
SIZE C DWG. NO. 91008-3

CHG. LTR. | E.C.S. NO. | DATE | BY | CHK'D

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .06 XXX ± .010
FRACTIONAL ± 1/64
ANGULAR ± 5°



4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15F. WITH R25
3. MATING PLUG FOR J1: MS 3106B 18-9S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-5

C	FT 1266	1/12					
B	FT 1266	1/11					
A	FT 164	7/1					
CHG. LTR.	E.C.O. NO.	DATE	BY	CHK'D			

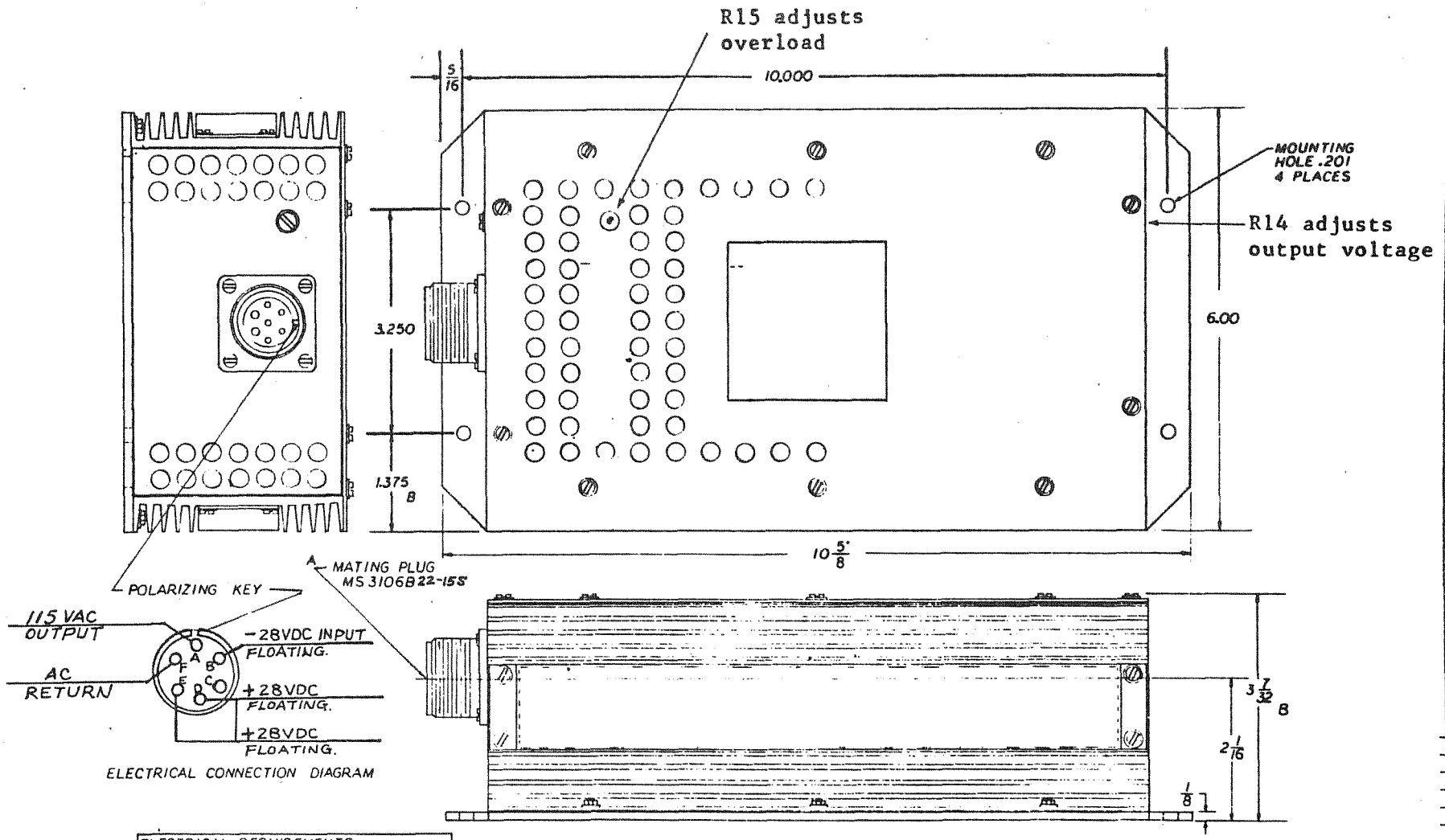
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL XX ± .03 XXX ± .010
FRACTIONAL ± 1/16
ANGULAR ± 2°

ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ.
	MATL			

FLITE-TRONICS, INC.
3212 BURTON AVE., BURBANK, CALIF.

TITLE
PC15F SCHEMATIC

DRAWN 10/1/68
CHK'D 10/1/68
APPR'D 10/1/68
SCALE —
MODEL PC15F
NEXT ASSY. —
SIZE C — 91003-3



ELECTRICAL CONNECTION DIAGRAM

ELECTRICAL REQUIREMENTS		
INPUT	VOLTAGE: DC, NOM.	28
OUTPUT	POWER: VA TOTAL	250
	VOLTAGE: AC	115
	FREQUENCY: HZ	400
	POWER FACTOR	.8 TO 1
	PHASE	1
EFFICIENCY	% AT FULL LOAD	70
ALTITUDE	FEET	45000
WEIGHT	POUNDS	8.2

FIGURE 2.2-4
INSTALLATION AND MOUNTING DIMENSIONS

ITEM	PART NO.	CIRCUIT REF. NO.	DESCRIPTION	NO. REQ'D
	MAT'L			

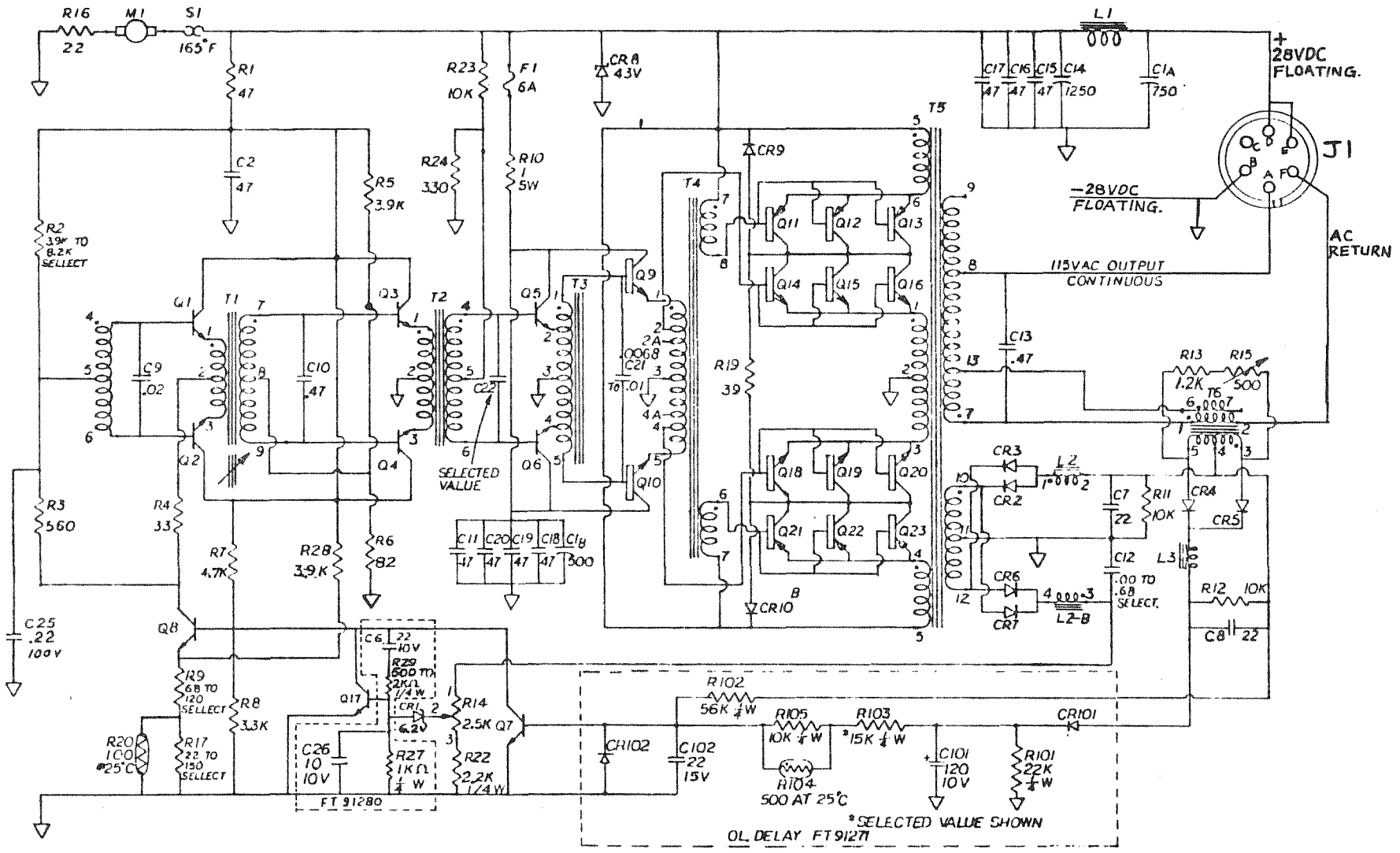
CHG. LTR | E.C.O. NO. | DATE | BY | CHK'D

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL .XX ± .03
.XXX ± .010
FRACTIONAL ± 1/32
ANGULAR ± 5°

FLITE-TRONICS, INC.
3318 BURTON AVE., BURBANK, CALIF.

TITLE
PC-15 G STATIC INVERTER MOUNTING DETAILS

DRAWN Jm 4/5/78
CHK'D 4/6/78
APPR'D 4/6/78
SCALE FULL
MODEL PC15G
NEXT ASSY.
SIZE C
DWG. NO. 91008-6



4. USE CAPACITOR C23 (TYPICALLY .0047μF, 600V.) TO FREQ. LOCK TO OTHER 115VAC 400HZ LINE, PHASE LOCK TO OTHER PC15.B(4) WITH R25
3. MATING PLUG FOR J1: MS 3106B 22-15S.
2. CAPACITORS IN μF: C22 SELECTED AMONG VALUES BETWEEN .002 AND .0068 μF
1. RESISTORS IN OHMS: 1/2 W UNLESS OTHERWISE NOTED

NOTES

FIGURE 3.3-6

FLITE-TRONICS, INC. 2812 BURTON AVE., BURBANK, CALIF.	DRAWN		
	CHK'D		
	APPR'D		
	SCALE		
TITLE PC15G SCHEMATIC	MODEL PC15G		
	NEXT ASSY.		
	SIZE C	DWG. NO. 91003-6	